Akash

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Degree	Institute	Year	CPI/%
M.Tech (Electronic Systems)	IIT Bombay	2025	10.0
B.Tech (Electronics & Communication)	Vellore Institute of Technology	2022	9.48

AREAS OF INTEREST

• Digital VLSI Design • Computer Architecture • RTL Design • Physical Design • Testing and Verification

SCHOLASTIC ACHIEVEMENTS

- Secured **Rank 1** among **110+** MTech students of **EE Department** at **IIT Bombay** *(2024)*
- Secured **AA Grade** in **11** courses including **Processor Design**, **VLSI Design**, **VLSI Design Lab**, **Testing and Verification of VLSI Circuits** and **Hardware Description Languages** at **IIT Bombay** *(2024)*
- Secured **99.27%ile** in **GATE 2022** Electronics and Communications among 54,292 appeared candidates *(2022)*
- Received **Merit Scholarship** for Outstanding Academic Performance for **three** consecutive years in B.Tech *(2022)*

RESEARCH EXPERIENCE

- **Implementation and Optimization of Hardware Accelerators for 5G NR PHY Layer Subsystems**
  Master's Thesis | *Guide:* ***Prof. Sachin B Patkar****, Dept. of EE, IIT Bombay* *(May'24 - Present)*
  Objective: To design and integrate a high performance **5G OFDM** transceiver and hardware accelerator for **5G NR Polar** Error Correcting Codes with **IIT Bombay In-House Developed AJIT Processor**
  Completed Work:
  - Designed a **Programmable Polar Encoder** and **SC Decoder** for code sizes up to **1024** with an **AXI-Stream** interface in Vivado HLS and integrated the design with a **Zynq** Processing System **SoC** using **DMA** in Vivado
  - Achieved **36x** acceleration and **15%** resource utilization for Polar encoder and decoder on **PYNQ-Z2** board
  - Designed a scalable **MATLAB** model for the **Sum-Product** algorithm used in **LDPC decoding**

  Ongoing & Future Work:
  - Currently working on **CRC**-aided **Successive-Cancellation List Decoder** for 5G New Radio standards
  - Implementing **MMSE** based **Channel Estimation** and **Zero Forcing** equaliser for 5G OFDM transceiver
  - Integrating OFDM transceiver blocks into **SoC** with **AJIT** Processor and its **ASIC** implementation
- **Components and Architecture of 5G NR PHY Layer Subsystems for FPGA Implementation**
  Master's Seminar | *Guide:* ***Prof. Sachin B Patkar****, Dept. of EE, IIT Bombay* *(June'23 - December'23)*
  - Reviewed literature on **5G NR** waveforms and FFT-IFFT based architecture for **MIMO-OFDM** systems
  - Studied **ISI mitigation** techniques, including **Cyclic Prefix** insertion and removal, and Channel Estimation models such as **LS**, **MMSE**, and **QR decomposition** algorithms, along with Channel Equalization techniques
  - Literature survey on **DSP Co-Processor** integration with **SHAKTI RISC-V** core by **IIT M** on **Arty-A7**

PUBLICATIONS - PREPRINTS

- M. Datar, D. S. Hegde, V. D. Prasad, M. Prajapati, N. Manikanta, D. Gupta, J. Pavanija, P. Pare, **Akash**, S. Gupta, S. B. Patkar. "**Python-based DSL for Generating Verilog Model of Synchronous Digital Circuits**." arXiv 2406.09208v1. arxiv.org/2406.09208v1

R & D PROJECT

- **Communicating Across Multiple Logic Circuits**
  Guide: ***Prof. Sachin B Patkar****,* ***Prof. Kumar Appaiah*** *, EE Dept., IIT Bombay* *(Jan'24 - May'24)*
  - Designed and tested **Correlator** for **Bias Point Estimation** on the PYNQ-Z2 board for optical communication, achieving **12x** acceleration with **13%** resource utilization and reducing estimation error to less than **0.05%**
  - Implemented **Folding Correlator** in PyHLS (In-House HLS Tool) and tested it on PYNQ-Z2 with AXI-Stream
  - Validated **HLS-NOC** (In-House Tool) project on a scalable QCLDPC decoder and achieved **80x** acceleration

KEY COURSE PROJECTS AND ASSIGNMENTS

- **ASIC Design and FPGA Implementation of LMS Filter |** ***VLSI Design Lab***
  Course Project | *Instructor: Prof. Sachin B Patkar, EE Dept., IIT Bombay* *(Jan'23 - May'23)*
  - Developed and optimized an **LMS Filter** in MATLAB, utilized **HDL Coder** for **RTL design** conversion
  - Executed **RTL to GDSII** flow for LMS Filter using **OpenLane** and **Skywater-130A PDK** for silicon design
  - Performed **Static Timing Analysis** using **Quartus Time-Quest** and tested the design on **Xen-10 Board**
  - Performed **RTL and Gate Level Simulation** using **Model-Sim** and **Icarus Verilog** to verify functionality

- **Implementation of 6-Stage Pipelined RISC Processor | *Processor Design***
  Course Project | *Instructor: Prof. Virendra Singh, EE Dept., IIT Bombay* *(Jan'23 - May'23)*
  - Designed a **6 Stage-Pipelined** 16 bit RISC processor for custom **IITB-RISC** Instruction Set Architecture
  - Incorporated **Data Forwarding Unit** and **Dynamic Branch Predictor** to mitigate pipeline hazards
  - Implemented a synthesizable **Verilog** design in Quartus Prime and verified it with **RTL** simulation in ModelSim
- **Design of Dual Clock Asynchronous FIFO | *Self Project*** *(Jun'23 - Jul'23)*
  - Designed a **Dual Clock Asynchronous FIFO in Verilog**, synthesised and verified the design in **Xilinx Vivado**
  - **Gray Code** encoding is used for inter-clock domain control data transfer to avoid multi-bit signal transition
  - Implemented **2 Flip-Flop Synchronizer** to avoid **meta-stability** issues in **Clock Domain Crossing**
- **Multi Cycle Carpinelli's Very Simple CPU (VSCPU) | *Hardware Description Languages***
  Course Project | *Instructor: Prof. Sachin B Patkar, EE Dept., IIT Bombay* *(Nov'22)*
  - Designed a **16-bit** Multi-Cycle Processor for a custom ISA of **13** instructions using VHDL in QuartusPrime
  - Implemented **CORDIC Algorithm** requiring only **Shifter** and **Adder blocks** for computing trigonometric functions and equipped the processor with the capability of computing **GCD** of two numbers
  - Verified the implemented **VHDL** design with proper testbench using **ModelSim** to validate the functionality
- **Design of 6-bit Flash ADC | *Mixed Signal VLSI Design***
  Course Project | *Instructor: Prof. Rajesh H Zele, EE Dept., IIT Bombay* *(Jan'23 - Apr'23)*
  - Designed a **6-bit Flash ADC** using GPDK **45nm** CMOS technology at a sampling clock frequency of **1 GHz**
  - Realized the design using **Bootstrapped S/H circuit** and **Strong Arm Comparator** in **Cadence Virtuoso**
  - Designed comparator **layout** with DRC & LVS checks, achieving an ENOB of **5.49** bits and SFDR of **44.58 dB**

TEXAS INSTRUMENTS DSP LAB PROJECTS

- **Real-time Dual Tone Multiple Frequency (DTMF) Decoding using TMS320C5535**
  Instructor: ***Prof. Preeti Rao****, EE Dept., IIT Bombay* *(Mar'23)*
  - Implemented **real-time** computation of FFT of input tones using **FFT coprocessor** and **DMA controller**
  - Implemented simple **DTMF decoder** using **peak detection** algorithm which can be used in **Interactive Voice Response (IVR)** systems as a way for callers to navigate their menus
- **Efficient Implementation of FIR Filter using TMS320C5515**
  Instructor: ***Prof. Preeti Rao****, EE Dept., IIT Bombay* *(Feb'23)*
  - Implemented **convolution** in **C** and performed **profiling**, obtained **482 average exclusive counts**
  - Reduced the counts to **30** by implementing the convolution using **circular buffer** in **assembly**

CERTIFICATIONS

- **VSD - Physical Design Flow** *(Aug'24)*
  - Covered **Floorplanning**, **Placement**, **Routing**, **Timing Analysis**, and **Clock Tree synthesis** concepts
- **VSD - Static Timing Analysis - I** *(Jul'24)*
  - Studied **Setup & Hold time**, **Timing Paths** concepts and Methods to **fix Setup & Hold Violations**

TECHNICAL SKILLS

- **Programming Languages :** Verilog, VHDL, Python, TCL, C, MATLAB, Assembly Language
- **Tools and Software :** Quartus Prime & Pro, ModelSim, Xilinx Vivado, Vivado HLS, Code-Composer Studio, Synopsys HSPICE, Cadence Virtuoso, Openlane and Magic Layout, Matlab, NGSpice, AHIR v2-toolchain, LATEX
- **Hardware Platform :** Kintex KC705, Texas Instruments TMS320C5535/5515, Arty-A7, PYNQ-Z2, ZCU-104, Intel De0 Nano, Intel MAX10 (Xen10) and Intel Stratix 10 Tx

RELEVANT COURSES

- VLSI Design
- Hardware Description Languages
- Processor Design
- VLSI Design Lab
- Testing & Verification of VLSI Circuits
- Mixed Signal VLSI Design

POSITIONS OF RESPONSIBILITY

- **Research Assistant** | **SrijaTI TI-DSP Lab**, **IIT Bombay** *(Aug'23 - Present)*
  - Contributed in the **development** of **course material** and lab manuals for the UG and PG **DSP lab** courses
- **Student Companion** | **Institute Student Companion Program (ISCP)** *(Jan'23 - May'23)*
  - Worked in a **team** of **220**+ coordinators, ensuring **smooth transition** of incoming first year PG students

EXTRACURRICULAR ACTIVITIES

- Served with **Red Cross** VIT for one year, contributing to humanitarian assistance and health awareness initiatives
- **Hobbies:** Listening to music, Watching Movies and Reading Comics