**A REPORT**

ON

**TEST SYSTEM DEVELOPMENT FOR  
TESTING RADIATION EFFECTS ON EDAC**



by

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**MAY - JULY 2017**

# BONAFIED CERTIFICATE

This is to certify that this project report entitled “**TEST SYSTEM DEVELOPMENT   
FOR TESTING RADIATION EFFECTS ON EDAC**” submitted to “**Birla Institute of Technology and Science Pilani, Pilani Campus**” is a bonafide work done by “**Aakriti Agrawal**”, ID – 2015A3PS276P under my supervision from **22nd May 2017** to **15th July 2017**.

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# ABSTRACT

Error Detection and corrections (EDAC) functions have been widely used for protecting memories from single event upsets, which occur in environments with high levels of radiation or in deep submicron manufacturing technologies. These errors are caused by various perturbations such as cosmic radiations, solar radiations, galactic noise, electromagnetic radiations and extreme temperature in space which can corrupt the data stored. Error detection techniques allow detecting such errors while error correction enables reconstruction of the original data. The error detection and correction techniques enable reliable delivery of digital data. Therefore, error detection and correction techniques (EDAC) are commonly used for protecting the system against soft errors.

Hamming code is used in the Error Detection and Correction (EDAC). Hamming code algorithm is based on parity bits which can detect and correct up to single bit errors. The extended Hamming code can also detect double bit errors. In this sense, extended Hamming codes are single-error correcting and double-error detecting, abbreviated as SECDED.

The EDAC is integrated with an on-board microcontroller to achieve the evaluation board for the EDAC. The Microcontroller (PIC18F6527) belongs to the PIC18 family. It is controlled using C language written in MPLAB software with XC8 compiler. The Serial ports are used to establish serial communication using USART protocol between the user and the evaluation board. Further, A Graphical user Interface is developed on the C# .NET framework.

# ACKNOWLEDGMENT

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# CHAPTER 1

# INDUSTRY DETAILS

## 1.1 INTRODUCTION TO THE ORGANISATION

Semi-Conductor Laboratory (SCL), an autonomous body under the Department of Space is engaged in Research & Development in the area of Microelectronics to meet the strategic needs of the country. Its aim includes research and development in the field of semiconductor technology. SCL has its origin as the *Semiconductor Complex Limited,* a public sector undertaking of the Government of India. It came under the administrative control of Department of Space in March 2005 and has since undergone organizational restructuring to become focused on research and development. It has integrated facilities / supporting infrastructure, all under one roof and undertakes activities focused on Design, Development, Fabrication, Assembly & Packaging, Testing and Quality Assurance of CMOS and MEMS Devices for various applications SCL is also engaged in Fabrication of Hi-Rel Boards, Radio Sonde Systems and indigenization of electronic sub systems in the existing 6" wafer fab. SCL has over the years developed and supplied a number of key VLSIs, majority of which have been Application Specific Integrated Circuits (ASICs) for high reliability applications in industrial and space sectors. Steps have been initiated to upgrade the facilities to fabricate devices in 0.25 micron or better technology.



Fig. 1-Semi-conductor Laboratory

SCL continues to strive for technological excellence in the field of semiconductor fabrication with a basic objective of:

***“Self-Reliance both in terms of having domestic control over a fundamental building block technology (For Electronics Industry) and in terms of strategic needs.”***

SCL, through its in-house R&D efforts has developed 3 microns, 2 microns, 1.2 microns and 0.8 microns CMOS technologies as well specialized technologies such as EEPROM and CCD. SCL has over the years developed and supplied a number of key VLSIs, majority of which have been Application Specific Integrated Circuits (ASICs) for high reliability and industrial applications.

The Semi-Conductor Laboratory is responsible for design and development of very-large-scale integration (VLSI) devices and development of systems for telecommunication and space sectors. SCL has facilities for fabrication of micro-electronic devices in 0.8 micrometer range and Micro Electro Mechanical Systems. Facilities to fabricate advanced devices in 0.35 micrometer range are planned.

## 1.2 SCL VISION

* Create a strong R&D base in the country in the field of Microelectronics.
* Design and Development of devices in cutting edge technology.
* Manufacture VLSI/MEMS based systems & sub-systems.
* Transform SCL as a centre of Excellence in microelectronics in the country.

## 1.3 TECHNICAL ACTIVITIES

For intense research and development and obtaining better results, SCL constitutes of various departments wherein different technical activities are carried out:

* VLSI Design and Process Development
* VLSI and MEMS Fabrication, Assembly and Testing
* Engineering and Assembly
* Screening of Components and Hi-Reliability Fabrication
* Technical Support Services
* Reliability and Quality Assurance

# CHAPTER TWO

# DEPARTMENTS IN ORGANIZATION

## 2.1 TECHNICAL DIVISIONS

### 2.1.1 VLSI DESIGN

SCL has developed suites implementing full Electronic Design Automation (EDA) Flows forDigital, Mixed Signal and Analog ASIC Design. Wide spectrum industry standard EDA toolsviz. Cadence /Synopsys Design tools backed by state of the art hardware and a highlyexperienced design team isthe core strength of SCL.



Fig. 2- System Assembly Facility

#### KEY DESIGN CAPABILITIES:

* References
* Power Management
* Data Converters
* Sensor Interfaces, Amplifiers
* Systems on Chip (SOCs)

#### ASIC/ Logic Design Implementation

* HDL Code/ Gate level Netlist/ Schematic Entry
* Synthesis/ DFT/ ATPG/ Embedded Memory
* Layout and Physical Verification

#### Handling of Electronic Design Automation and Tools at Various Steps

* Analog /Digital/ Mixed Signal Design Flow
* Script Writing

### 2.1.2 SYSTEM ASSEMBLY

System Assembly Division of SCL is engaged in Design and Development of Electronic Systems & Subsystems. The resources include Assembly stations, Test & Measurement Equipment, Calibrators, Chambers to undertake assembly and testing of electronic systems conforming to ISRO PAX and MIL Standards.



Fig. 3- System Assembly Facility

#### KEY CAPABILITIES

* Product Development & Prototyping
* Qualification / Type Testing
* Product Approval
* Assembly of Systems/ Sub-Systems and Boards

### 2.1.3 VLSI ASSEMBLY AND PACKAGING

VLSI & MEMS Packaging facility operating in Class 100 and Class 10000 Clean Rooms includes Die Bonders, Ball & Wedge Wire Bonders, Multi-Zone Furnaces for Hermetic Sealing, Multi-Function Bond Pull Testers, Laser Welder, Dicing Saw, Tape Mounter etc.



Fig. 4- Assembly & Packaging Facility

#### KEY CAPABILITIES

* Fine Pitch Bonding capability for pad size of 57µmx57µm and 65µm pitch.
* Capability of developing customised ceramic packages to address signal integrity and reliability issues for ASICs in 180nm Process Assembly of Systems/ Sub-Systems and Boards.
* Low Temperature Process for packaging large dies.
* Multi-Chip Packaging Process for ASICs and sensor devices.
* MIC Packaging.

### 2.1.4 VLSI & MEMS TESTING

VLSI and MEMS Test Facility meets the demanding test requirements of complex, high speed and high pin count Integrated Circuits in Digital, Mixed Signal and Analog domains. The Facility also caters to testing of a variety of MEMS and RF devices such as Pressure, Temperature & Humidity Sensors, Accelerometers, RF Switches and Band-Pass Filters.

Test plan and engineering activities implemented at various stages of product development include:

* Prototype Testing/Debug at wafer and device level.
* Device characterization.
* Volume testing on Automatic Test Equipment.



Fig. 5-VLSI & MEMS Testing Facility

#### KEY CAPABILITIES

* 8” / 6” wafer probing capability.
* High Pin Count Probe Card building expertise.
* Characterization of Digital, Mixed Signal and Analog devices from –55°C to 125°C up to 256 pins (400 MHz clock rate).
* Expertise to develop Test Programs for variety of devices such as Digital ASICs, Mixed Signal ASICs, CCDs, Imager devices, ADC, DAC, SRAM, Voltage Regulators, Op-amp etc.
* Design capability for multilayer & high speed Device Interface Boards.
* Characterization of Pressure Sensors (up to 600 bar), Temperature Sensors ( -90°C to 180°C), Humidity Sensors (10%RH to 95%RH ) & Accelerometers (up to 20g).
* Characterization of RF devices up to 40GHz.

### 2.1.5 RELIABILITY& QUALITY ASSURANCE

The Reliability & Quality of the Devices/ boards/ sub-systems/ systems manufactured at SCL is maintained throughout design, chip fabrication, assembly/ packaging and testing phases. Regular inline QA Inspection/Audits are carried out to ensure defect free manufacturing. Screening and Qualification of products for required applications is an integral part of the process. The quality & reliability assurance requirements are guided by global performance specifications as per MIL-PRF-38535, JEDEC, MIL-883 and other relevant standards. Continuous Improvements in processes are implemented through feedbacks at appropriate stages and performing failure analysis. The key features includeScreening & Qualification of VLSI / MEMS devices / boards / sub-systems / systems, Process Qualification, Device Failure Analysis, and Process Audits. The screening of devices is carried out to ensure their suitability for a given application by appropriate selection of tests, their duration and severity. The screening activities are carried out in Static Safe areas in controlled temperature and humidity conditions.



Fig. 6- Environment Test Facility

### 2.1.6 PROCESS TECHNOLOGY DEVELOPMENT DIVISION

In PTDD, a variety of processes catering to the different requirements of fabrication of digital, mixed signal IC’s and that of electro-optical image sensors are available. These processes have been developed in house through the efforts of a team of process engineers on the Class-10, 6inch Wafer Fabrication Facility-the facility is designed and equipped to meet the requirements of 0.8 micron CMOS and CMOS-compatible process technologies.

### 2.1.7 VLSIFABRICATION FACILITY

SCL has an 8’’ Wafer Fabrication Facility with following key features:

* 180 nanometre CMOS process for Fabrication of products in Digital, Mixed Signal and Analog Domains.
* Process Equipment Line, In-Line Inspection and Metrology Tools and Support Utilities as per international standards.
* Clean Rooms of Class 1, 10, 100 and 1000 with controlled environmental conditions
* Dedicated bays for Wafer Fabrication processes viz. Diffusion, Lithography, Etching (Dry & Wet), Implantation, Thin Films working seamlessly from Wafer-In to Wafer-Out.
* Best Known Methods comprising regular tool QCs, Preventive Maintenance and Process Control and Monitoring through in-line defect inspection & Measurement through Metrology Tools as per industry standards.
* Commensurate with the requirements of Fab Line, support infrastructure namely High Purity Systems, Utility Plants and Distribution Network operating on 24x7 basis.

CMOS Processes

* Thin Film Growth, Deposition, and Doping
* Lithography
* Etching(Wet and Dry)
* Implantation

Post CMOS Processes (MEMS Specific Processes)

* Surface micromachining
* Bulk Micromachining
* Wafer Bonding(Eutectic & Anodic)
* E-Beam Evaporation Metal Deposition

|  |  |
| --- | --- |
| Gate Density | 100K gates/mm |
| Core Clock | 800 MHz |
| I/O Data Rate | 130 MHz @40 pF & 20 nH |
| Bit Cell Size (SRAM) | 4.7 µm²/bit (14 Mbit SRAM) |
| Metal Layers | 4-6 |
| Power Supply(VDD) | 1.8V core CMOS & 3.3V I/O |
| Gate Delay | 27.3-29.4 ps/gate |

Table 1- Key Capabilities of 180 Nanometer Technology at SCL

# CHAPTER 3

# INTRODUCTION TO THE TESTING DEPARTMENT

## 3.1 VLSI TESTING DIVISION

Testing is used to screen out a small fraction of the total production volume at various stages in the manufacturing process. Defective products are usually repaired and returned to the thrown out. Although some testing is done during device fabrication, most of the testing is performed after the semiconductor wafers have been fabricated. The first such test is called wafer probe or sort. Here wafers are tested by electro gas machine in which bad dyes are marked with inker. The inked wafer is sent to the assembly section where good dyes are separated from the bad ones. Wafer after fabrication and testing in the main plant come to the assembly department where dies are converted into devices.

## 3.2 NECESSITY OF VLSI TESTING

Ever-growing scale, ever-increasing complexity, and ever-shrinking process feature sizes make the design of VLSI circuits highly prone to design errors and their fabrication to manufacturing defects. Therefore, VLSI design verification is needed on the design side to determine whether a design is error-free, while VLSI testing is needed on the manufacturing side to determine whether a fabricated VLSI circuit is defect-free.

## 3.3 ROLES OF TESTING

* Detection: Determination of whether or not the device under test (DUT) has some fault.
* Diagnosis: Identification of a specific fault that is present on DUT.
* Device characterization: Determination and correction of errors in design and/or test procedure.
* Failure mode analysis (FMA): Determination of manufacturing process errors that may have caused defects on the DUT.

## 3.4 TESTING PRINCIPLE

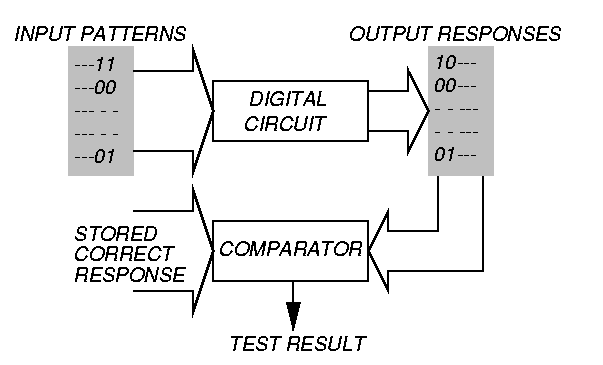
**

Fig. 7Basic Testing Principle

VLSI testingis conducted by applying test stimuli to the circuit-under-test (CUT), measuring actual circuit responses, and comparing them with expected circuit responses. The CUT is declared defective if measured and expected circuit responses do not match with each other.

When yield improvement or reliability enhancement is required, detailed failure analysis needs to be conducted to identify the location and the root-cause of the defect(s).There are two basic goals in VLSI testing, namely highest quality andlow test costs.

## 3.5TYPES OF TESTING

Different types of tests are conducted on every single device pre and post device fabrication and also during manufacture, each having a different test purpose.

* Verification Testing*-* Verifies correctness of design and of test procedure(software approach)
* Characterization Testing- Used to characterize devices and performed through production life to improve the process, hence yield.
* Manufacturing Testing-Factory testing of all manufactured chips for parametric faults and for random defects. For example, Wafer test, packaged device tests, Parametric Tests, Functional tests. Some functions of Manufacturing Testing are

1. Determines if manufactured chip meets specs

2. Must cover high % of modeled faults

3. Minimize test time (to control cost)

4. Go/no-go decision is made

5. Tests every device on chip

6. Tests are functional or at speed of application or speed guaranteed by supplier.

## 3.6 TERMS THAT APPLY TO DEVICE TESTING

1**. DC Testing**: When a voltage/current is measured during the test and fail results are based upon the measured value.

2. **Functional Testing**: When the device is actively performing logical functions, I/P data is supplied to the DUT and O/P data is read from the DUT, the functional comparator circuitry located on the pin electronic card is used to determine the pass/fail results of the test.

3**. AC Testing**: AC testing guarantees that the device meets all the timing specifications. AC testing is performed by setting up the appropriate timing values (edge placements) and the signal format is defined in the device and then executing a functional test sequence.

4. **Wafer Test**: Testing of individual dies when they are still in wafer form. This is the first attempt of separating the good dies from the bad ones. This activity is also referred to as Wafer Sort.

5**. Package Test**: Wafer are cut into individual dies and each die is then assembled into a package. The packaged device is then tested to ensure that assembly process was correctly performed and to verify that the device still meets its design specification. Package test is also called Final Test.

## 3.7TESTSPECIFICATIONS

### 3.7.1 THE TEST PROGRAM

The purpose of a semi-conductor test program is to control the test hardware in a manner that will guarantee that the DUT (Device under Test) meets or exceeds all of its design parameters. The design parameters are defined in detail in device specification. While carrying out the testing of a digital semi-conductor device, the test program is often segmented into three parts:

1. DC Test
2. Functionality Test
3. AC Test

The test program controls the test system hardware so that each test is performed in a manner that will result in a pass or a fail condition. If the test result is a pass, the device meets or exceeds the design specifications and if the result is a failure, the device does not operate within its specifications and should not be used in its intended application.

The test program must also be capable of controlling external hardware such as device handlers or wafer probers. It must collect test result and present the results in a summarized form. The test results provide valuable information to the test and product engineers and can be used to help increase yields.

### 3.7.2 PARAMETES THAT APPLY TO DC TESTING

When developing the DC test plan, the following information must be determined.

1. Input voltages and currents.
2. Output voltages and currents.
3. Power supply current and voltages.
4. Pass/Fail limits for each parameter.

### 3.7.3 PARAMETES THAT APPLY TO FUNCTIONAL AND AC TESTING

When developing AC test plan, the following information must be determined.

1. Input Conditions (VIL, VIH)
2. Output Conditions (VOL,VOH, IOL, IOH)
3. Timings (frequency, pulse widths)
4. Pass/Fail limits for each parameter.

## 3.8VLSI TEST DIVISION

The VLSI and MEMS Test Facility meets the demanding test requirements of complex, high speed and high pin count Integrated Circuits in digital, analogue and mixed signal domains. The facility also caters to testing of a variety of MEMS devices such as Pressure Sensors, Temperature Sensors and Accelerometers.

Test plan and engineering activities are implemented at various stages of product development include:

* Prototype testing/Debug at wafer and device level
* Device characterization
* Volume testing by Test program development on ATE



Fig. 8VLSI test division

#### KEY CAPABILITIES

* 8” / 6” wafer probing capability.
* High Pin Count Probe Card building expertise.
* Characterization of Digital, Mixed Signal and Analog devices from –55°C to 125°C up to 256 pins (400 MHz clock rate).
* Expertise to develop Test Programs for variety of devices such as Digital ASICs, Mixed Signal ASICs, CCDs, Imager devices, ADC, DAC, SRAM, Voltage Regulators, Op-amp etc.
* Design capability for multilayer & high speed Device Interface Boards.
* Characterization of Pressure Sensors (up to 600 bar), Temperature Sensors (-90°C to 180°C), Humidity Sensors ( 10%RH to 95%RH ) & Accelerometers (up to 20g).

### 3.8.1 TESTESR IN VLSI TEST LAB

1. Mixed Signal VLSI Tester:

The Mixed Signal VLSI Tester is one of the latest test platforms with capabilities to characterize analog, digital and mixed signal devices with up to 256 digital pins (400 MHz Clock Rate) and analog operation.



Fig. 9Mixed Signal Ultra Flex Tester

The test resources include:

* 20 DC channels having ±30V @ 200mA
* DC channels having +75V @ 200mA
* 256 Digital Channels @ 400 MHz Clock/Data rate un-compromised.
* Analog Instrumentation(DC to 150 MHz)
* Devices can be characterized in the temperature range of -55⁰C to 125⁰C using precision Temperature test equipment.

1. MEMS Tester

Making use of the MEMS Tester, the following MEMS Devices are tested:

* Pressure Sensors:
* Upto 6 bar for wafer level die testing
* Upto 600 bar for device testing
* Temperature Sensors from -20⁰C to 150⁰C
* Accelerometers upto ± 20g



Fig. 10-MEMS Tester

1. Wafers Probers

Two different wafer probers are present in VTD to test 8 and 6 inch wafers.

* 8’’ Automatic Wafer Prober
* 6’’ Semi-Automatic Wafer Prober



Fig. 11- Wafer Prober

1. ASIX-2 Tester

The ASIX-2 TESTER is designed to:-

* Focus exclusively on testing ASIC
* Suit the specific needs of the ASIC community
* Perform fast and easy testing of devices
* Eliminate the need to learn a programming language
* Be a cost effective test solution
* Generate test program automatically
* Automate test program generation
* Satisfy the need of the production environment.

1. STS 3000 Tester

STS 3000 test system perform high-speed precision tests on linear & mixed technology semiconductor devices and PC modules. Test applications include: Pulse width module power supply controllers, voltage regulator, integrated power devices, power buffers, operational amplifier, A/D & D/A converters and data acquisition subsystems.

The STS 3000 processing architecture employs a MC68020-based microcomputer in each test station to execute test plans, manage test data & control system hardware during testing. The station computer also controls system diagnostics & supports networked comm. through Ethernet interface. Memory capacity includes up to 16 MB of dynamic RAM, 160-MB Winchester disk & 51/4 inches streaming tape drive.

The software environment is based on the UNIX operating system. The test operating system is a menu drive utility, which manages run time operations including data management such as data logging etc.

Test plans are based on the structural language Pascal, which facilitates efficient and self-documenting programs. Axiom Pascal is an enhanced version of the standard language and test plan is linked to a library of procedures used to control test hardware. System hardware is designed to ensure applications flexibility, system expandability & maintainability. Synchronized source/measurement functions enhanced system performance, especially in mixed technology test applications.

## 3.9 VLSI PRODUCTS

VLSI design covers a variety of activities starting from functionality and specification generation till post-fab product qualification - activities such as architecture finalization, RTL design, simulations, floor planning, layout, physical verification, post-layout simulations, GDSII release, device fabrication, wafer sorting, packaging, device test and qualification are all part of the process. Over 80 ASIC products have been designed for a variety of applications in professional sectors including Telecomm, Railways, Medical and the Consumer Sector. Low-geometry designs for four standard products, namely LDO Regulator, Buck Converter, Boost converter and temperature sensor have also been carried out.

Besides ASICs, Application Specific Standard Products (ASSP) like data converters, codec, tone ringer, speech circuit, DTMF generator, single chip telephone, energy meter (1 phase and 3 phases), Hearing Aid, etc. were designed and developed. MANAS (Multiplexed Analog Signal processor) was designed, characterized and mass produced for ALICE experiment conducted at CERN, Geneva.

#### STANDARD VLSI PRODUCTS:

* Tone Pulse Switchable Dialler
* Single Chip Telephone IC
* Single Chip Codec with Filter
* DTLMUX
* Analog Watch
* Multifunction Digital Clock with Timer
* Time Slot Zero Transmitter
* Time Slot Zero Receiver
* Hearing Aid IC

#### ASICs & ASSPs:

* Programmable Signal Processor(PSP-I)
* Programmable Timer
* Water Purifier ASIC
* Smoke Detector ASIC
* Signal Processing Card ASIC
* Conference Card ASIC
* Pulse Cord Modulator Encoder
* Infinite Impulse Response Filter
* Direct Memory Access Controller
* Hearing Aid ASIC
* Line Card ASIC
* STD PCOASIC
* Radio Sonde ASIC
* Multiplexed Analog Signal Processor(MANAS)
* GIST-11(Graphical and Intelligence Based Scripting Technology)

#### SYSTEMS

* Digital Pair Gain
* HDSL
* Electronic Energy Meter
* OPTIMUX Range Of Products
* SDH (Synchronous Digital Hierarchy)
* DLC (Digital Loop Carrier)

# CHAPTER 4

# INTRODUCTION TO EDAC

## 4.1 INTRODUCTION

The general idea for achieving error detection and correction is to add some [redundancy](https://en.wikipedia.org/wiki/Redundancy_(information_theory)) (i.e., some extra data) to a message, which receivers can use to check consistency of the delivered message, and to recover data that has been determined to be corrupted. Error-detection and correction schemes can be either [systematic](https://en.wikipedia.org/wiki/Systematic_code) or non-systematic: In a systematic scheme, the transmitter sends the original data, and attaches a fixed number of check bits (or parity data), which are derived from the data bits by some [deterministic algorithm](https://en.wikipedia.org/wiki/Deterministic_algorithm). If only error detection is required, a receiver can simply apply the same algorithm to the received data bits and compare its output with the received check bits; if the values do not match, an error has occurred at some point during the transmission. In a system that uses a non-systematic code, the original message is transformed into an encoded message that has at least as many bits as the original message.

Good error control performance requires the scheme to be selected based on the characteristics of the communication channel. Common [channel models](https://en.wikipedia.org/wiki/Channel_model) include memory-less models where errors occur randomly and with a certain probability, and dynamic models where errors occur primarily in [bursts](https://en.wikipedia.org/wiki/Burst_error). Consequently, error-detecting and correcting codes can be generally distinguished between random-error-detecting/correcting and burst-error-detecting/correcting. Some codes can also be suitable for a mixture of random errors and burst errors.

Electrical or magnetic interference inside a computer system can cause a single bit of [dynamic random-access memory](https://en.wikipedia.org/wiki/Dynamic_random-access_memory) (DRAM) to spontaneously flip to the opposite state. It was initially thought that this was mainly due to [alpha particles](https://en.wikipedia.org/wiki/Alpha_particle) emitted by contaminants in chip packaging material, but research has shown that the majority of one-off [soft errors](https://en.wikipedia.org/wiki/Soft_error) in DRAM chips occur as a result of [background radiation](https://en.wikipedia.org/wiki/Background_radiation), chiefly [neutrons](https://en.wikipedia.org/wiki/Neutron) from [cosmic ray](https://en.wikipedia.org/wiki/Cosmic_ray) secondaries, which may change the contents of one or more memory cells or interfere with the circuitry used to read or write to them. Hence, the error rates increase rapidly with rising altitude; for example, compared to the sea level, the rate of [neutron flux](https://en.wikipedia.org/wiki/Neutron_flux) is 3.5 times higher at 1.5 km and 300 times higher at 10–12 km (the cruising altitude of commercial airplanes). As a result, systems operating at high altitudes require special provision for reliability.

As an example, the spacecraft [Cassini–Huygens](https://en.wikipedia.org/wiki/Cassini%E2%80%93Huygens), launched in 1997, contains two identical flight recorders, each with 2.5 gigabits of memory in the form of arrays of commercial DRAM chips. Thanks to built-in [EDAC](https://en.wikipedia.org/wiki/Error_detection_and_correction) functionality, spacecraft's engineering telemetry reports the number of (correctable) single-bit-per-word errors and (not correctable) double-bit-per-word errors. During the first 2.5 years of flight, the spacecraft reported a nearly constant single-bit error rate of about 280 errors per day. However, on November 6, 1997, during the first month in space, the number of errors increased by more than a factor of four for that single day. This was attributed to a [solar particle event](https://en.wikipedia.org/wiki/Solar_particle_event) that had been detected by the satellite [GOES 9](https://en.wikipedia.org/wiki/GOES_9).

## 4.2HAMMING CODE

In telecommunication, Hamming codes are a family of linear error correcting codes that generalize the Hamming (7, 4)-code, and were invented by Richard Hamming in 1950. Hamming codes can detect up to two-bit errors or correct one-bit errors without detection of uncorrected errors. By contrast, the simple parity code cannot correct errors, and can detect only an odd number of bits in error. Hamming codes are perfect codes, that is, they achieve the highest possible rate for codes with their block length and minimum distance of three.

Hamming algorithm is the most straightforward and relatively simple to implement on software as well as hardware. In comparison to other codes, hamming acquires lesser area and avoids the complexities related to the decoder. Hamming encoding involves deriving a set of parity check bits covering different subsets of bits comprising a data word and concatenating or merging the check bits with the original data word.

Decoding involves recalculating parity over the encoded data word, including the parity check bits. The parity check bits calculated at the encoder are designated syndrome bits and define what is known as the syndrome vector. The ability to correct single bit errors is provided by specifying encoding parity check relationships such that single bit errors in the encoded data words yield unique and specific syndrome vectors.

With Hamming-based codes, double error detection is typically provided by an additional parity check bit across all the data and other parity bits. Double bit errors are indicated when the syndrome bit corresponding to the overall parity is 0 and one or more of the other syndrome bits is 1. Hamming codes are widely used. In this context, an extended Hamming code having one extra parity bit is often used. Extended Hamming codes achieve a Hamming distance of four, which allows the decoder to distinguish between when at most one one-bit error occurs and when any two-bit errors occur. In this sense, extended Hamming codes are single-error correcting and double-error detecting, abbreviated as SECDED.

Due to the limited redundancy that Hamming codes add to the data, they can only detect and correct errors when the error rate is low. This is the case in computer memory (ECC memory), where bit errors are extremely rare.

|  |  |
| --- | --- |
| P0 | XOR(D0,D1,D3,D4,D6) |
| P1 | XOR(D0,D2,D3,D5,D6) |
|  | XOR(D1,D2,D3,D7) |
| P3 | XOR(D4,D5,D6,D7) |
| P4 | XOR(P0,P1,P2,P3 ,D0-D7) |

|  |  |
| --- | --- |
| S0 | XOR(P0,D0,D1,D3,D4,D6) |
| S1 | XOR(P1,D0,D2,D3,D5,D6) |
| S2 | XOR(P2,D1,D2,D3,D7) |
| S3 | XOR(P3,D4,D5,D6,D7) |
| S4 | XOR(P0,P1,P2,P3,P4 ,D0-D7) |

# CHAPTER 5

# EDAC HARDWARE SPECIFICATIONS

## 5.1 EDAC

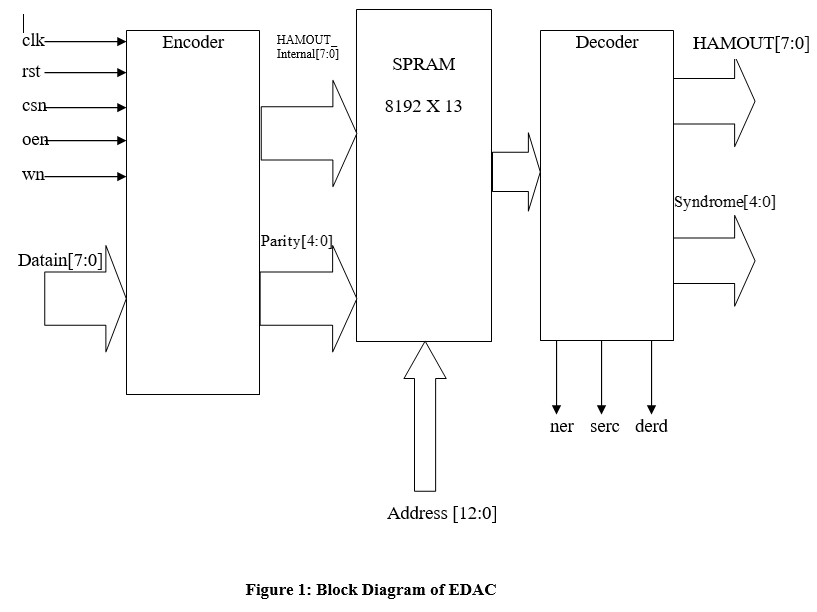


Fig. 12Block Diagram of EDAC

## 5.2 GENERAL SPECIFICATIONS

* Technology : 0.18µ SCL CMOS Process
* Operating voltage(VDDO) : 3.3V± 10%
* Operating voltage(VDD) : 1.8V± 10%
* Compatibility : CMOS compatible I/O
* Operating frequency : 20 MHz
* Total no. of Pads : 64
* Total no. of Pins : 64
* Package Type : 64 pin Ceramic Quad Flat Pack (CQFP)

# CHAPTER 6

# PIC18F6527 MICROCONTROLLER

## 6.1 PERIFERAL INTERFACE CONTROLLER (PIC)

PIC (usually pronounced as "pick") is a family of microcontrollers made by Microchip Technology. The first parts of the family were available in 1976; by 2013 the company had shipped more than twelve billion individual parts, used in a wide variety of embedded systems.

Early models of PIC had read-only memory (ROM) or field programmable EPROM for program storage, some with provision for erasing memory. All current models use flash memory for program storage, and newer models allow the PIC to reprogram itself. Program memory and data memory are separated. Data memory is 8-bit, 16-bit, and, in latest models, 32-bit wide. Program instructions vary in bit count by family of PIC, and may be 12, 14, 16, or 24 bits long.

The hardware capabilities of PIC devices range from 6-pin SMD, 8-pin DIP chips up to 144-pin SMD chips, with discrete I/O pins, ADC and DAC modules, and communications ports such as UART, I2C, CAN and even USB.

The manufacturer supplies computer software for development known as MPLAB, assemblers and C/C++ compilers, and programmer/debugger hardware under the MPLAB and PICKit series. Third party and some open-source tools are also available.

PIC devices are popular with both industrial developers and hobbyists due to their low cost, wide availability, large user base, extensive collection of application notes, availability of low cost or free development tools, serial programming, and re-programmable Flash memory capability.

## 6.2 DEVICE FEATURES

* Operating Frequency DC - 40 MHz
* Program Memory (Bytes) - 48K
* Program Memory (Instructions) - 24576
* Data Memory (Bytes) - 3936
* Data EEPROM Memory (Bytes) - 1024
* Interrupt Sources - 28
* I/O Ports - Ports A, B, C, D, E, F, G Ports
* Timers - 5
* Capture/Compare/PWMModules -2
* Enhanced Capture/Compare/PWM Modules- 3
* Enhanced USART - 2
* Serial Communications - MSSP,Enhanced USART
* Parallel Communications (PSP) - Yes
* 10-bit Analog-to-Digital Module - 12 Input Channels
* Resets (and Delays) - POR, BOR,RESET Instruction,Stack Full, StackUnderflow (PWRT, OST),MCLR (optional), WDT
* ProgrammableHigh/Low-Voltage Detect- Yes
* Programmable Brown-outReset- Yes
* Instruction Set - 75 Instructions;83 with ExtendedInstruction Set enabled
* Packages - 64-pin TQFP

## 6.3 SPECIAL MICROCONTROLLER FEATURES:

* C compiler optimized architecture:- Optional extended instruction set designed to optimize re-entrant code
* 100,000 erase/write cycle Enhanced Flash program memory typical
* 1,000,000 erase/write cycle Data EEPROM memory typical
* Flash/Data EEPROM Retention: 100 years typical
* Self-programmable under software control
* Priority levels for interrupts
* 8 x 8 Single-Cycle Hardware Multiplier
* Extended Watchdog Timer (WDT):- Programmable period from 4 ms to 131s
* Single-Supply In-Circuit Serial Programming™ (ICSP™) via two pins
* In-Circuit Debug (ICD) via two pins
* Wide operating voltage range: 2.0V to 5.5V
* Fail-Safe Clock Monitor
* Two-Speed Oscillator Start-up
* NanoWatt Technology

## 6.4 PIN DIAGRAM

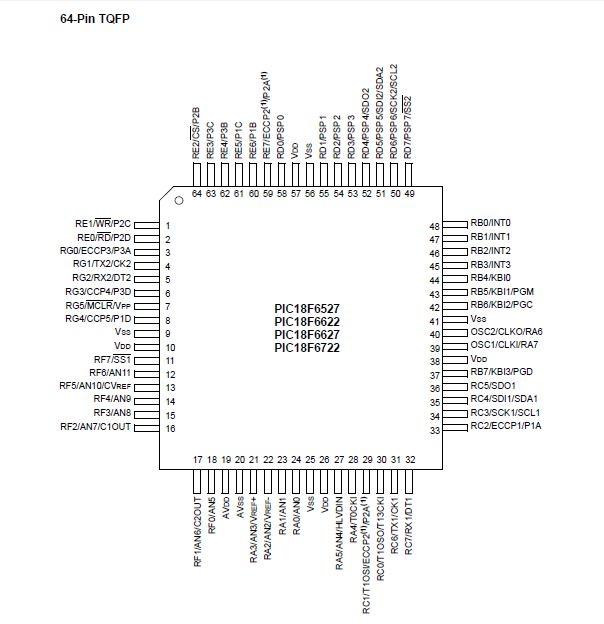


Fig. 13 PIC18f6527 pin configuration

# CHAPTER 7

# OTHER COMPONENTS AND DEVICES USED

## 7.1 PRINTED CIRCUIT BOARD

A printed circuit board (PCB) mechanically supports and electrically connects electronic components using conductive tracks, pads and other features etched from copper sheets laminated onto a non-conductive substrate. Components are generally soldered on the PCB.

In this project, a 4-layer PCB has been designed using OrCAD software. The four layers being Top, Power, Ground and Bottom.

* Top layer: PIC18F6527,SC-1702-0 SRAM, DB50, MAX 232, 10uF capacitors
* Power Layer: Routing of Three Power lines (3.3VDDO,1.8VDD,3.3VDD)
* Ground layer: Copper Pour
* Bottom Layer: SC-1702-0 SRAM, DB50, 0.1uF Capacitors, MAX 232

For the completion of the setup, this PCB is connected to

* Personal Computer for Serial Communication using DB9, to provide a conduit of communication between PCB and User.
* Real Ice In-Circuit Emulator using 5 Pin Connector, to emulate and debug the firmware on the PCB.
* Power Supply via DB 50, using 3 channels (1.8V, 3.3V and 3.3 V˘) of the Power Supply, to power up the test board.



Fig. 14- A PCB as a design on a computer and a board-assembly populated with components.

## 7.2 MAX232

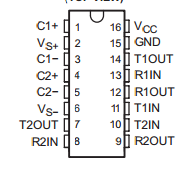
As the RS 232, which is being used for serial communication with personal computer is not compatible with microcontrollers (PIC, in this case), a line driver is needed to convert RS232 voltage levels to TTL voltage levels, that will be acceptable to the PIC18’s RX and TX pins.

Thus, MAX232 IC is being used to convert the RS232 to TTL voltage levels, and vice versa. The operating voltage of MAX232 is 3 V to 5V, which is in the range of the operating voltage of PIC. It is a 16 pin DIP IC having line drivers for TX pin as T1 and T2 and line drivers for RX pin as R1 & R2. Detailed pin description is given in the annexure.

### 7.2.1 Features

* Meets or Exceeds TIA/EIA-232-F and ITU includes a capacitive voltage generator to supply Recommendation V.28 TIA/EIA-232-F voltage levels from a single 5-V
* Operates from a Single 5-V Power Supply with supply. Each receiver converts TIA/EIA-232-F inputs 1.0-µF Charge-Pump Capacitors to 5-V TTL/CMOS levels.
* Operates up to 120 kbit/s typical threshold of 1.3 V, a typical hysteresis of 0.5 V, and can accept ±30-V inputs.

### 7.2.2 Pin Configuration and Functions



**Fig. 15-**Pin Diagram of MAX232

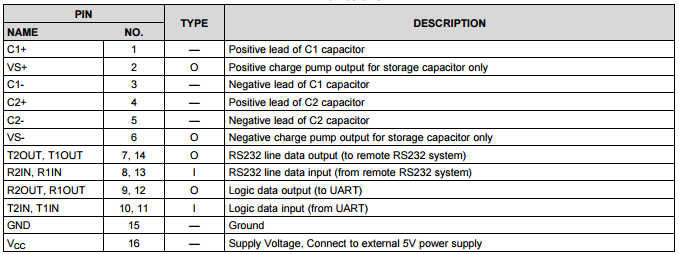


Table 2- Pin Configuration of MAX232 16 Pin IC

## 7.3 RS 232

RS-232 is a standard for serial communication transmission of data. It formally defines the signals connecting between a DTE (data terminal equipment) such as a computer terminal, and a DCE (data circuit-terminating equipment), such as a modem. The RS-232 standard is commonly used in computer serial ports.

The standard defines the electrical characteristics and timing of signals, the meaning of signals, and the physical size and pin-out of connectors.

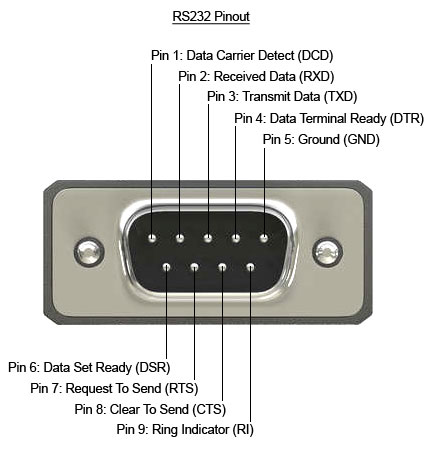


Fig. 16- RS232

An RS-232 serial port was once a standard feature of a personal computer, used for connections to modems, printers, mice, data storage, uninterruptible power supplies, and other peripheral devices.

Some of the major disadvantages of RS-232, when compared to other serial interfaces such as RS-422, RS-485 and Ethernet are

* Low transmission speed,
* Short maximum cable length,
* Large voltage swing,
* No multipoint capability

RS-232 interfaces are still used—particularly in industrial machines, networking equipment, and scientific instruments where a short-range, point-to-point, low-speed wired data connection is adequate.

### 7.3.1 Pin Description of DB9 Connector (RS-232)

|  |  |  |  |
| --- | --- | --- | --- |
| **Pin** | **SIG.** | **Signal Name** | **DTE (PC)** |
| 1 | DCD | Data Carrier Detect | In |
| 2 | RXD | Receive Data | In |
| 3 | TXD | Transmit Data | Out |
| 4 | DTR | Data Terminal Ready | Out |
| 5 | GND | Signal Ground | - |
| 6 | DSR | Data Set Ready | In |
| 7 | RTS | Request to Send | Out |
| 8 | CTS | Clear to Send | In |
| 9 | RI | Ring Indicator | In |

Table 3- Pin Configuration of DB9 Connector (RS-232)

## 7.4 MIXED SIGNAL OSCILLOSCOPE

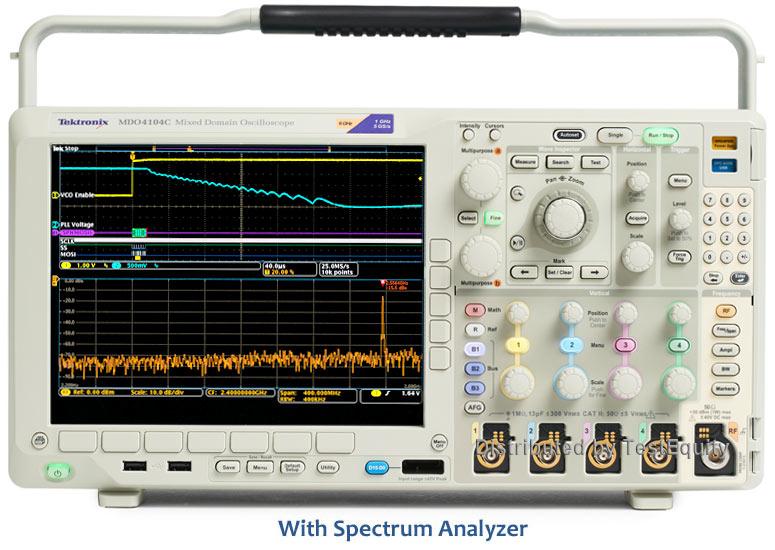
A mixed signal oscilloscope (MSO) has two kinds of inputs, a small number of analog channels (typically two or four), and a larger number of digital channels (typically sixteen). It provides the ability to accurately time-correlate analog and digital channels, thus offering a distinct advantage over a separate oscilloscope and logic analyser. Typically, digital channels may be grouped and displayed as a bus value displayed at the bottom of the display in hex or binary. On most MSOs, the trigger can be set across both analog and digital channels.

### 7.4.1 Key Performance Specifications

* 1GHz, 500MHz, 350MHz, and 100MHz bandwidth models.
* 2 to 4 analog models
* Up to 20 mega-point record length on all channels
* >50,000 waveform/s maximum capture rate
* Standard passive voltage probes with less than 4pF capacitive loading and 500MHz or 1GHz analog bandwidth.

### 7.4.2 Key Features

* Wave Inspector controls provide easy navigation and automated search for waveform data.
* 41 automated measurements, and FFT analysis for simplified waveform analysis.
* 16 digital channels (MSO Series)
* Mixed signal design and analysis (MSO Series)
* Optional serial triggering and analysis-automated serial triggering. Decode.
* Tek VPI Probe interface supports active, differential, and current probes pr automatic scaling and units.

[](https://www.google.co.in/url?sa=i&rct=j&q=&esrc=s&source=images&cd=&cad=rja&uact=8&ved=0ahUKEwiT7rCLhPTTAhVCLo8KHYdIAWkQjRwIBw&url=https://www.testequity.com/products/32772/&psig=AFQjCNHUcEPWgmFGwHVvdc7ElGQLUYXszQ&ust=1495010958336135)

**Fig. 17-**MSO4104 TEKTRONIX Oscilloscope

# CHAPTER 8

# EDAC SOFTWARE SPECIFICATIONS

## 8.1 MPLAB X IDE

MPLAB X IDE is a software program that is used to develop applications for Microchip microcontrollers and digital signal controllers. The development tool is called an Integrated Development Environment, or IDE. EDAC is controlled using PIC18F6527. PIC is programmed using C language using MPLAB 2.24 IDE.

In this project, the development of the test program which is to be emulated in PIC microcontroller is described and briefly explains how MPLAB X IDE from Microchip is used in the process.

### 8.1.1 DEVELOPMENT OF PROGRAM

**STEP 1**

1. Choose “Microchip Embedded”.
2. Choose a project type. In this instance, choose “Standalone Project”.
3. Click **Next>**to move to the next dialog.

**STEP 2**

Choose the required device, in this case PIC18F6527.When done, click **Next**.

**STEP 3**

From “Select Tool”, choose a connected hardware tool from all the options given and then click NEXT.

**STEP 4**

1. MPLAB REAL ICE in-circuit emulator is selected as tool.
2. “none” is selected for Plug-In board and **Next** is clicked.

**STEP 5**

Select the language tool, either a C compiler or assembler. Again, the coloured circle in front of the compiler name signifies the device support level. Select your tool and then click **Next.**

**STEP 6**

Select the project Name, Location and other project options. Select **Finish** tocomplete new project creation.

**STEP 7**

After writing the source code, the project is debugged onto the PIC microcontroller, using “REAL ICE” PIC KIT.

### 8.1.2 IDE DEXTOP

Once the project has been created, several panes are opened in the IDE.

* **File Pane-** A pane with four tabbed windows – *Projects, Files, Classes and Services* (not shown automatically) windows.
* **Navigation Pane-** A pane that displays information on the file or project selected. For a project, the project environment shows details about the project and for a file, symbols and variables as shown.
* **Editor Pane-** A pane for viewing and editing project files. The Start Page also is visible here.
* **Task Pane-** A pane that displays task output from building, debugging or running an application.

## 8.2 OSCILLATOR CONFIGURATION

### 8.2.1 OSCILLATOR TYPES

The PIC18F8722 family of devices can be operated inten different oscillator modes. The user can programthe configuration bits, FOSC3:FOSC0, in Configuration

Register 1H to select one of these ten modes:

1. LP Low-Power Crystal
2. XT Crystal/Resonator
3. HS High-Speed Crystal/Resonator
4. HSPLL High-Speed Crystal/Resonator with PLL enabled
5. RC External Resistor/Capacitor with FOSC/4 output on RA6
6. RCIO External Resistor/Capacitor with I/O on RA6
7. INTIO1 Internal Oscillator with FOSC/4 output on RA6 and I/O on RA7
8. INTIO2 Internal Oscillator with I/O on RA6and RA7
9. EC External Clock with FOSC/4 output
10. ECIO External Clock with I/O on RA6

*We are using INTIO mode particularly INTIO1 mode.*

### 8.2.2 INTIO MODES

Using the internal oscillator as the clock source eliminates the need for up to two external oscillator pins, which can then be used for digital I/O. Two distinct configurations are available:

* In INTIO1 mode, the OSC2 pin outputs FOSC/4, while OSC1 functions as RA7 (see Figure 2-8) for digital input and output.
* In INTIO2 mode, OSC1 functions as RA7 andOSC2 functions as RA6 (see Figure 2-9), both for digital input and output.



Fig. 18- INTIO1 oscillator mode

### 8.2.3 PLL IN INTOSC MODES

The 4x Phase Locked Loop (PLL) can be used with the internal oscillator block to produce faster device clock speeds than are normally possible with the internal oscillator sources. When enabled, the PLL produces a clock speed of 16 MHz or 32 MHz

Unlike HSPLL mode, the PLL is controlled through software. The control bit, PLLEN (OSCTUNE<6>), is used to enable or disable its operation.

The PLL is available when the device is configured to use the internal oscillator block as its primary clock source (FOSC3:FOSC0 = 1001 or 1000). Additionally, the PLL will only function when the selected output frequency is either 4 MHz or 8 MHz (OSCCON<6:4> = 111 or 110). If both of these conditions are not met, the PLL is disabled and the PLLEN bit remains clear (writes are ignored).



Fig. 19- Clock Diagram

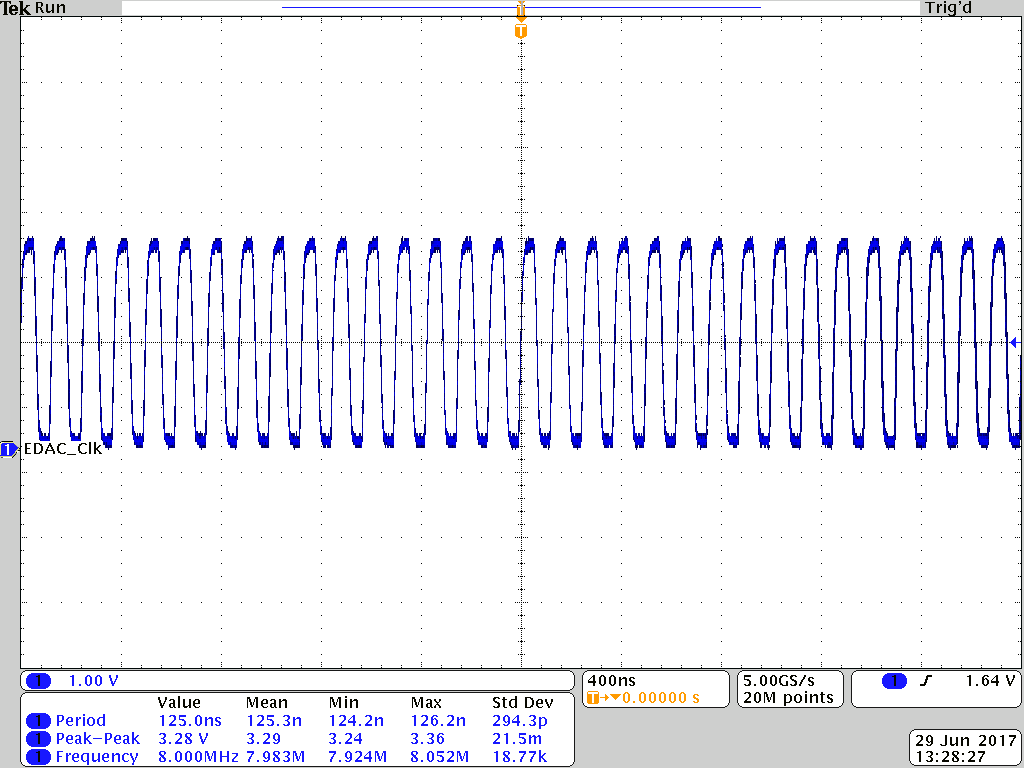


Fig. 20- Clock frequency going to the EDAC

Internal Clock frequency is 32 MHz and therefore Fosc/4 comes out to be 8 MHz i.e. clock going to the EDAC.

## 8.3 PWM

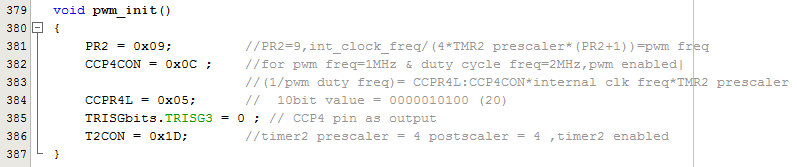


Fig. 21PWM code

## 8.4INTERRUPTS

### 8.4.1 INTRODUCTION –

There are two methods by which devices receive service from the microcontroller: interrupts and polling.

**Interrupt Method** – the device sends interrupts to microcontroller when it wants its service thereby stopping the microcontroller from whatever it is doing and runs the ISR(Interrupt Service Routine).

**Polling Method-** the microcontroller continuously monitors the status of given device and when the condition is met, it performs the service.

The PIC18F6527 family of devices 00have multiple interrupt sources and an interrupt priority feature that allows most interrupt sources to be assigned a high priority level or a low priority level.

High priority interrupt vector is at - 0008h

Low priority interrupt vector is at - 0018h.

High priority interrupt events will interrupt any low priority interrupts that may be in progress.

There are ten registers which are used to control interrupt operation. These registers are:

• RCON

• INTCON

• INTCON2

• INTCON3

• PIR1, PIR2, PIR3

• PIE1, PIE2, PIE3

• IPR1, IPR2, IPR3

### 8.4.2SOURCES OF INTERRUPTS IN PIC18 –

* Interrupts for all the timers.
* External Hardware interrupts. Pins RB0, RB1 and RB2 are for external hardware interrupts INT0, INT1 and INT2.
* Serial Communication’s USART interrupts, one for receive and one for transmit.
* PORTB – Change interrupt.
* ADC (analog to digital converter interrupt) interrupts.
* CCP (compare capture pulse-width-modulation) interrupt.

### 8.4.3 USING INTERRUPTS –

* **HIGH/LOW PRIORITY MODE** - The interrupt priority feature is enabled by setting the IPEN bit (RCON<7>). When interrupt priority is enabled, there are two bits which enable interrupts globally. Setting the GIEH bit (INTCON<7>) enables all interrupts that have the priority bit set (high priority). Setting the GIEL bit (INTCON<6>) enables all interrupts that have the priority bit cleared (low priority). When the interrupt flag enable bit and appropriate global interrupt enable bit are set, the interrupt will vector immediately to address 0008h or 0018h, depending on the priority bit setting. Individual interrupts can be disabled through their corresponding enable bits.

**COMPATIBILITY MODE** – When the IPEN bit is cleared (default state), the interrupt priority feature is disabled and interrupts are compatible with PIC micro mid-range devices. In Compatibility mode, the interrupt priority bits for each source have no effect. INTCON<6> is the PEIE bit, which enables/disables all peripheral interrupt sources. INTCON<7> is the GIE bit, which enables/disables all interrupt sources. All interrupts branch to address0008h in Compatibility mode.

* When an interrupt is responded to, the global interrupt enable bit is cleared to disable further interrupts. If the IPEN bit is cleared, this is the GIE bit. If interrupt priority levels are used, this will be either the GIEH or GIEL bit. High priority interrupt sources can interrupt a low priority interrupt. Low priority interrupts are not processed while high priority interrupts are in progress.
* The return address is pushed onto the stack and the PC is loaded with the interrupt vector address (0008h or 0018h). Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bits must be cleared in software before re-enabling interrupts to avoid recursive interrupts.

### 8.4.4 PIC18F6527 FAMILY INTERRUPT LOGIC

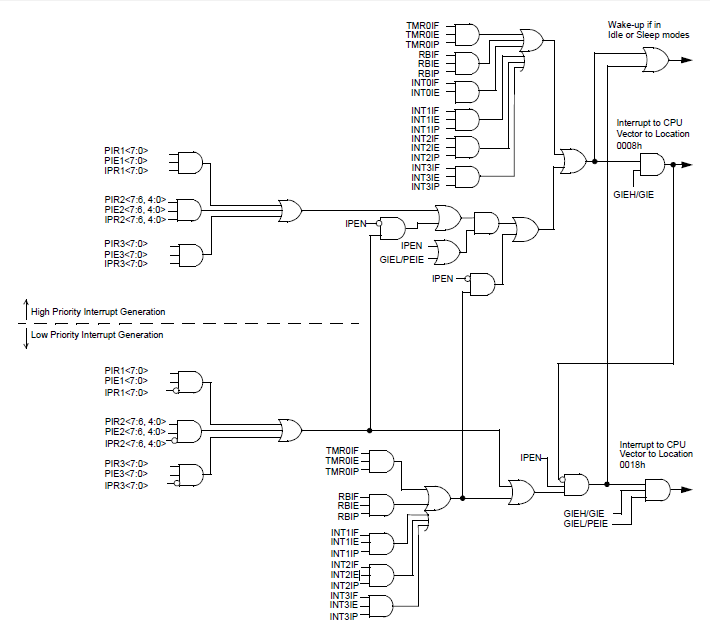


Fig. 22- Interrupt logic

### 8.4.5 THE CODE

### 8.4.5.1 INTERRUPT REGISTER INITIALISATION –

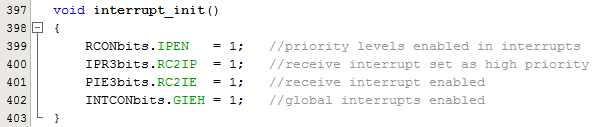
****

Fig. 23- Interrupt registers initialization

### 8.4.5.2 INTERRUPT AS HIGH PRIORITY –

Note: Only 8 bytes of location is set aside for high priority interrupts therefore code() function is called into it.

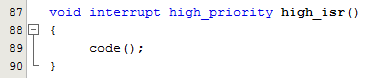
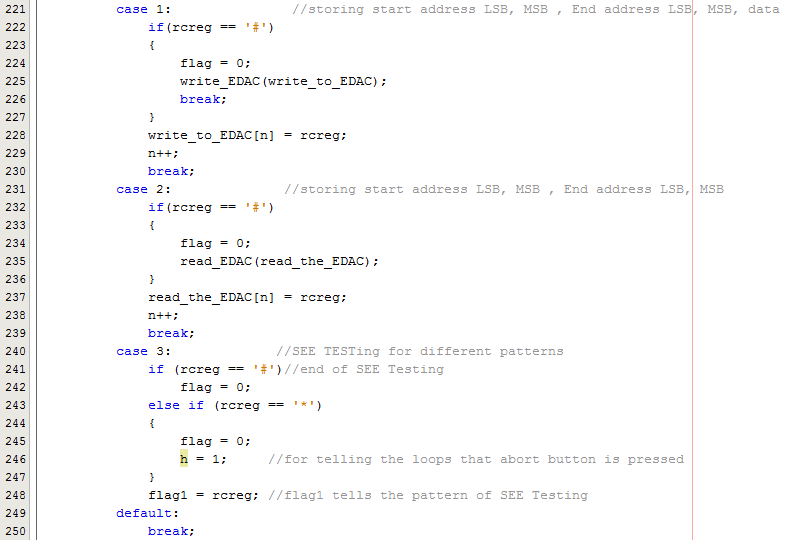
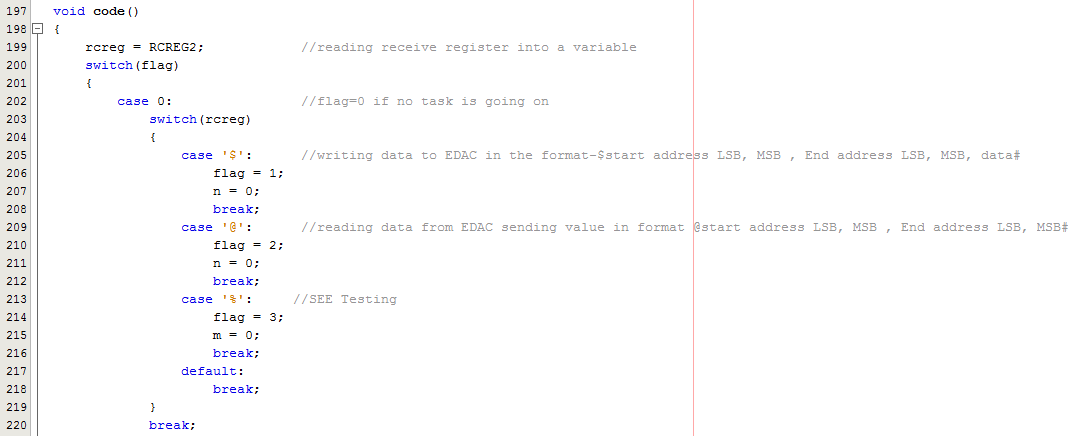
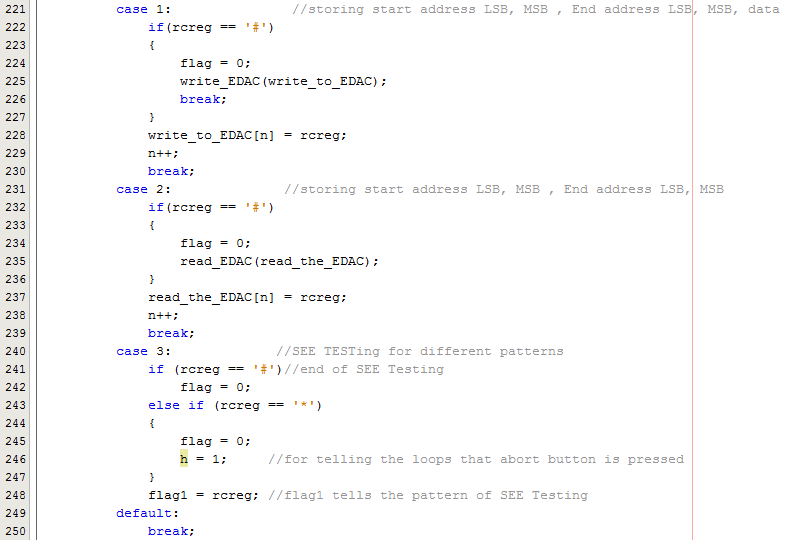


Fig. 24- Receive interrupt as high priority

#### Code () function

****

****

**Fig. 25-**Code function

## 8.5SERIAL COMMUNICATION

A universal asynchronous receiver/transmitter is a computer hardware device for synchronous serial communication in which the data format and transmission speeds are configurable.

The Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART) module is one of two serial I/O modules.

The EUSART can be configured in the following modes:

• Asynchronous (full duplex) with:

- Auto-Wake-up on Character Reception

- Auto-Baud Calibration

- 12-bit Break Character Transmission

• Synchronous – Master (half duplex) with Selectable Clock Polarity

• Synchronous – Slave (half duplex) with Selectable Clock Polarity

The pins of EUSART1 and EUSART2 are multiplexed with the functions of PORTC (RC6/TX1/CK1 and RC7/RX1/DT1) and PORTG (RG1/TX2/CK2 and RG2/RX2/DT2), respectively.

RG1/TX2/CK2 and RG2/RX2/DT2 pins – PIC18 has RX and TX pins specifically for transferring and receiving data serially. These pins are TTL compatible, therefore they require a line driver (here MAX232) to make the RS232 compatible.

The operation of each Enhanced USART module is controlled through three registers:

* Transmit Status and Control (TXSTAx)
* Receive Status and Control (RCSTAx)
* Baud Rate Control (BAUDCONx)

For EUSART2:

- bit SPEN (RCSTA2<7>) must be set (= 1)

- Bit TRISG<2> must be set (= 1)

- Bit TRISG<1> must be cleared (= 0) for Asynchronous and Synchronous Master modes

- Bit TRISC<6> must be set (= 1) for Synchronous Slave mode (slave mode not used here)

-TXSTA2 is loaded with 0x24 indicating asynchronous mode with 8-bit data frame, high baud rate, and transmit enabled.

-RCSTA2 is loaded with 0x90, to enable the continuous receive in addition to the 8-bit data size option.

-SPBERG2 is loaded with 0x08 for 115200 baud rate (since, SYNC=0, BRGH=1, BRG16=1 and Fosc is 4MHz)

-SPBERGH2 is 0x00

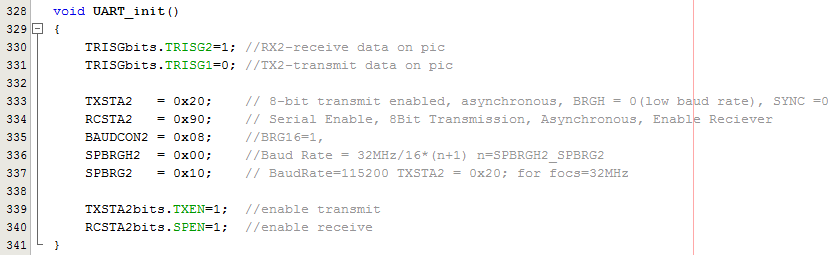
****

Fig. 26- USART registers initialization

#### Transfer Function



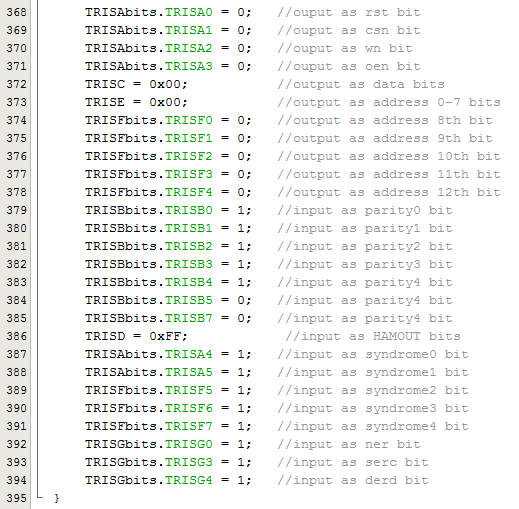
Fig. 27- USART transfer function

## 8.6 PORT INITIALIZATION

* Made all pins of PORT A digital by setting ADCON1 to 0x0F as default is analog input pins.
* Then cleared all the latches.



Fig. 28- Clearing port latches

* Initialized the various I/O ports as input or output given according to hardware pins in ANNEXURE Section. ****

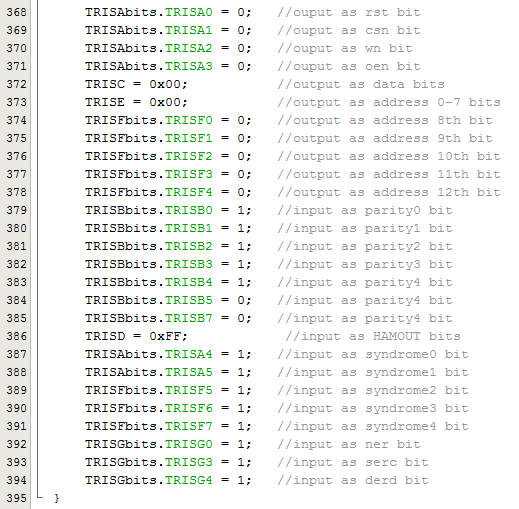


Fig. 29- Setting ports as I/O

## 8.7 READ EDAC FUNCTION

This function is used for reading the output of EDAC. ADDRESS range is given as input and it reads HAMOUT bits, SYNDROME bits, Ner-Serc-Derd bits and sends the same along with current address (4 Bytes) to serial port.

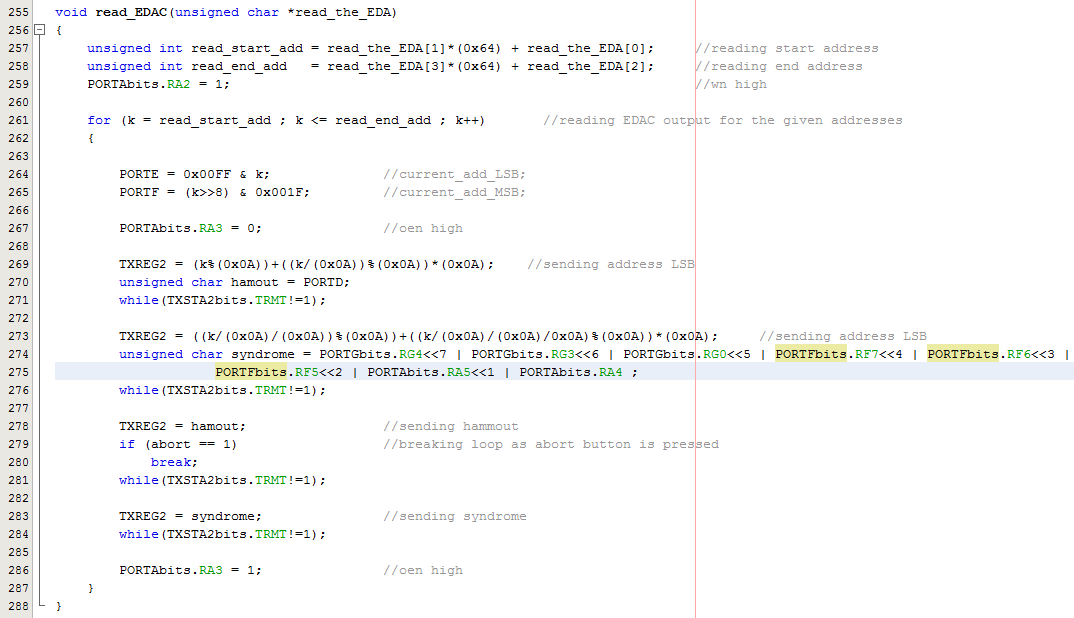
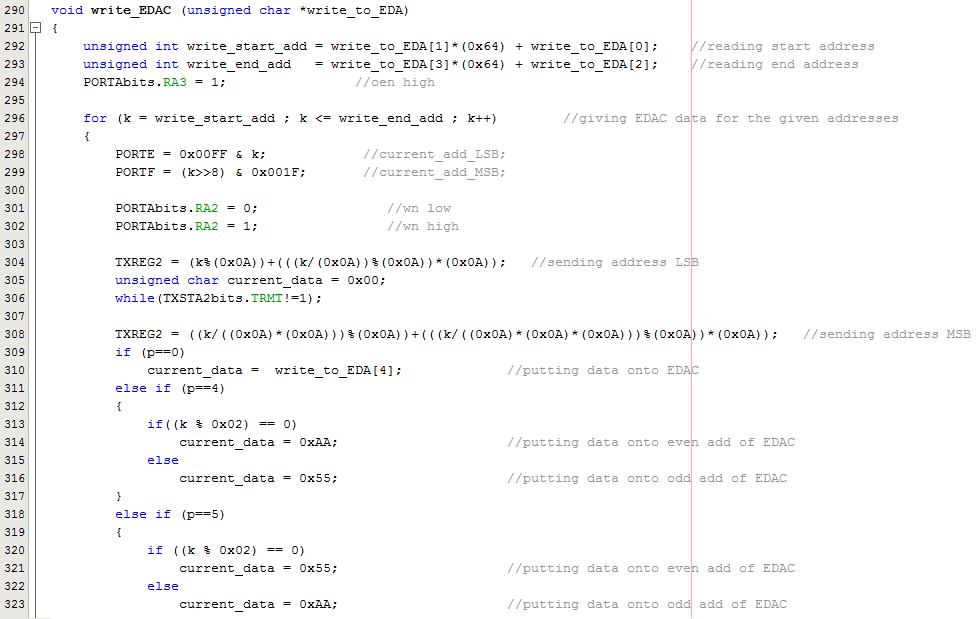


Fig. 30- Read EDAC function

## 8.8 WRITE EDACFUNCTION

This function is used for writing data to EDAC to corresponding address. The DATA and ADDRESS range is given as input and its transfers Data bits, Parity bits along with current address (4 Bytes) through serial port.



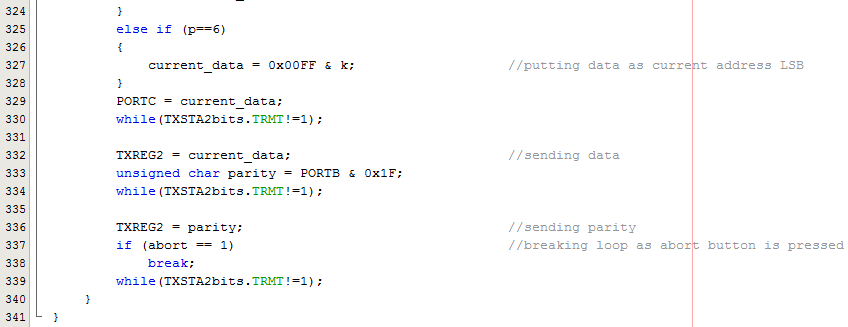
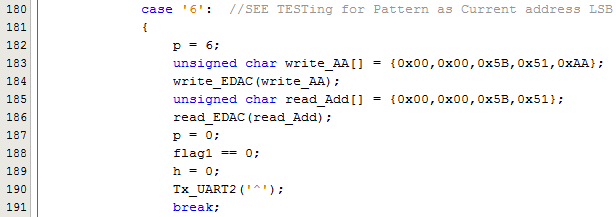
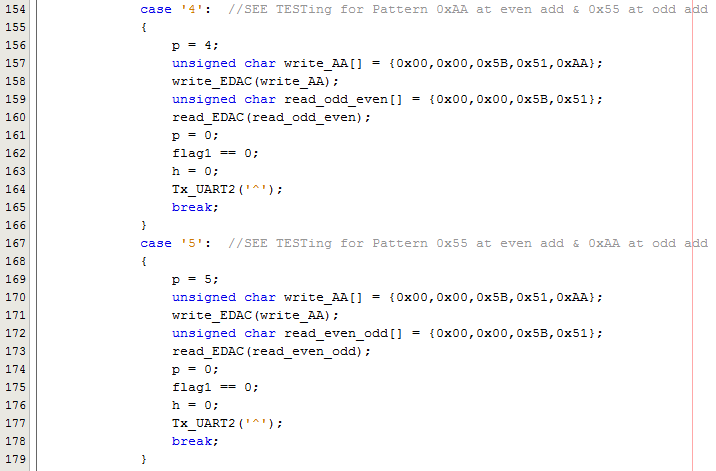
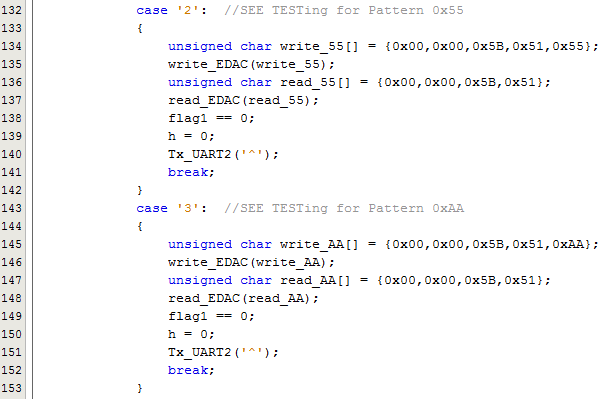
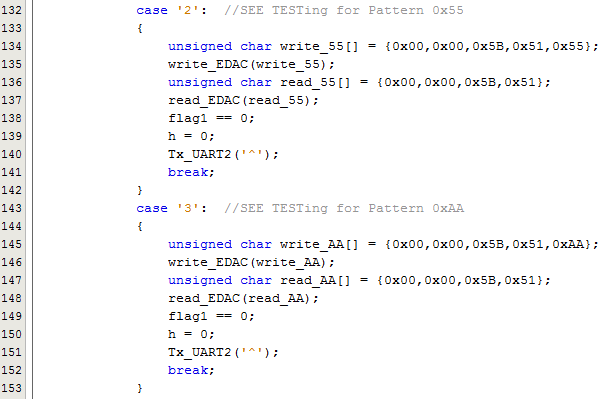
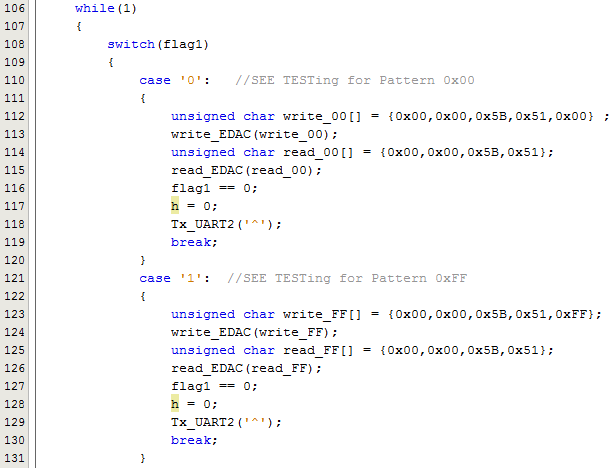
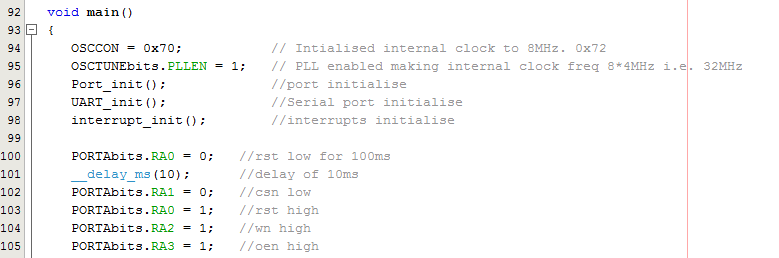


Fig. 31- Write EDAC function

## 8.9MAIN FUNCTION

****

**Fig. 32-**Main function

## 8.10CONTROL SIGNALS TO EDAC

* WN-Write Enable
* OEN-Output Enable
* RST-Reset
* CSN-chip Enable

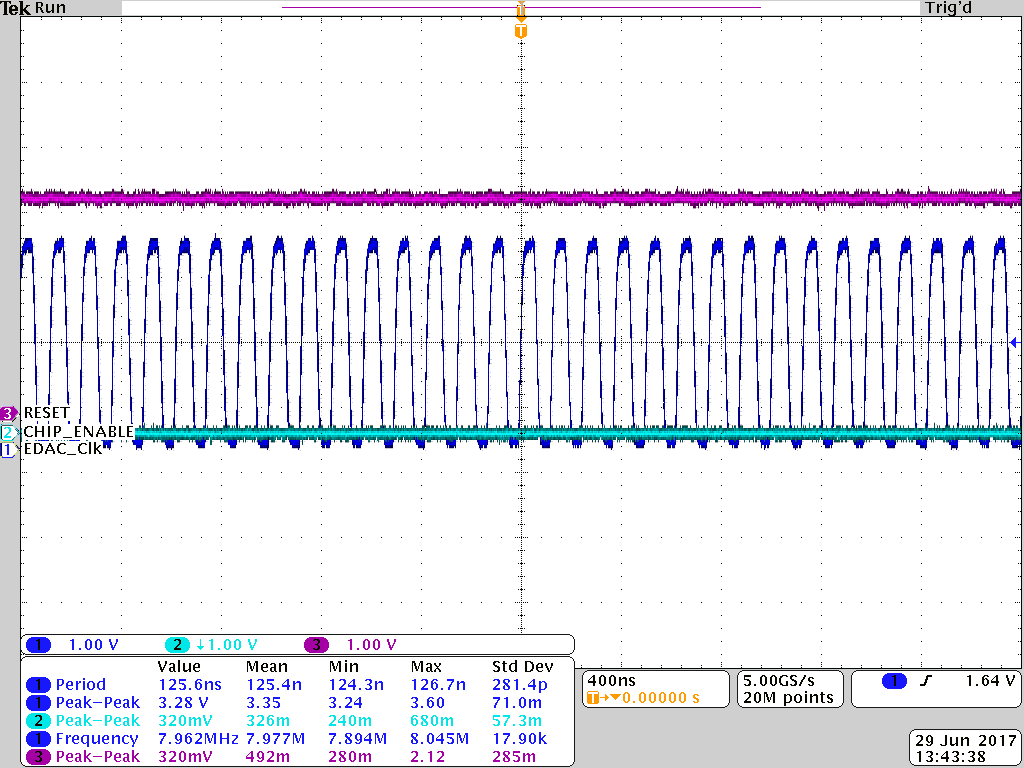


Fig. 33- Default status of reset and chip enable signals



Fig. 34- Default status of write enable and output enable signals

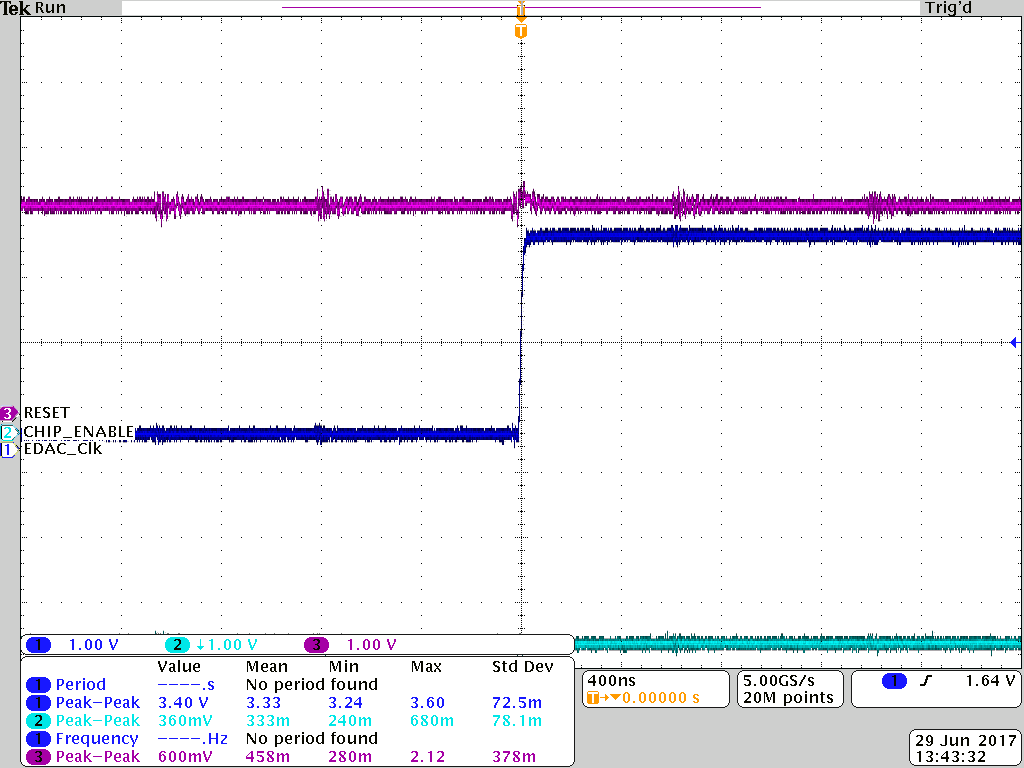


Fig. 35- Reset and chip enable signals during time of burning of PIC code

### 8.10.1 WRITE TIMING DIAGRAM



Fig. 36- Write Enable control signal while writing data into memory. Output enable is always high.

### 8.10.2 READ TIMING DIAGRAM

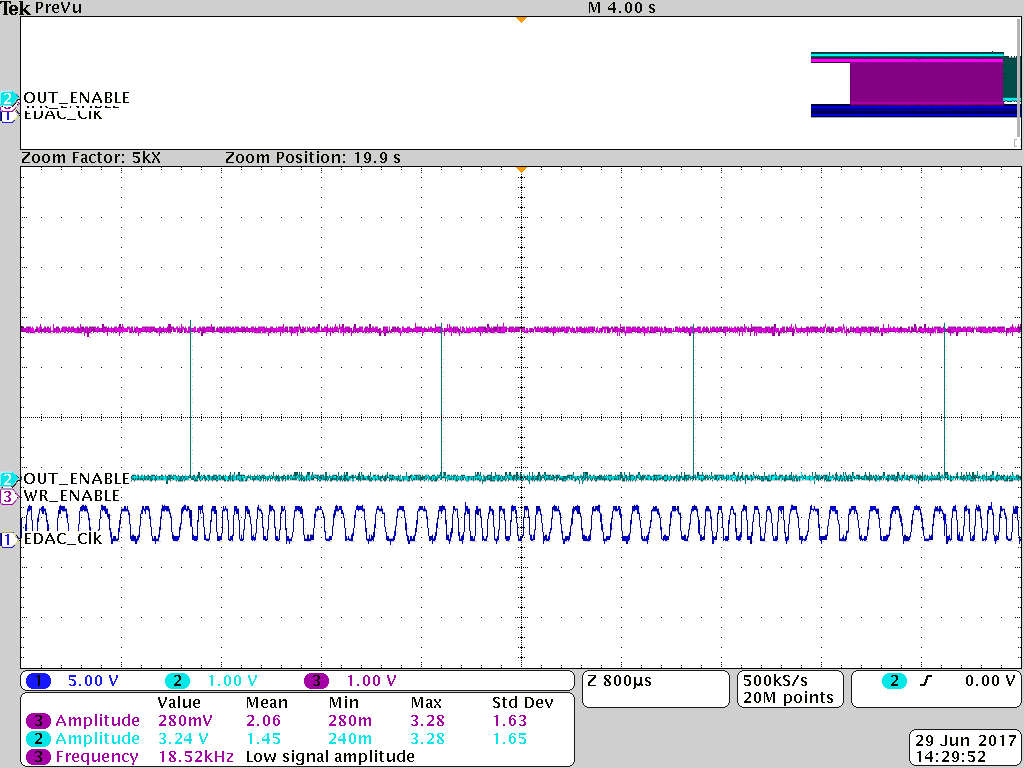


Fig. 37- Output Enable control signal while reading data from memory. Write enable is always high.

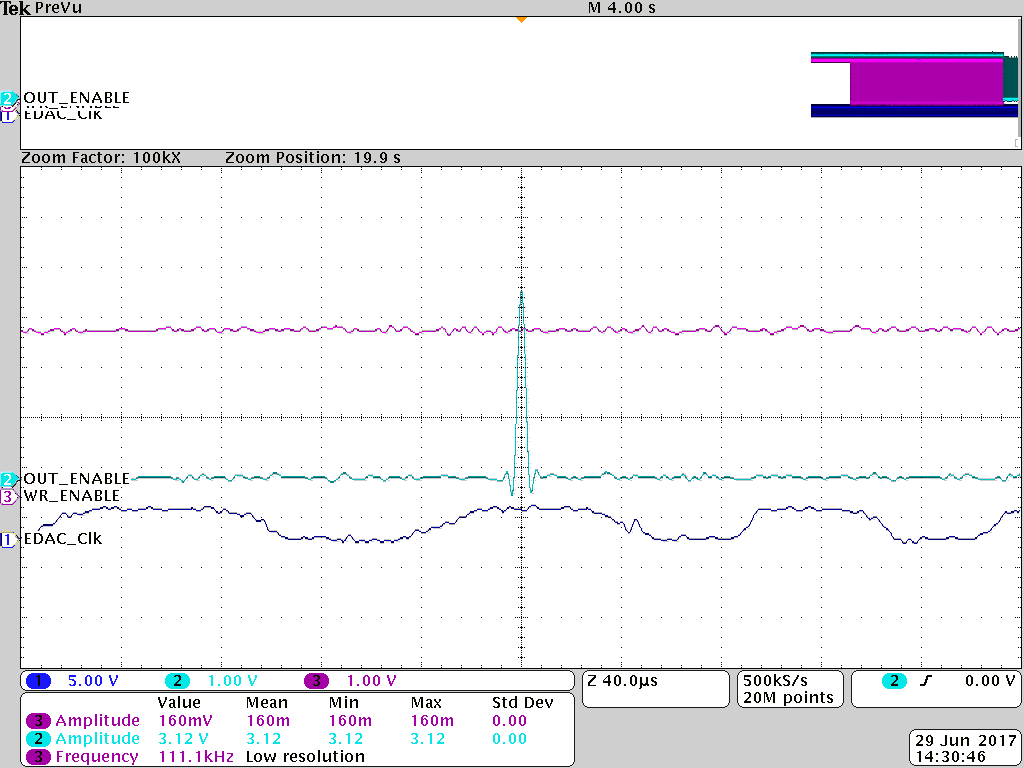
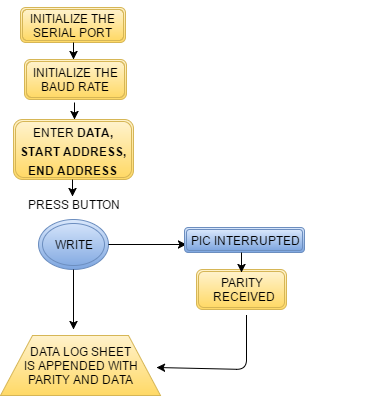


Fig. 38- Zoomed in view of the output enable control sign.

## 8.11 WRITE CYCLE

#### At frontend



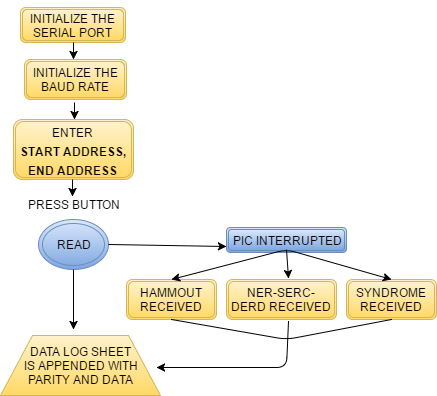
Block 1- 1 Write Cycle at frontend

#### At backend

**Block 2-**Write Cycle at backend

## 8.12 READ CYCLE

#### At frontend



Block 3- Read Cycle at frontend

#### At backend

Block 4- Read Cycle at backend

## 8.13 SEE TESTING CYCLE

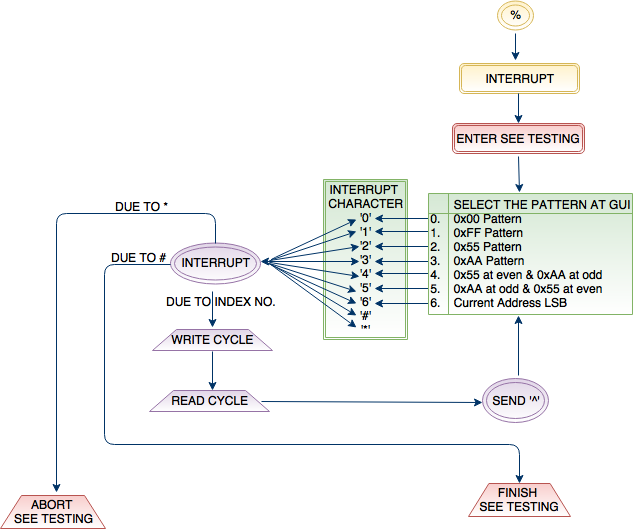


Fig. 39- SEE Testing Cycle

# CHAPTER 9

# GUI

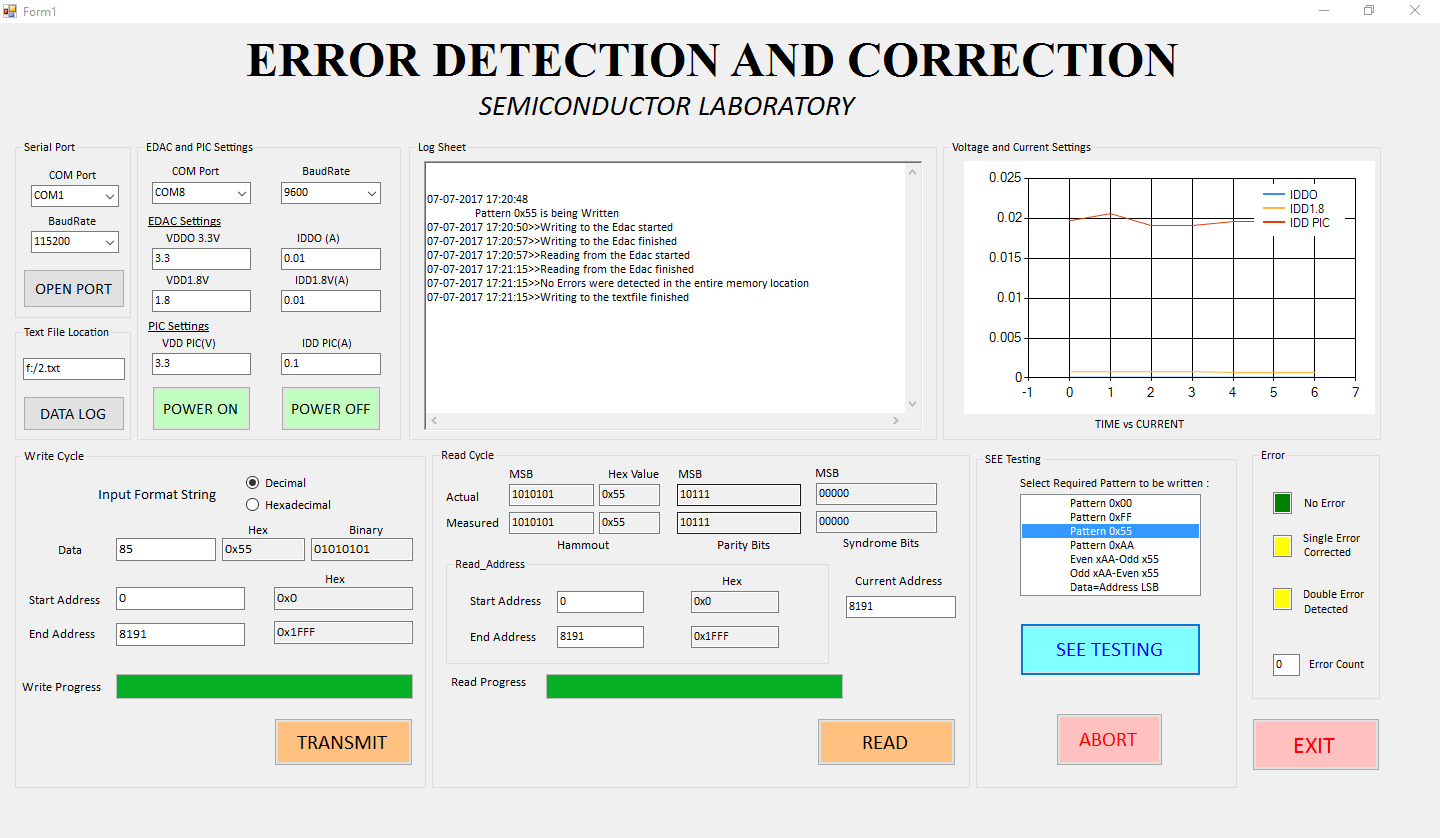
## 8.1 INTRODUCTION

The graphical user interface (GUI), is a type of user interface that allows users to interact with electronic devices through graphical icons and visual indicators such as secondary notation, instead of text-based user interfaces, typed command labels or text navigation. GUIs were introduced in reaction to the command-line interfaces (CLIs), which require commands to be typed on a computer keyboard.

The actions in a GUI are usually performed through direct manipulation of the graphical elements. Beyond computers, GUIs are used in many handheld mobile devices such as MP3 players, portable media players, gaming devices, Smart phones and smaller household, office and industrial controls.

The GUI for the EDAC Serial Communication is built on Microsoft Visual Studio along with C# .NET framework. //rephrase the sentence above//. The two basic functions at the front end are to read and write data onto the EDAC through PIC controller using the serial ports available.

## 8.2 GUI WINDOW



## 8.3 SERIAL PORT INITIALIZATION

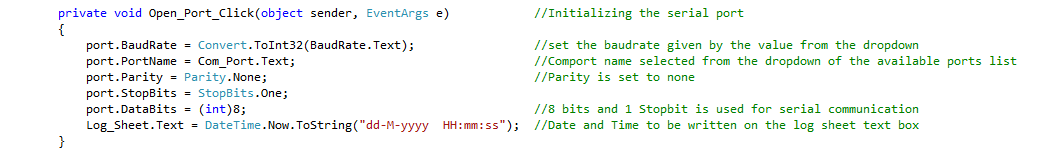


Fig. 40- Initialization of the serial port

## 8.4 WRITE CYCLE

## 

## Block 5- Write cycle flowchart

During the write cycle, the data and the addresses in which the data is to be written is sent to the PIC microcontroller in a specific format. The Flowchart above summaries the write cycle process.

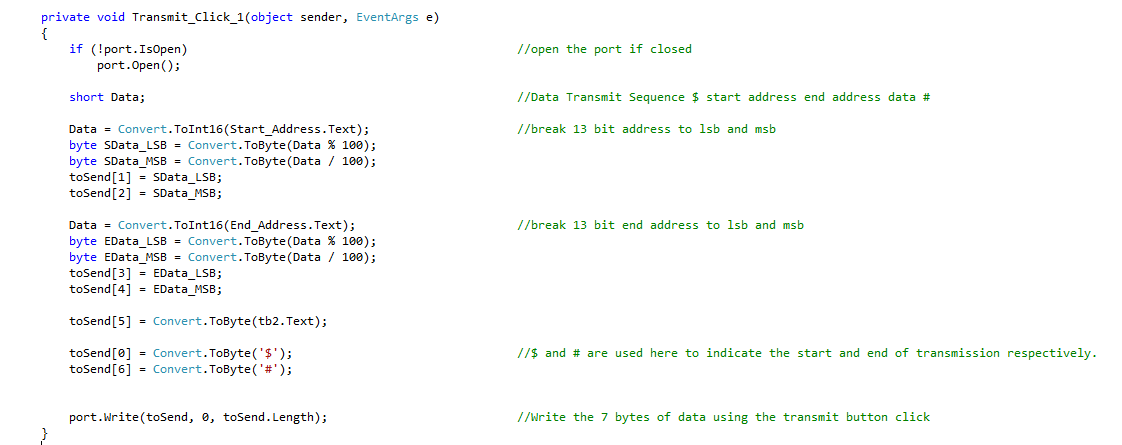
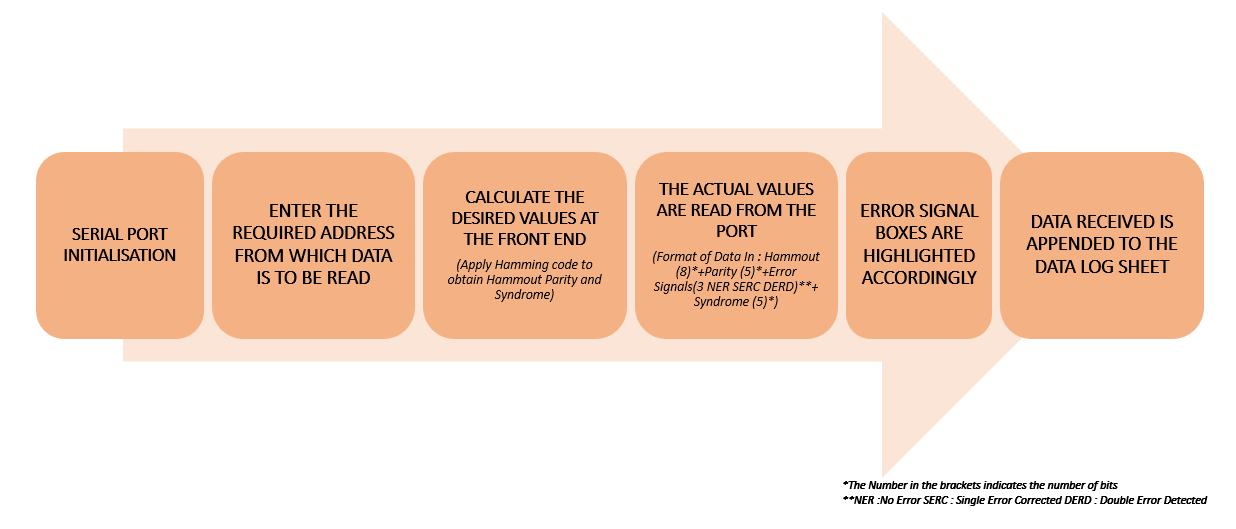


Fig. 41-Write cycle in which address is broken down into 2 bytes

Since, Serial communication happens in byte size, i.e., 8 bits of data can be transferred at once, the start and end address being 13bit is broken down into 8 bits and 5 bits respectively and transmitted.

## 8.5 READ CYCLE



Block 6- read cycle flowchart

During the read cycle, the address from which the data is to be read is sent to the PIC microcontroller in a specific format. The Parity and the Syndrome bits are calculated using the hamming code (bitwise XOR) logic as a reference to the values which will be obtained from the EDAC through PIC. Hammout, Syndrome and other error signals are received accordingly. The Flowchart above summaries the read cycle process.



Fig. 42- Write cycle code

## 8.6 HAMMING CODE CALCULATION USING C#

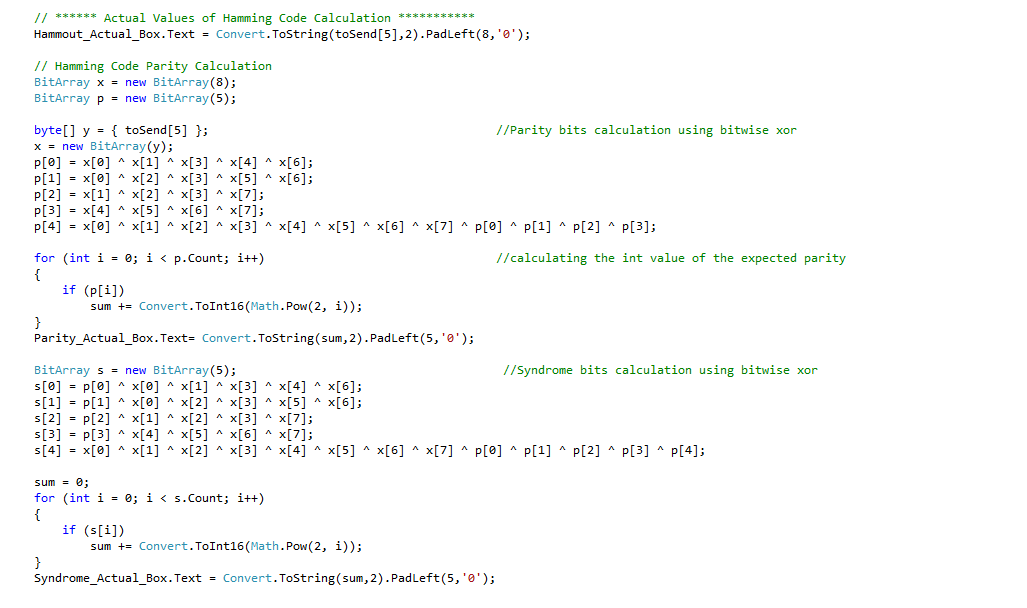


Fig. 43- Hamming code calculation code using bitwise xor

## 8.7 CREATING A TEXT FILE

All the calculations performed by the EDAC need to be saved in some format to verify the consistency of the device and also maintain a database for future reference. A text file is created using FileStream Class.

A file is a collection of data stored in a disk with a specific name and a directory path. When a file is opened for reading or writing, it becomes a stream. The stream is basically the sequence of bytes passing through the communication path. There are two main streams: the input stream and the output stream. The input stream is used for reading data from file (read operation) and the output stream is used for writing into the file (write operation).

The FileStream class in the System.IO namespace helps in reading from, writing to and closing files. This class derives from the abstract class Stream.

You need to create a FileStream object to create a new file or open an existing file. The syntax for creating a FileStream object is as follows:

FileStream <object\_name> = new FileStream( <file\_name>,

<FileMode Enumerator>, <FileAccess Enumerator>, <FileShare Enumerator>);

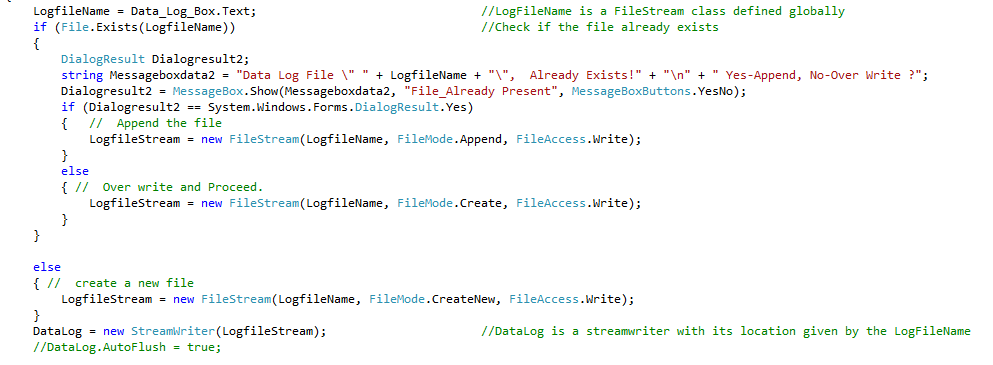


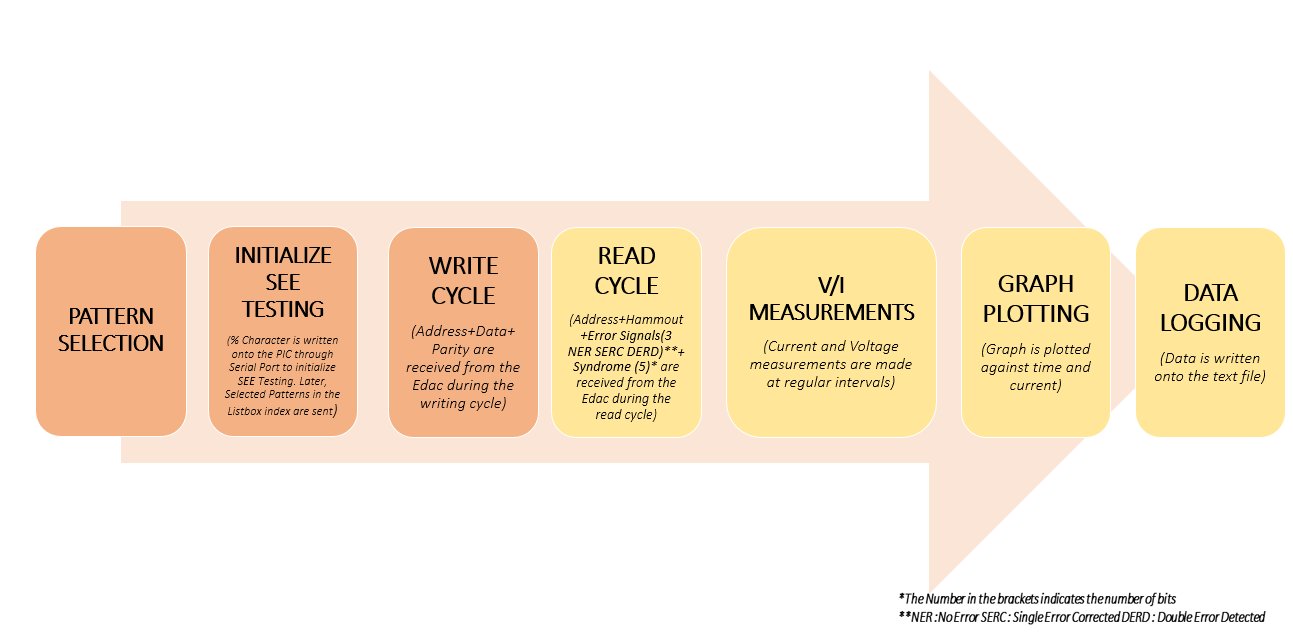
Fig. 44- creating a textfile

#### The StreamWriter Class

The StreamReader and StreamWriter classes are used for reading from and writing data to text files. These classes inherit from the abstract base class Stream, which supports reading and writing bytes into a file stream. The StreamWriter class inherits from the abstract class TextWriter that represents a writer, which can write a series of character.

## 8.8 SEE TESTING

Predefined Patterns are listed in a Listbox which are to be written to the entire memory of the EDAC. On selecting the required pattern, the data associated with it is written on the entire chunk of memory. The process is summarized in the flowchart mentioned below. The last 4 blocks in yellow are the processes which happens simulateneously. Data is read from the serial port in a write cycle and Hamming Code is calculated at the front for verifying, Current and Voltage measurements are taken periodically and a graph is plotted against Time and Current. All the information is logged into the text file simultaneously.



Block 7- SEE Testing Flowchart

The % character is sent to the PIC to initiate SEE testing. The index of the listbox items is sent to perform read and write operation of that pattern selected in the for loop. On successful completion, # character is sent indicating that the all the patterns selected are finished.

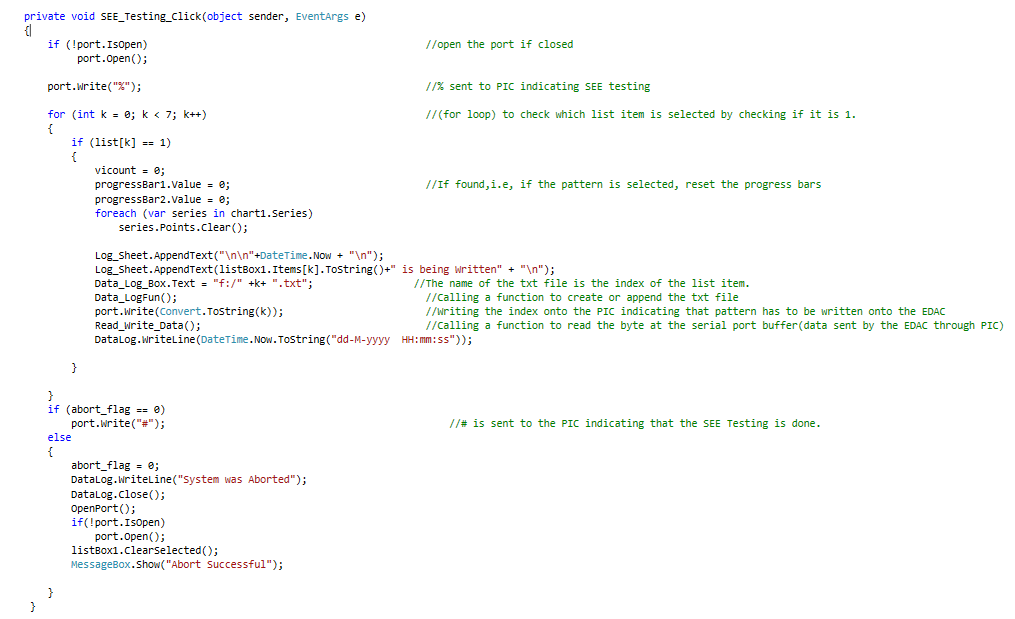


Fig. 45- SEE Testing Code

# CHAPTER 10

# HAMEG POWER SUPPLY CONTROL

## 10.1 INTRODUCTION

For remote control, RS-232 / USB (standard interface HO720), Ethernet / USB (optional interface HO730) or GPIB (optional interface HO740) can be used. The optional interfaces replace the RS-232 / USB HO720 interface module on the rear panel. SCPI (Standard Commands for Programmable Instruments) SCPI commands - messages - used for remote control. Commands that are not taken from the SCPI standard follow the SCPI syntax rules.



Fig. 46- HMP2030 Power Supply

### 10.1.1RS-232 Interface

If you use classic RS-232 you do not need any driver. In order to set the interface parameter at the HMP, please press the button MENU at the front panel and choose the menu item INTERFACE. Make sure the RS 232 interface is chosen. The menu item SETTINGS opens a menu where you can set and save all parameter for the RS-232 communication. Setting of the RS-232 must fit the setting of the corresponding PC COM port. In general, there exist two options for the RS-232 communication: with or without interface handshake. If you are working without handshake you have to integrate appropriate delays between the commands to make sure that all commands are executed correctly (approx. 50ms to 100ms). Without handshake you can have the problem that the interface buffer can overflow (e.g. missing commands). If you are working with interface handshake (set on both sides, HMP and PC) you don‘t need to integrate delays.

### 10.1.2 USB Interface

If you are using USB, you need to install a USB driver which is available on the Rohde & Schwarz Website. The HMP USB interface has to be chosen in the MENU and does not need any setting. The interface is equipped with a Type A USB female connector. For direct connection with a host controller or an indirect connection via a USB hub, a USB cable is required, equipped with Type B male connector one end and a Type A male connector at the other.



Fig. 47-From Left to Right: Type A, Type B

## 10.2 Switching to Remote Control

When you switch on the instrument, it is always in manual operation state (local state) and can be operated via the front panel. When you send a command via PC, it will be received and executed by the instrument. The display remains on, manual operation via the front panel is always possible.

### 10.3.1 Commands

Commands (program messages) are messages which the controller sends to the instrument. They operate the instrument functions and request information. The commands are subdivided according to two criteria:

According to the instrument effect:

• Setting commands cause instrument settings such as a reset of the instrument or setting the frequency.

• Queries cause data to be provided for remote control, e.g. for identification of the instrument or polling a parameter value. Queries are formed by appending a question mark to the command header.

### 10.3.2 SCPI Command Structure

SCPI commands consist of a so-called header and, in most cases, one or more parameters. The header and the parameters are separated by a white space. The headers may consist of several mnemonics (keywords). Queries are formed by appending a question mark directly to the header. The commands can be either device-specific or device-independent (common commands). Common and device-specific commands differ in their syntax.

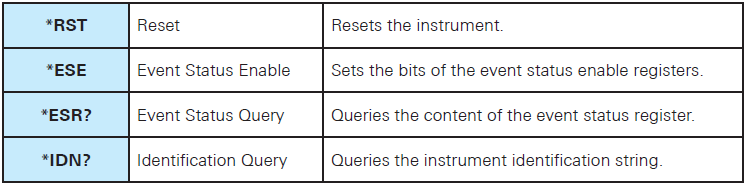


Table 4- Examples of Common Commands

#### Long and short form

The mnemonics feature a long form and a short form. The short form is marked by upper case letters; the long form corresponds to the complete word. Either the short form or the long form can be entered; other abbreviations are not permitted.

Example: MEASure:CURRent? Is equivalent to MEAS:CURR?

#### SCPI Parameters

Many commands are supplemented by a parameter or a list of parameters. The parameters must be separated from the header by a white space (ASCII code 0 to 9, 11 to 32 decimal, e.g. blank). Allowed parameters are:

• Numeric values

• Special numeric values

• Boolean parameters

• Text

• Character strings

• Block data

## 10.4 Common Commands

Common commands are described in the IEEE 488.2 (IEC 625-2) standard. These commands have the same effect and are employed in the same way on different devices. The headers of these commands consist of “\*“followed by three letters. Many common commands are related to the Status Reporting System.

#### Examples:

1. \*IDN?

IDeNtification

Returns the instrument identification string.

Return values:

<ID> HAMEG,‹device type›,‹serial number›,‹firmwareversion›

Example: HAMEG,HMP4040,055310003,HW50020001/SW2.41

Usage: Query only

1. \*RST

ReSeT

Sets the instrument to a defined default status. The default settings are indicated in the description

of commands.

Usage: Setting only

1. INSTrument[:SELect]?

Queries the channel selection.

Return values:

e.g. OUTP1 (= channel CH1)

Example:

INST OUT1

INST?, Response: OUTP1

1. [SOURce:]VOLTage[:LEVel][:IMMediate][:AMPLitude] {UP I DOWN}

Increases resp. decreases the voltage value of the selected channel. The voltage step size will be

defined with the VOLT:STEP command.

Example:

INST OUT1

VOLT:STEP 4

VOLT UP (= channel 1 will be set to 4.000V)

1. MEASure[:SCALar]:CURRent [:DC]?

Returns the measured current value of the previous selected channel.

Return values e.g. 1.0000

## 10.5 SNIPPETS FROM THE CODE

#### SERIAL PORT INITIALISATION:

#### SETTING THE VOLTAGE AND CURRENT VALUES FOR A SPECIFIC CHANNEL

#### MEASURING THE VOLTAGE AND CURRENT VALUES

# CHAPTER 11

# EDAC OUTPUT

The various patterns if SEE Testing were tested and data pins and hammout pins were read on the Oscilloscope.

## 10.1 Pattern 1 – writing 0x00 in all memory locations

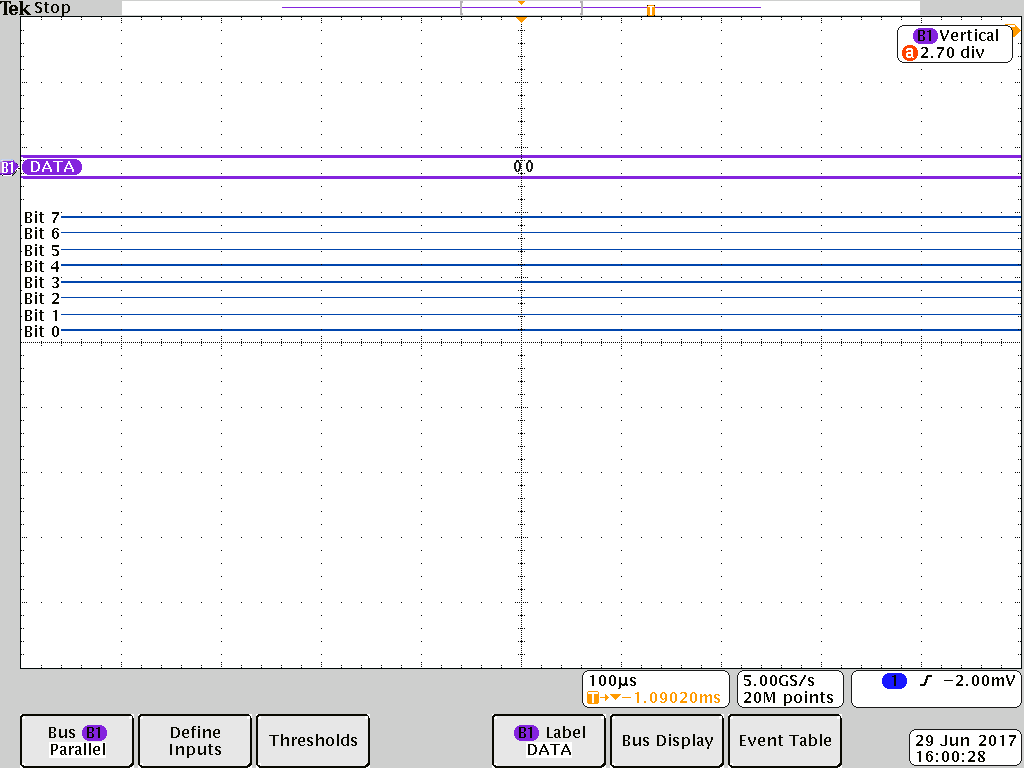


Fig. 48- Data comes out to be 0x00

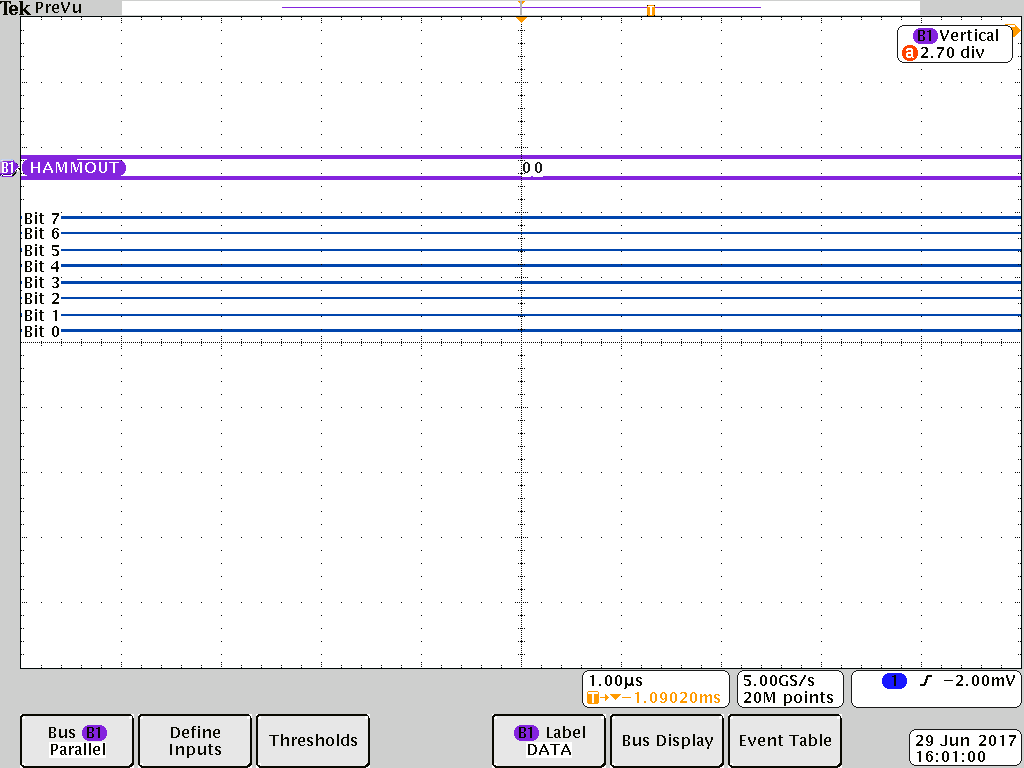
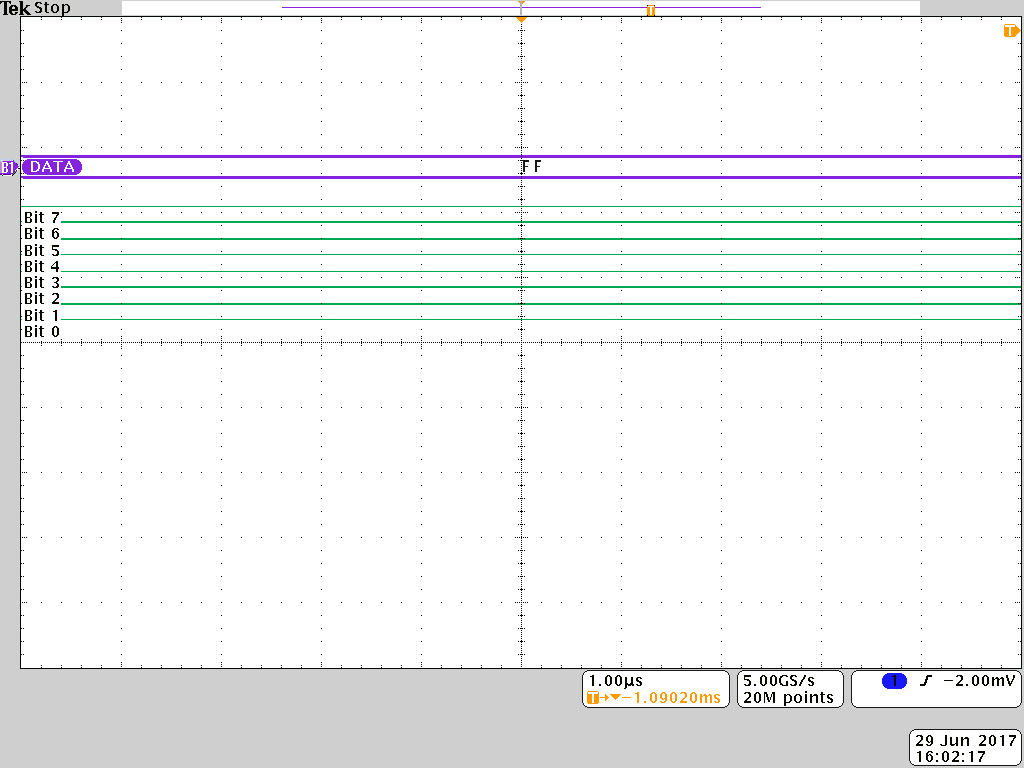


Fig. 49- Hammout also comes out same as Data i.e. 0x00

## 10.2 Pattern 2 – writing 0xFF in all memory locations

****

**Fig. 50-**Data comes out to be 0xFF

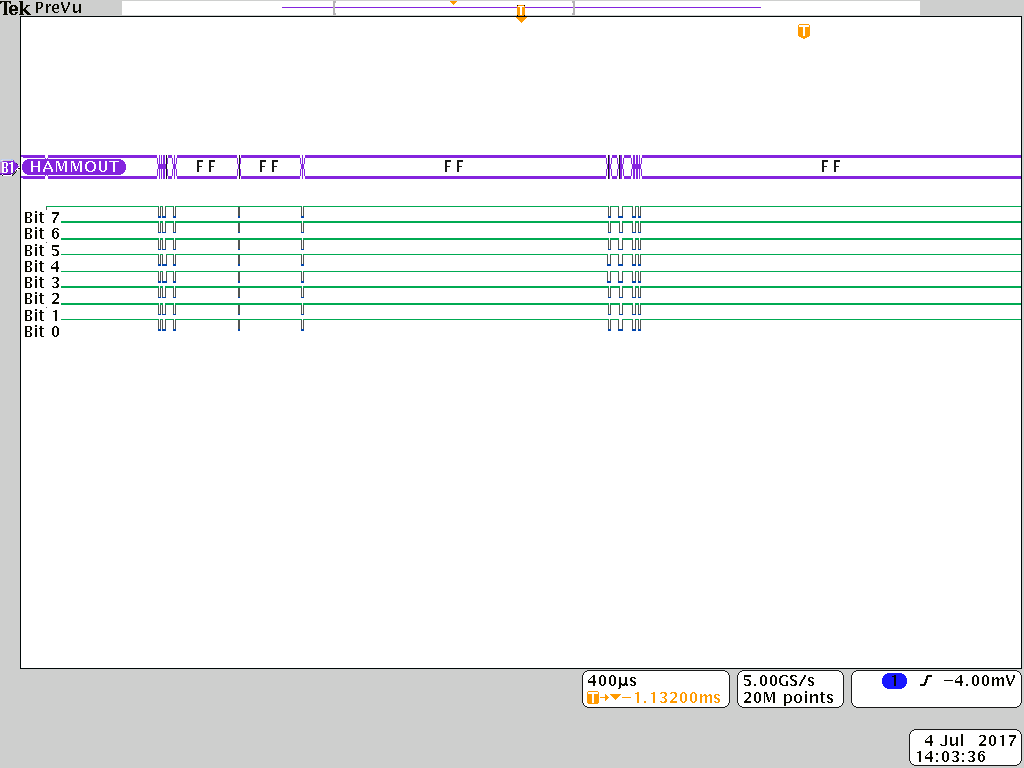


Fig. 51-Hammout also comes out same as Data i.e. 0xFF

## 10.3 Pattern 3 – writing 0x55 in all memory locations

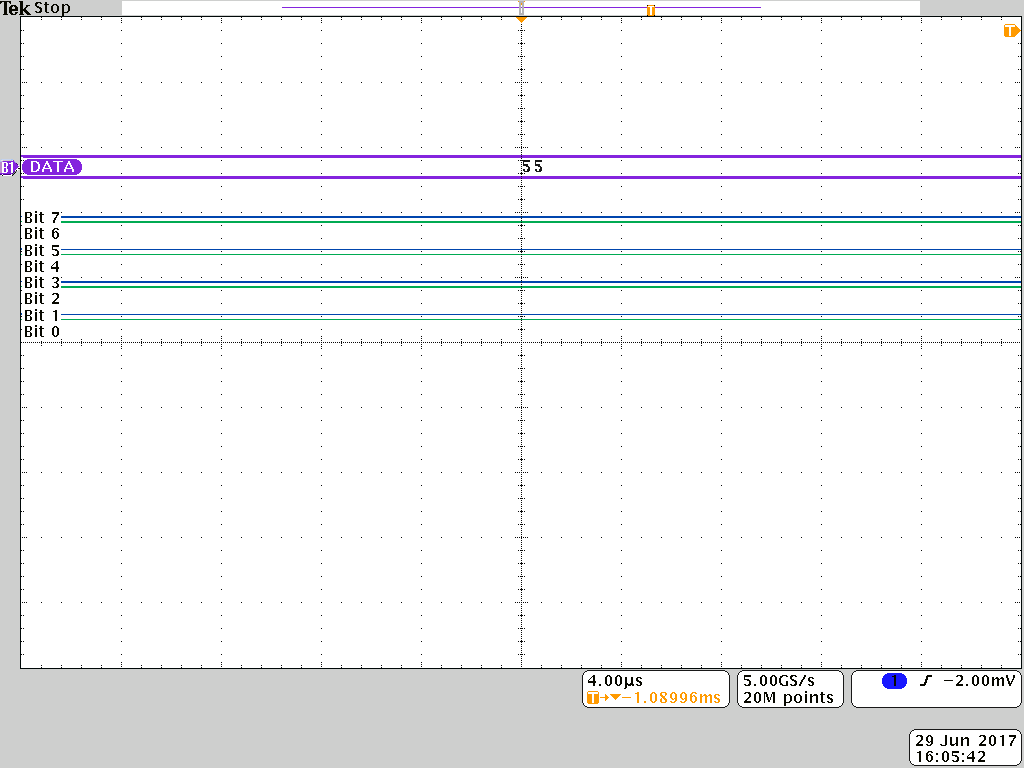


Fig. 52- Data comes out to be 0x55

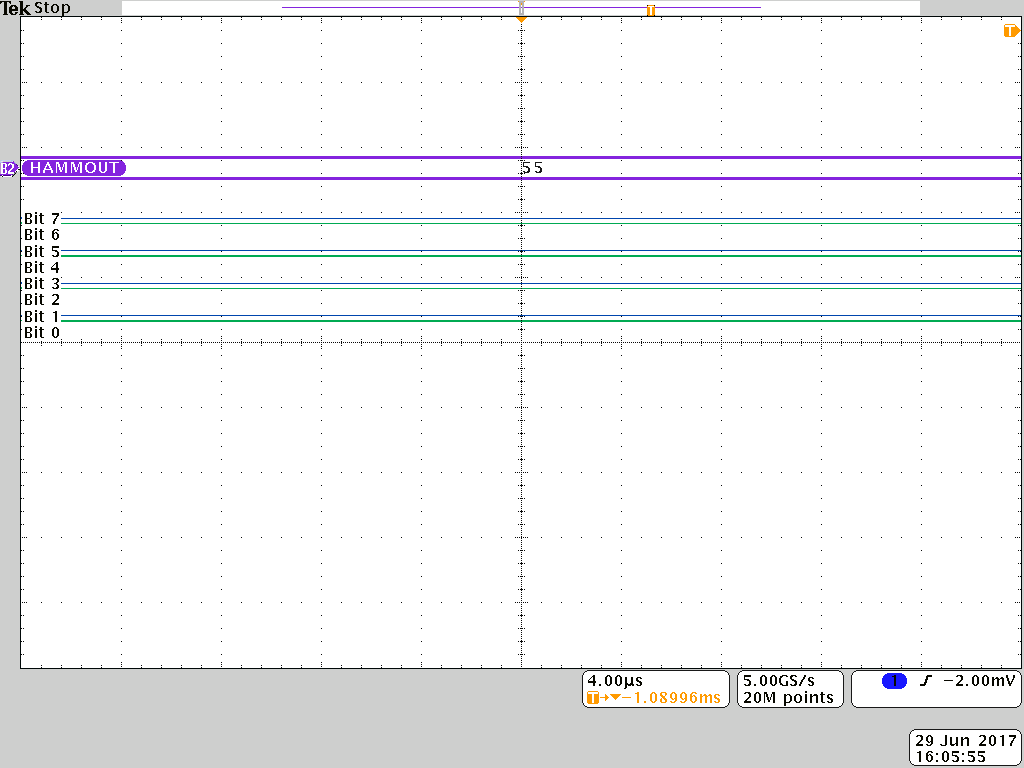


Fig. 53- Hammout also comes out same as Data i.e. 0x55

## 10.4 Pattern 4 – writing 0xAA in all memory locations

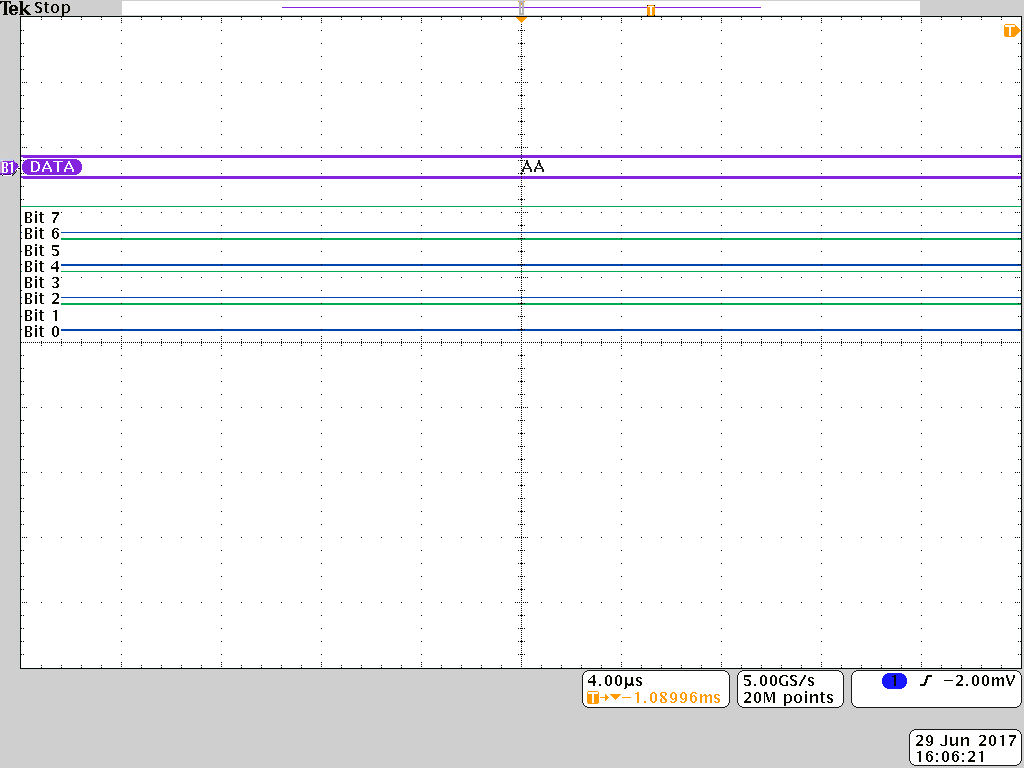


Fig. 54-Data comes out to be 0xAA

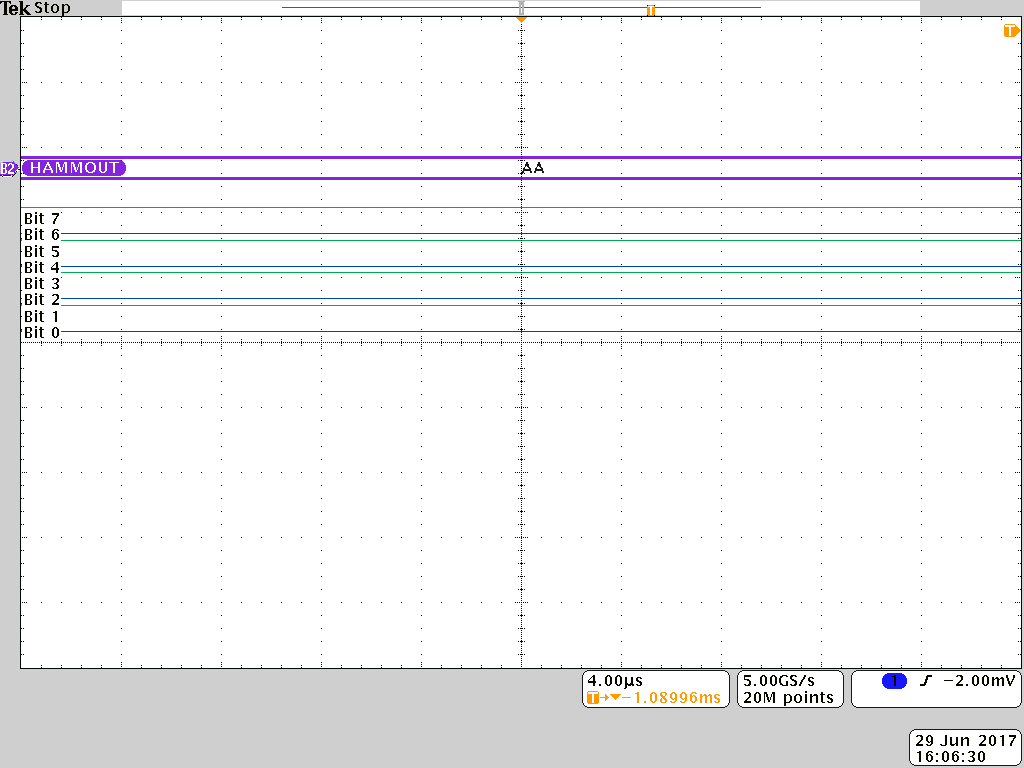


Fig. 55-Hammout also comes out same as Data i.e 0xAA

## 10.5 Pattern 5 – writing 0x55 in odd and 0xAA in even memory locations

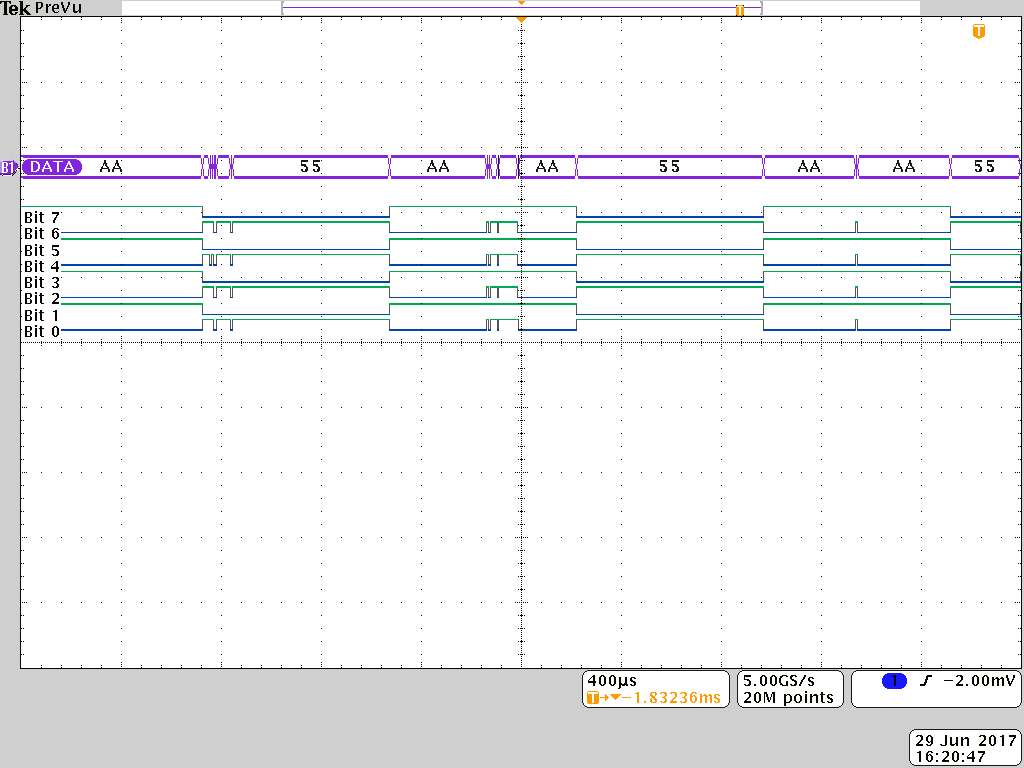


Fig. 56-Data is 0xAA in even locations and 0x55 in odd locations.

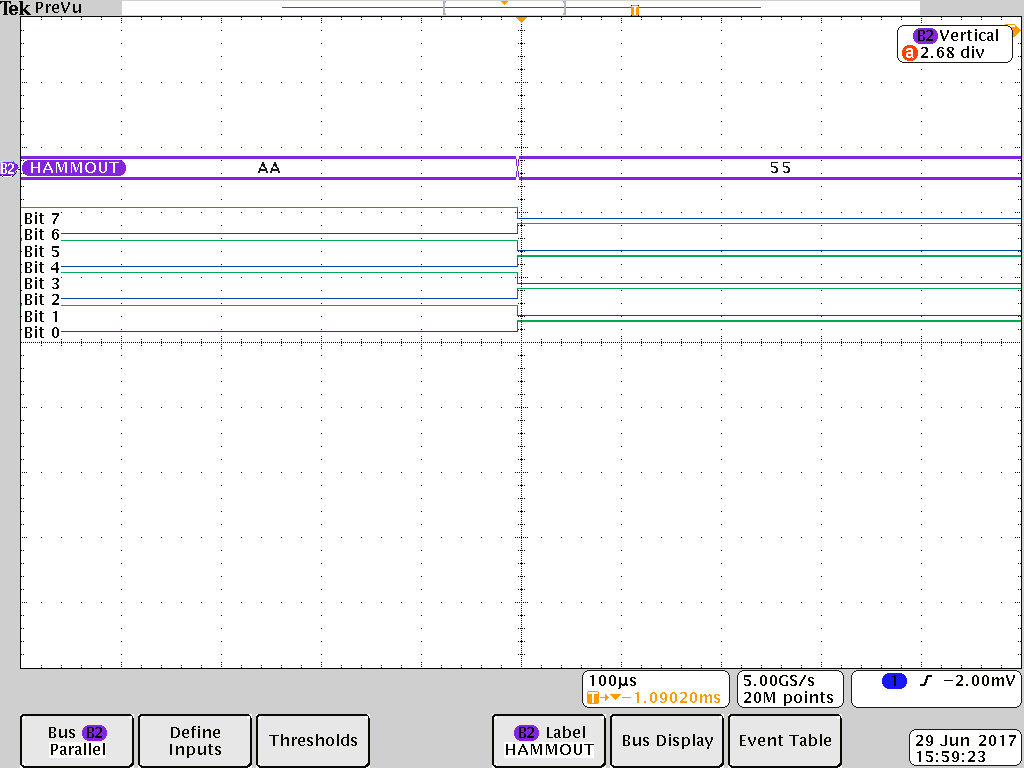


Fig. 57-Hammout is same as data i.e. 0xAA in even locations and 0x55 in odd locations.

## 10.6 Pattern 6 – writing 0x55 in even and 0xAA in odd memory locations

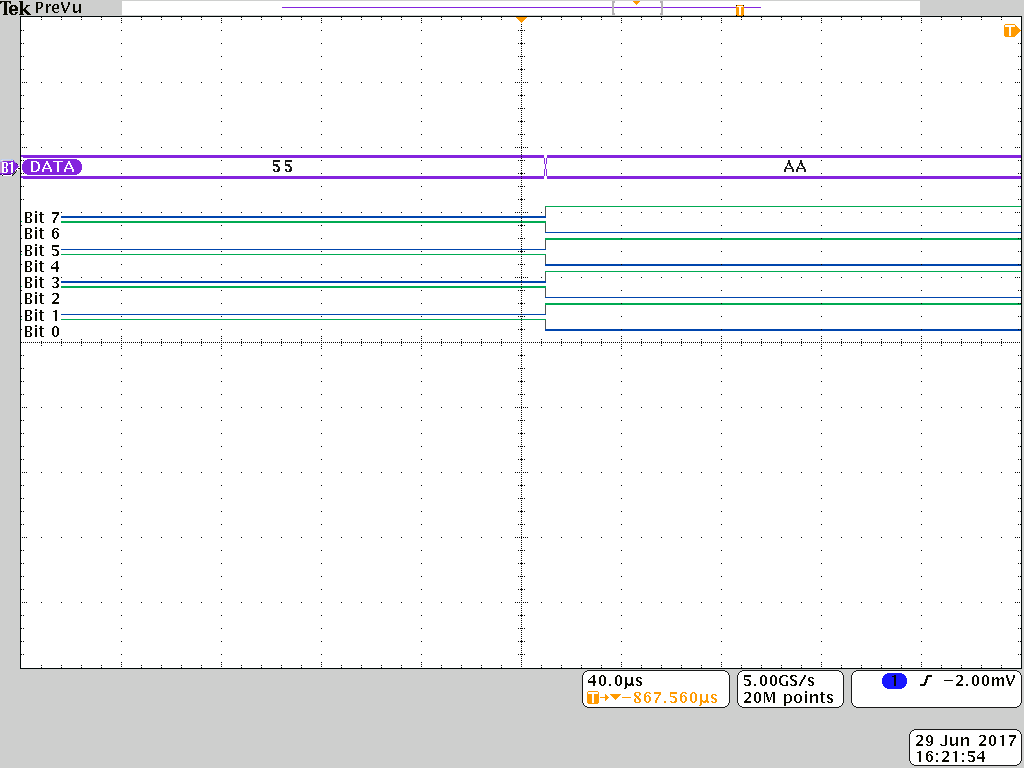


Fig. 58-Data is 0x55 in even locations and 0xAA in odd locations

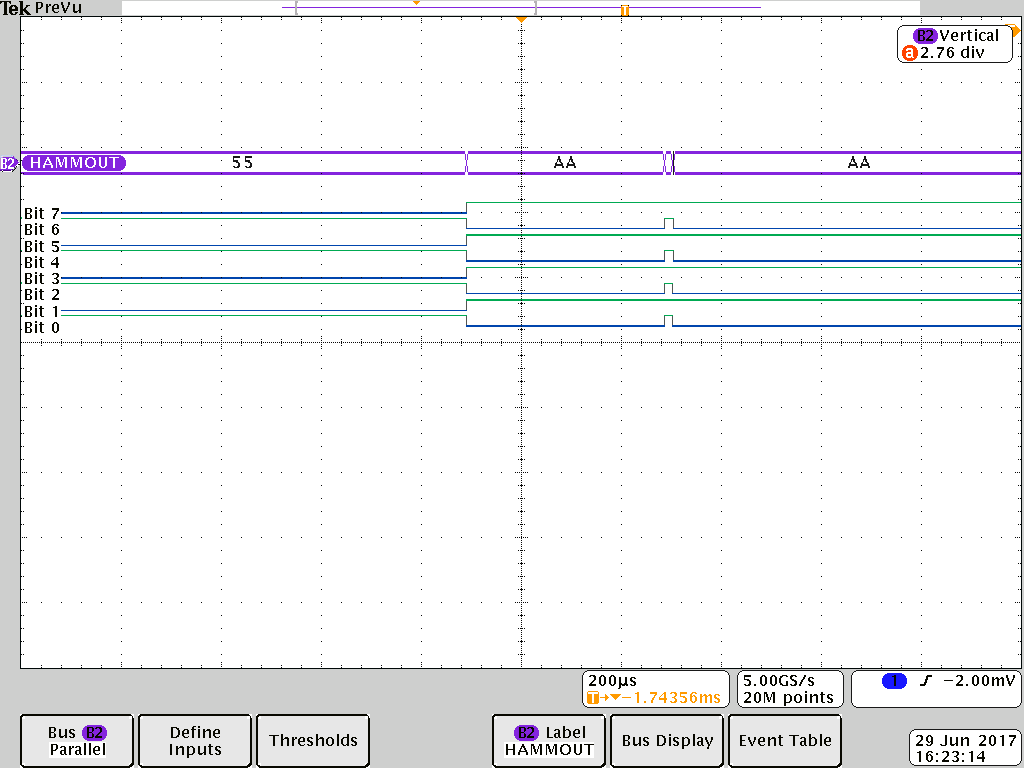


Fig. 59-Hammout is same as data i.e. 0x55 in even locations and 0xAA in odd locations.

## 10.7 Pattern 7 – writing 0x55 in even and 0xAA in odd memory locations

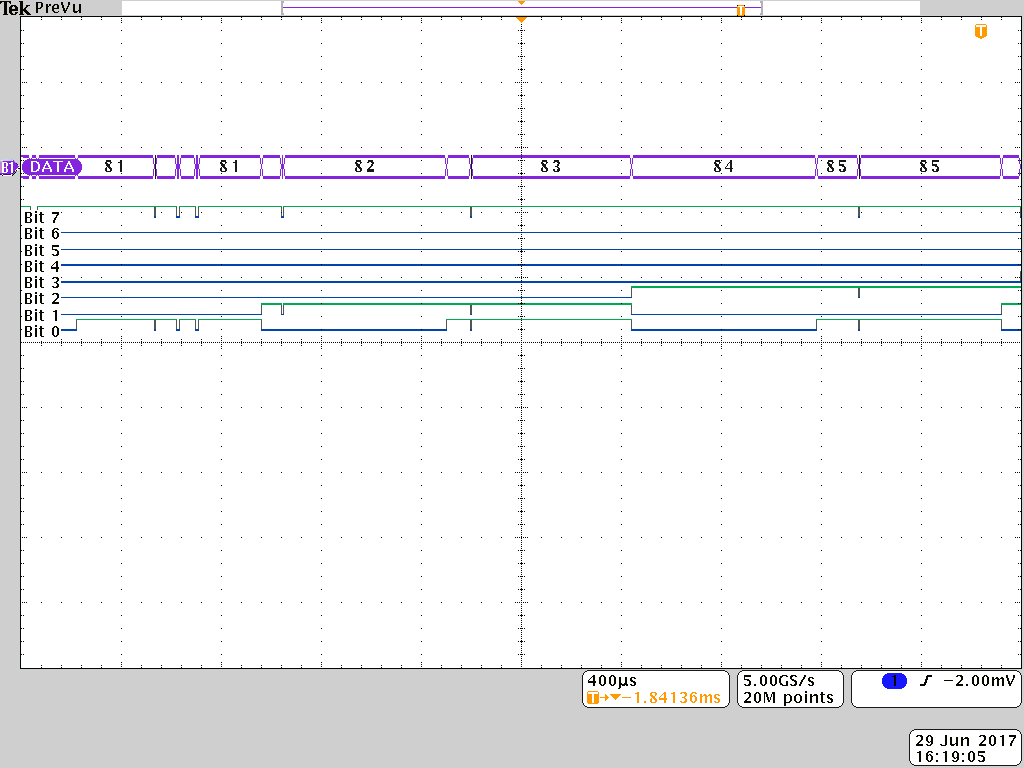


Fig. 60-Data is same as current address LSB

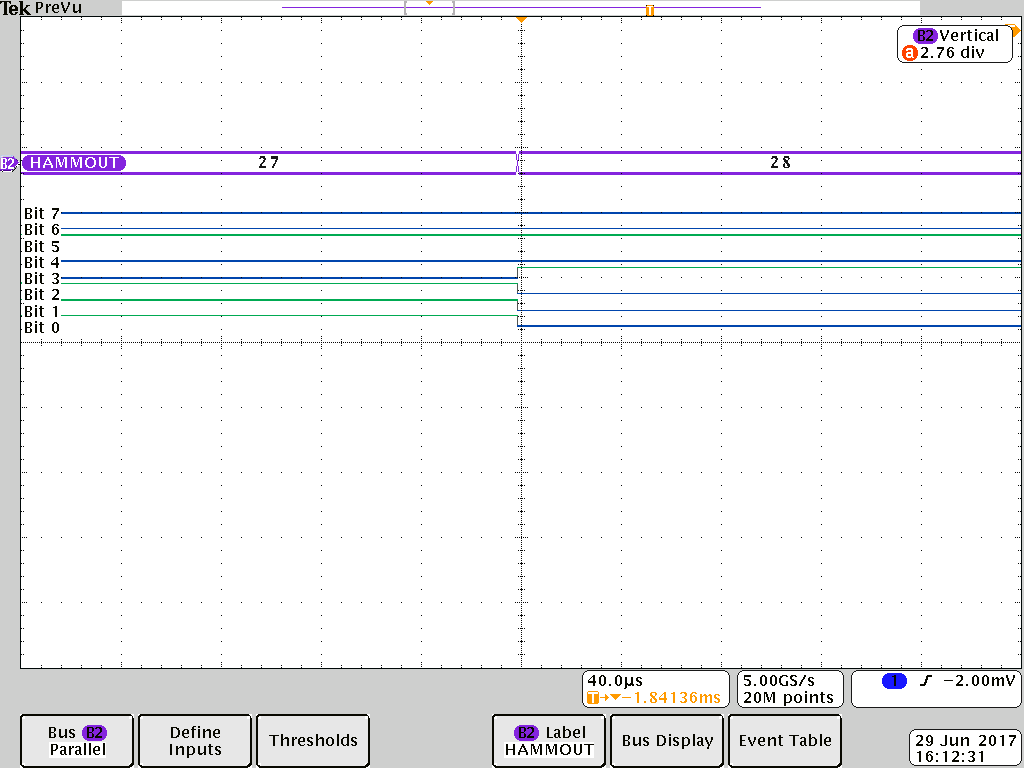


Fig. 61-Hammout is same as data i.e. current address LSB

## 10.8 Current Address

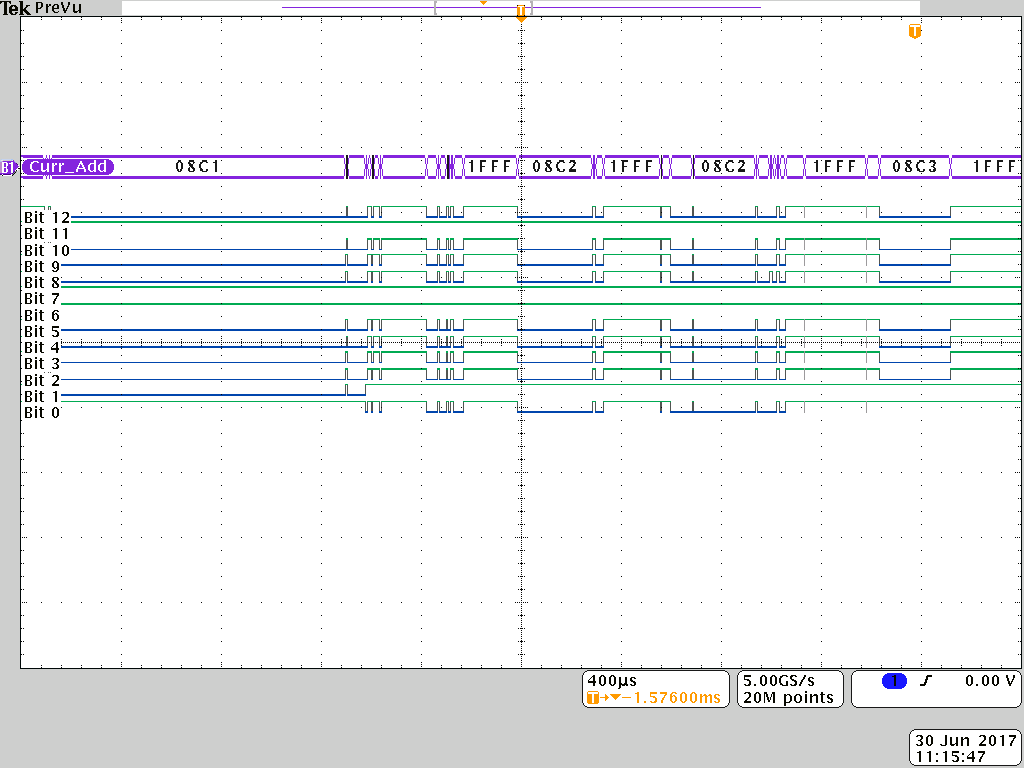


Fig. 62-Current address (13 bits) during write as well as read cycle.

# CONCLUSION

In this project, EDAC (Error Detection and Correction) Hardware Testing Board and its software has been designed and developed. Analytical study and implementation of required hardware and software has been done.

* EDAC chip is a self-designed product of SCL, Mohali. The chip has been thoroughly studied focusing on its different timing waveforms, control signals, SPRAM Memory, outputs and inputs.
* Dedicated PCB has been designed using OrCAD v9.1.
* Thorough analysis of the PIC18F6527 Microcontroller has been done, which essentially included the device’s specifications, ports, registers, configuration registers, oscillator clocks, Serial Communication, interrupts etc. Software interrupts form the major heart of the code.
* Subsequently, the programming of the PIC18F6527 microcontroller has been done in “C Language” using MPLAB X IDE software which controls the write and read operations on the device. SEE Testing is developed which tests various patterns (0x00, 0xFF, 0x55, 0xAA, 0xAA at even & 0x55 at odd, 0x55 at even & 0xAA at odd, Address LSB) by writing and reading from the whole memory location.
* Each pattern takes 13 seconds for execution.
* To create a conduit of communication between user and the PIC microcontroller, a Graphical User Interface (GUI) has been created in “Visual Studio 2010” using C# Language. Utilizing this GUI, the access to PIC port, Power Supply and Data Log was established.
* This testing board is for checking any errors that might occur due to extreme conditions and therefore a summary sheet below the log sheet is developed which lists all the errors.

# FUTURE SCOPE

# REFERENCES

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2. PIC Controller and Embedded System by Muhammad Ali Mazidi,Rolin D.Mckinlay,Danny Causey
3. Microelectronic Circuits by Sedra &Smith.
4. Micro-Processor course (EEE F241) and Digital Design course (EEE F125) of BITS Pilani.
5. C# pdf tutorial.
6. Visual Studio help of C#.
7. Stack Overflow website.

# ANNEXURE

## Parity bit

A parity bit, or check bit, is a bit added to a string of binary code to ensure that the total number of 1-bits in the string is even or odd. Parity bits are used as the simplest form of error detecting code. There are two variants of parity bits: even parity bit and odd parity bit.

## HARDWARE PINS

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Sr. No. | EDAC Pin No. | Pin Name | Pin Type | PIC Pin | Remarks |  | | | |
|  | 1 | 23 | clk | input PORAT A | **40** | **OSC2/CLK0/RA6** |  | | | |
|  | 2 | 24 | rst | 24 | RA0/AN0 |  | | | |
|  | 3 | 32 | csn | 23 | RA1/AN1 |  | | | |
|  | 4 | 38 | wn | 22 | RA2/AN2/Vref- |  | | | |
|  | 5 | 39 | oen | 21 | RA3/AN3/Vref+ |  | | | |
|  |  |  |  |  |  |  | |  |  |  |
|  | 45 | 48 | derd | Output PORTG | 8 | RG4/CCP5/P1D |  | | | |
|  | 46 | 33 | serc | 6 | RG3/CCP4/P3D |  | | | |
|  | 47 | 17 | ner | 3 | RGO/ECCP3/P3A |  | | | |
|  |  |  |  |  |  |  | |  |  |  |
|  | 35 | 61 | parity4 | Output   PORTB | 44 | RB4/KBI0 |  | | | |
|  | 36 | 62 | parity3 | 45 | RB3/INT3 |  | | | |
|  | 37 | 63 | parity2 | 46 | RB2/INT2 |  | | | |
|  | 38 | 64 | parity1 | 47 | RB1/INT1 |  | | | |
|  | 39 | 16 | parity0 | 48 | RB0/INT0 |  | | | |
|  |  |  |  |  |  |  | |  |  |  |
|  | 40 | 49 | syndrome4 | Output PORTF  And  PORT A(RA5 And RA4) | 11 | RF7/SS1 |  | | | |
|  | 41 | 50 | syndrome3 | 12 | RF6/AN11 |  | | | |
|  | 42 | 1 | syndrome2 | 13 | RF5/AN10/CVref |  | | | |
|  | 43 | 2 | syndrome1 | 27 | RA5/AN4/HLVDIN |  | | | |
|  | 44 | 3 | syndrome0 | 28 | RA4/TOCK1 |  | | | |
|  |  |  |  |  |  |  | |  |  |  |
|  | 6 | 34 | data7 | input PORTC | 32 | RC7/RX1/TD1 |  | | | |
|  | 7 | 31 | data6 | 31 | RC6/TX1/CK1 |  | | | |
|  | 8 | 29 | data5 | 36 | RC5/SDO1 |  | | | |
|  | 9 | 28 | data4 | 35 | RC4/SD1/SDA1 |  | | | |
|  | 10 | 27 | data3 | 34 | RC3/SCK1/SCL1 |  | | | |
|  | 11 | 26 | data2 | 33 | RC2/ECCP1/P1A |  | | | |
|  | 12 | 19 | data1 | 29 | RC1/T1OSI/ECCP2/P2A |  | | | |
|  | 13 | 18 | data0 | 30 | RC0/T1OSO/T13CKI |  | | | |
|  |  |  |  |  |  |  | |  |  |  |
|  | 14 | 57 | hamout7 | Output   PORTD | 49 | RD7/PSP7/SS2 |  | | | |
|  | 15 | 58 | hamout6 | 50 | RD6/PSP6/SCK2/SCL2 |  | | | |
|  | 16 | 59 | hamout5 | 51 | RD5/PSP5/SDI2/SDA2 |  | | | |
|  | 17 | 60 | hamout4 | 52 | RD4/PSP4/SDO2 |  | | | |
|  | 18 | 8 | hamout3 | 53 | RD3/PSP3 |  | | | |
|  | 19 | 9 | hamout2 | 54 | RD2/PSP2 |  | | | |
|  | 20 | 10 | hamout1 | 55 | RD1/PSP1 |  | | | |
|  | 21 | 11 | hamout0 | 58 | RDO/PSP0 |  | | | |
|  |  |  |  |  |  |  | |  |  |  |
|  | 22 | 45 | address7 | input     **PORTE AND   PORTF** | 59 | RE7/ECCP2/P2A |  | | | |
|  | 23 | 44 | address6 | 60 | RE6/P1B |  | | | |
|  | 24 | 42 | address5 | 61 | RE5/P1C |  | | | |
|  | 25 | 41 | address4 | 62 | RE4/P3B |  | | | |
|  | 26 | 40 | address3 | 63 | RE3/P3C |  | | | |
|  | 27 | 37 | address2 | 64 | RE2/P2B/CS/ |  | | | |
|  | 28 | 36 | address1 | 1 | RE1/WR/P2C |  | | | |
|  | 29 | 35 | address0 | 2 | RE0/RD/P2D |  | | | |
|  | 30 | 46 | address8 | 18 | RF0/AN5 |  | | | |
|  | 31 | 47 | address9 | 17 | RF1/AN6/C2OUT |  | | | |
|  | 32 | 15 | address10 | 16 | RF2/AN7/C1OUT |  | | | |
|  | 33 | 13 | address11 | 15 | RF3/AN8 |  | | | |
|  | 34 | 12 | address12 | 14 | RF4/AN9 |  | | | |
|  |  |  |  |  |  |  | |  |  |  |

|  |  |  |
| --- | --- | --- |
| Pin No. | Pin Name | Levels |
| 22 | VDD | 1.8V |
| 43 |
| 20 | VDDO | 3.3V |
| 30 |
| 6 |
| 4 |
| 55 |
| 53 |
| 51 |
| 25 | VSS | 0V |
| 7 |
| 21 | VSSO | 0V |
| 14 |
| 5 |
| 56 |
| 54 |
| 52 |

|  |  |  |  |
| --- | --- | --- | --- |
| 50 Pin Connector Connection | | | |
| Pn Name | Wire Board | PCB Board | Remarks |
| VDD | 1 | 10 | PIC VDD 3.3V |
| VDD\_1 | 3 | 2 | 1..8V |
| VDDO | 5 | 33 | 3.3V |
|  |  |  |  |
| VSS | 2 | 1 |  |
| VSS | 4 | 8 |  |
| VSS | 6 | 50 |  |
|  |  |  |  |
| PC\_TX | 44 | 11 |  |
| PC\_RX | 46 | 13 |  |

## SCHEMATIC OF THE BOARD

