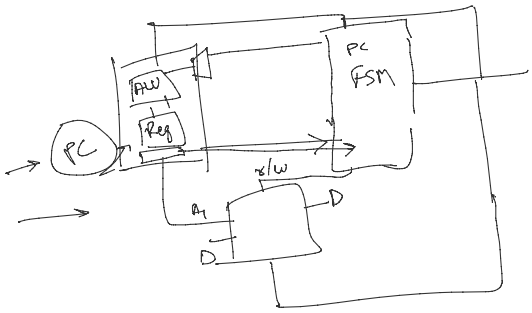
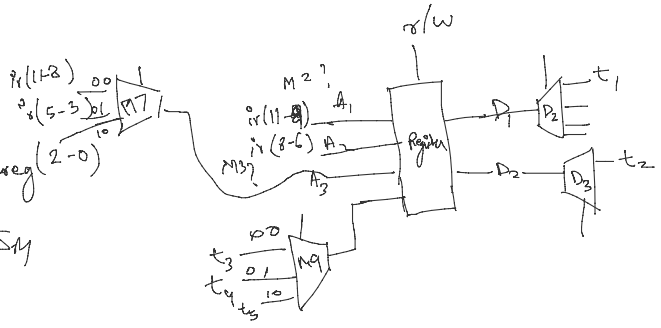
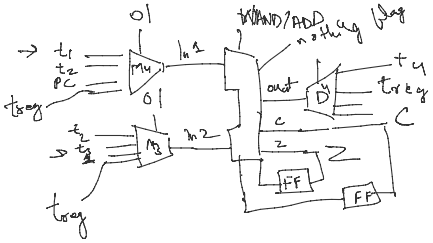
20 May 2021 23:39



1) Datapath

signals —
1) PC (15 – 0)
2) Instruction (15–0)
3) t_1
4) t_2
5) C
6) Z
7) t_3
8) t_4
9) t_5
10) t_{reg}
11) Instr_state ← by FSM





2) FSM

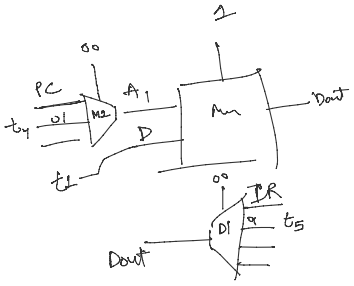
S_0 :— mem_read = 1

if LA, LHI, SA, JAL: M2 = 00
D1 = 00
else next_stat = S_1

S_1 :— D2 = 00
D3 = 00
M2 = 00?
M3 = 00?

if ADI, LHI, LW, SW, BEQ, JAL :-
next state :- S4

if ADD, ADC, ADZ, NAN
next state = S5



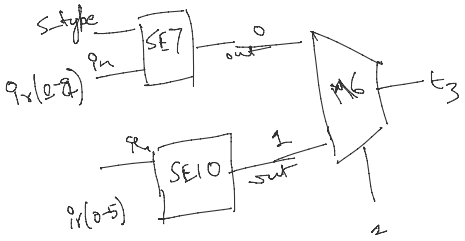
S_5 : if ADD,
ALU_control = 0
M_4 = 00
M_5 = 00
D_4 = 00
nothing = 0

ADC
nothing = !C
M_4 = 00
M_5 = 00
D_4 = 00
similarly ADZ

NAND —

if ADI, LW, SW,
M_4 = 01
M_5 = 01

if JAL:
M_4 = 00
M_5 = 01



if ADI
M_4 = 00
M_5 = 01

if LW:
if (treg == 8) treg = "00000000"
next_state = S10
ALU_c = ADD
else M_4 = 00
M_5 = 11
next_state = S7

check for last state also

S4: if LHI:
s_type = 1
else s_type = 0

if stype = 1

else stype = 0

if JAL or LHI

M6 = 0;

if ~~SW~~, ADI, LW, SW, BEQ

M6 = 1

S6: if ADD,
M7 = 1
w = 1

if ADI:
w = 1 C
0
M7 = 1

if ADZ

M4 = 1

next_state = S10

if NAND

if LHI:
M4 = 0
M7 = 0

if LA:
M7 = M4 = 10
reg_wr = 1
next_state =

next_state = S10

if LW:
M7 = 1
M4 = 10
next_state = S12

S10: M4 = 10

if (BF=0):

if ($t_1 = t_2$):
M3 = 01

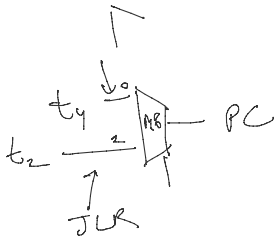
else M3 = 10

elsif (JAL):
M5 = 01

else
M5 = 10
next_state = S11

PC+Imm

if LA:
M1 = 01
D1 = 01
next state = S6



S11: if JLR:
M8 = 1

else M8 = 0

next_state = S0

S7:

mem_read = 1

~~M1 = 10~~

~~M4 = 10~~

M1 = 01

D1 = 01

next_state = S6

S8 :

mem_write = 1

$f_{11} = 01$

next_state = S10

---

t_1 - Address

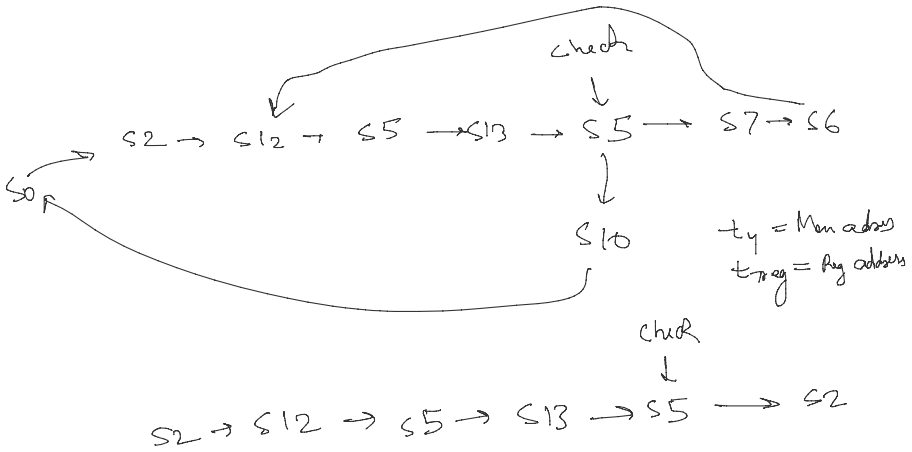
$t_1' \leftarrow t_1$

S12: Content increment → t_{reg}

next_state = S5

S13:

next_state = S5



check

S2 → S12 → S5 → S13 → S5 → S2