MD AAMIR RAIHAN

Graduate Research Assistant araihan@ece.ubc.ca

CAREER OBJECTIVE

My career objective is to be a part of an excellent research group and carrying out research in the interdisciplinary field of computer engineering, machine learning and AI. My lifelong aim is to build a machine Intelligent enough to carry out task with human level precision.

EDUCATION

University of British Columbia **2017-2019**

Degree: MASc

Currently working under the supervision of professor Tor Aamodt for the development of machine learning accelerator.

Indian Institute of Technology (BHU), Varanasi **2011 – 2015**

Degree: Bachelor of Technology

Semester	I	II	III	IV	V	VI	VII	VIII
SGPA	8.80	8.28	8.00	8.29	8.63	8.75	9.09	8.75
YGPA	8.54		8.14		8.69		8.91	
DGPA	8.56							

Mahendra Muni Saraswati Shishu – Vidya Mandir(Jharkhand) **2011**

- All India Senior School Certificate Examination [**12th**] (Percentage: **86.4%**) **2009**

CarmelSchool,Madhupur(Jharkhand)

- All India Secondary School Examination [**10th**] (Percentage: **93.14**%)

SKILLS AND INTERESTS

- **Languages**: Verilog HDL, VHDL, Assembly Language, C, C++, CUDA C, Bluespec Verilog, Python (Basics). ○ **Technologies:** Xilinx ISE, Xilinx EDK, ISIM, Matlab, Simulink, Octave, PSpice, Proteus, Eclipse, WINAVR, Mathematica.
- **Computer platforms**: Windows XP/7/8, Linux (Ubuntu 11.10, 12.04).
- **Areas of Interest:** VLSI, Computer Architecture, Neural Network and Machine Learning.

RESEARCH EXPERIENCE

Implementation of Neural Network(RBFNN) on reconfigurable hardware **May-2014 –July 2014**

Research Guide: Prof. SK Nandy (http://cadl.iisc.ernet.in/cadlab/people/nandy/)

CAD LAB(http://cadl.iisc.ernet.in/cadlab/),SERC, IISC Bangalore, India(http://www.iisc.ac.in/).

Software Used: Bluespec System Verilog, Verilog and MATLAB.

Research Outline: This research culminated in the development of a RBF Neural Network on a novel reconfigurable platform called Hyper-Cell. Hyper-Cell was a 2D mesh of configurable compute units. The task was to study the RBFNN dataflow graph and develop efficient partitioning and mapping algorithm for implementing any dimension RBFNN on Hyper-Cell. The algorithm must be scalable and backward compatible such that increasing the dimension doesn't disturb the existing mapping of neural network. Implemented neural network was found to be around 100x faster than neural network implemented on multi core configuration.

The Paper was presented at VLSI Design Conference 2015 (3 Jan. – 7 Jan. 2015).
Link: A Flexible Scalable Hardware Architecture for Radial Basis Function Neural Networks

INDUSTRIAL EXPERIENCE

FREESCALE ENGINEERING ROTATION PROGRAM **IP Verification Team**

July'16 – Nov'16

Project Outline: During this rotation I learned about the verification methodology such as constrained random stimulus generation, assertion-based verification, formal verification and functional coverage. I was given the task of migrating AXI VIP from Synopsys to Cadence vendor in the existing SD host controller testbench. During migrating VIP I gain familiarity with System Verilog, UVM based testbench, AXI Protocol and SD specs. I successfully completed the migration within the specified time.

SOC Validation Team **Nov'16 – Mar'16**

Project Outline: During this rotation I learned about the SOC validation and Debugging technique. I was given the task of validating UART in a SOC. I developed an entire regression framework consisting of around 3000 testcase for exhaustive validation of UART. The testcase comprises of both IP as well as SOC specific validation testcase.

Application Team **Mar'16 - July'16**

Project Outline: Worked on the development of low power and high data rate use case of direct attached storage. Low power target achieved by switching off the ddr and using the onchip memory and executing code directly from flash (XIP). High performance target is achieved by leveraging the hardware coherent capabilities. During this project I learned about the soc boot up procedure, uboot and yocto project.

The demo was showcased in NXP FTF demo(https://community.nxp.com/docs/DOC331590) A poster was presented in the NXP internal poster event.

POSITION OF RESPONSIBILITY

Graduate Teaching Assistant **Sept'17-Dec'17**

My responsibility was the to conduct the lab sessions for the course Introduction to Microcomputers, CPEN211, help students with their lab experiments, homeworks and evaluate their labs, grade the mid-terms and final.

Coordinator of Digisim (Digital System Model) **Feb'14**

Event Info: This is an event organized under the banner of **AAYAM 2014,** Techno-Management Fest by **Electronics Engineering Society, Department of Electronics Engineering, Indian Institute of Technology, Banaras Hindu University, India.**

Event Outline: I along with two other students coordinated this event called Digisim. The goal of the event was that participants should simulate a complex digital system at the higher abstraction level thus enabling them to think in term of architecture and design tradeoff. This event was successfully held in Feb. 2014 and witnessed great participation from the freshman and sophomore year students.

TECHNICAL/ONLINE COURSES

Machine Learning **Stanford Univ., Coursera** **Duration : 10 Weeks**

- This was an online certified course at www.coursera.org, by prof. Andrew Ng of Stanford University.
- Used Matlab and Octave to implement different types of Machine Learning problems.
- Covered Supervised-unsupervised learning, Neural Networks, Liner-logistic regression, SVM, Recommender System.
- Received a **Certificate of Accomplishment.**

Circuits And Electronics **MIT, Coursera** **Duration: 14 Weeks**

- This was an online certified course at www.edx.org, by prof. Anant Agarwal, MIT. This course was same as taught to students of MIT with the same toughness level but online exams.
- Course covered whole electronics course right from KCL, KVL to CMOS logic, including MOSFET, second order circuit solving, Op-amps, oscillators, filters, small signal analysis, feedbacks and different responses. Received a **Certificate of Master.**

PROJECTS COMPLETED

Implementation of a 32 Bit Pipelined MIP Processor **Supervised by: Prof P.K Mukherjee**

- Designed and implemented a subset of a 32-bit pipelined MIPS processor supporting basic instruction using verilog hardware description language.
- The design support forwarding and basic branch prediction logic.
- The design had been tested using a set of assembly language instructions by emulating the design on Xilinx Virtex 5 FPGA Board.

Text Extraction from Business Card **Supervised by: Prof R. R. Das**

- Implemented Optical Character Recognition using neural network on matlab. The preprocessing phase consist of noise removal and character segmentation using text bounding box detection and binarization. Feed forward neural network with one hidden layer was used to recongnize the segmented character.The recognized text is parsed to extract the name and phone number.
- Different neural network like feed forward neural network with different numbers of hidden layer and RBF neural network with different kernels were implemented to study the training and testing accuracy of neural network.

16 point FFT on Xilinx FPGA

- Developed a fully-pipelined implementation of the 16 point FFT algorithm based on time decimation using the butterfly structure. Verilog HDL was used for RTL description and the design was implemented on Xilinx ML505 evaluation platform.
- The design also included an overflow detection technique which would indicated that which of the 16 outputs have been affected due to overflow.

Autonomous bot based on Image Processing

- Developed Bot capable of distinguishing between different colors and shapes and is capable of making real time decision, for the selection of the path on the basis of object identified,in a 8*8 grid.
- Secured **Second Prize** in Optika, event based on Image Processing based Autonomous Bot in AAYAM'13.

OP-AMP Simulator

- Developed OP-AMP simulation program as a part of curricula software project.The simulator was developed in C and support basic OP-AMP circuits simulator supporting inverting and non inverting modes.

ACADEMIC AND EXTRACURRICULAR ACHIEVEMENTS

- Completed Airtel Delhi Half Marathon 2015.
- Part of the Freescale prestigious ERP Program in which only 20 individual from US, India and China get selected.
- Secured **2nd Place** in the event Optika –Image Processing Event in the annual technical fest(2013) of IIT (BHU) Varanasi.
- Secured **1st Place** in the event Robowar in the annual technical fest(2012) of IIT (BHU) Varanasi.
- An active member of Electronics Engineering Society,IIT (BHU) Varanasi.
- Secured a position in **top 0.5%** among **500,000** candidates in highly competitive **IIT-JEE 2011** in the first attempt. Cracked **AIEEE-2011** securing a position in **top 0.1%** among **1,000,000** lakh candidates. Secured **99.3 percentile** in National Cyber Olympiad 2009.