Total weightage in course total =30%	Objectives
Part 1 (30%=9 Marks)	Database Generation: Preferred PVT aware 5000 samples in targeted technology node at given supply voltage. Targeted performance: Leakage power Simulator: NGSPICE Targeted Std. Cells: NAND2, NOT, AND2, XOR2, OR2, AND3, etc. Targeted Technology nodes: CMOS 45nm, CMOS 32nm, CMOS 22nm, CMOS 16nm Targeted Models: MGK, HP, LP
	(5k*2^n number of samples for n input gates)
	EDA analysis for the given tech nodes
	Decide approach/technique for ML modelling
Part 2 (30%=9 Marks)	Fast and accurate ML models development for the prediction of leakage power in basic gates- NAND2, NOT, AND2, XOR2, OR2, AND3.
	ML model analysis for leakage power
Part 3 (20%=6 Marks) Project report (20%=6 Marks)	Verification of approach and ML model using C17 benchmark circuit
	Finally, the leakage power prediction in C499 benchmark circuit utilizing the pre-modelled std. cells. Comparison: Model Vs. Ngspice simulation
	Report+ Presentation