An Introduction to Lab2

Lecture 3 for Information Processing

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What is in this lab?

- Design a NIOSII system.
- Understand the design process of a NIOSII system.
- Program the Max 10 FPGA chip on the DE10-Lite board with your soft processor.
- Write code that runs on the NIOS processor to display a message on a terminal.
- Explore and test the capabilities of your NIOS II system design.

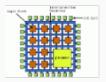
Soft Vs. Hard processors

- Hard processors normally have a fixed architecture
- NIOSII is a soft processor
 - customizable (eg. size, performance)
 - add or remove certain features (eg. floating-point units)
 - custom instructions or extensions of the instruction set
- Soft processors are normally on FPGAs, running at a slower clock rate

Hard Processors (eg. Intel, ARM, AMD)

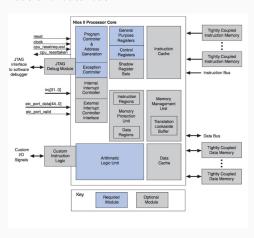


Soft Processors (MicroBlaze, NIOS II)



Processor architecture

- Register files
- Arithmetic logic unit (ALU)
- icache and dcache
- instruction bus and data bus ...

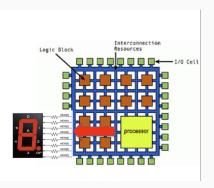


Processor implementation

- A NIOSII implementation is a set of design choices
- A functional unit (i.e. fp-mult) can be implemented in
 - hardware
 - emulated in software
 - omitted completely...
- Another example is division support

What do you do in Lab2?

• Control the lighting sequence on LEDs through the NIOSII processor



Questions?

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