p89 2
PR

VLSI design 2001

Question A

The *constant field* model of MOS scaling applies a dimensionless factor α to manufacturing dimensions (length, width and thickness), voltages and processing concentrations, so that channel thickness remains unchanged. For example, with $\alpha = 2$, all dimensions would be halved. Derive approximate expressions for the consequent scaling of:

- Gate area
- Channel resistance
- Current
- Load capacitance
- Gate delay
- Static power consumption (per gate)
- Power density (per unit area)
- Current density (in wires)

What are the main implications for speed, size and power? [8 marks]

Constant voltage is an alternative model in which only the manufacturing dimensions are scaled, leaving voltages unchanged, so the channel thickness increases by a factor α. Derive approximate expressions for the consequent scaling and summarise the main implications. [8 marks]

What further factors make both models inappropriate as device sizes continue to decrease? [4 marks]

Answer

		Constant field	Constant voltage
Length, width, thickness	L, W, D	$1/\alpha$	$1/\alpha$
Voltage	V	$1/\alpha$	1
Channel thickness	d	1	α
Gate area	$A = L \times W$	$1/\alpha^2$	$1/\alpha^2$
Channel resistance	$R \propto L \div (d \times W)$	1	$1/\alpha$
Current	$I = V \div R$	$1/\alpha$	α
Load capacitance	$C \propto A \div D$	$1/\alpha$	$1/\alpha$
Gate delay	$T \propto R \times C$	$1/\alpha$	$1/\alpha^2$
Static power consumption	$W = V \times I$	$1/\alpha^2$	α
Power density	$W \div A$	1	α^3
Current density	$I \div (W \times D)$	α	α^3

Speed increased by α, density by α^2 while keeping power density constant. Speed and density increased by α^2 but power density up by α^3.

Tunnelling, leakage, edge wall capacitance, metal migration, wire delay...