2001

Digital Electronics

a) $reg_0, reg_1, reg_2, reg_3$ clock.
   gnt_0, gnt_1, gnt_2 gnt_3

b) ~~two bit~~ eg $S_1 S_0$ to record last grant.

c) $gnt_0 = \overline{S_1}\,\overline{S_0}$ ~~eg~~ $reg_0\ \overline{reg_1}\ \overline{reg_2}\ \overline{reg_3}$

   $\overline{S_1}\, S_0\ \ reg_0\ \overline{reg_2}\ \overline{reg_3}$

   $S_1\, \overline{S_0}\ \ reg_0\ \overline{reg_3}$

   $S_1\, S_0\ \ reg_0$

   etc

   $S_1' = gnt_2 + gnt_3 + S_1\ \overline{gnt_0}\ \overline{gnt_1}\ \overline{gnt_2}\ \overline{gnt_3}$

   $S_0' = gnt_1 + gnt_3 + S_0\ \overline{gnt_0}\ \overline{gnt_1}\ \overline{gnt_2}\ \overline{gnt_3}$

d) take eg gnt_0, factor reg_0 out and minimise with
   five variables, then multiply reg_0 through.