Solution notes

ECAD 2005 – Paper 3 Question 1 (SWM)

(a) A D flip-flop (DFF) will go metastable if the data (D) input changes when the clock input is going high (assuming the DFF is positive edge triggered).

(b) The parameters *setup* and *hold* specify the time before and after the clock edge when the data input must not change in order to avoid metastability.

(c) A D flip-flop will eventually move from the metastable state to a stable state (i.e. outputting a binary value). The time it takes to move from the metastable state to a stable state can be modeled as a probabilistic process.

(d) Synchronisation is the process of sampling an asynchronous input using a clock which determines the sample rate. The sampled signal is said to be synchronous with the clock.

(e) A synchroniser can be made from two D flip-flops arranged as a two bit shift register.

(f) For `count0`, the asynchronous input will be used to determine whether to increment `count0` or leave it the same. Since `count0` is made of 64 flip-flops and the fan out of `asyncInput` will result in unequal delays, it is inevitable that when `asyncInput` arrives near a clock edge, some flip-flops will store the incremented state and others the unchanged state. There is also risk of metastability, but this is less probable. [3 marks for this part]

For `count1`, the key is likely to bounce which produces extraneous key presses. [2 marks for this part]

This material is covered in lectures 3 and 4, and this knowledge is applied in the associated laboratory sessions.