Digital Electronics Paper 2 Question 2 2005

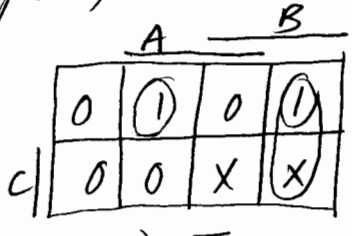
Also for Diploma & Part II (gen) Paper 11 Question 1

(a) The state table for the 0→5 counter is:

current state			next state		
C	B	A	C′	B′	A′
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	0	0	0
1	1	0	X	X	X
1	1	1	X	X	X

by inspection, $A' = \overline{A}$

for B′

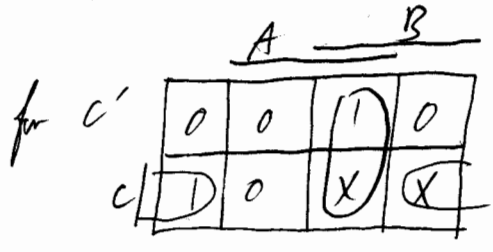


so $B' = (A \oplus B) \cdot \overline{C}$

min. sum of products for B′:

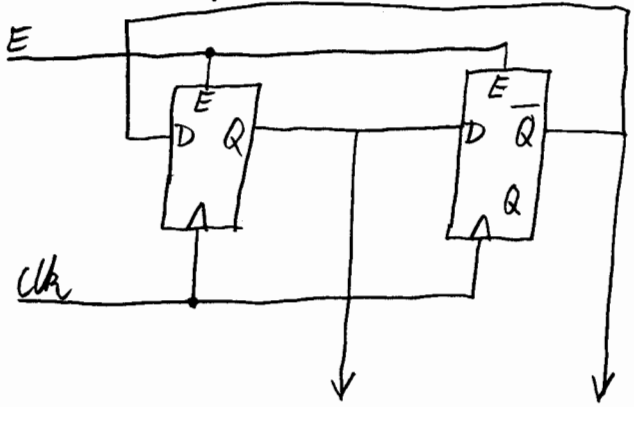
$B' = A.\overline{B}.\overline{C} + \overline{A}.B$

for C′



$C' = A.B + \overline{A}.C$

(b) This is basically from the nots but many will have to derive the circuit.



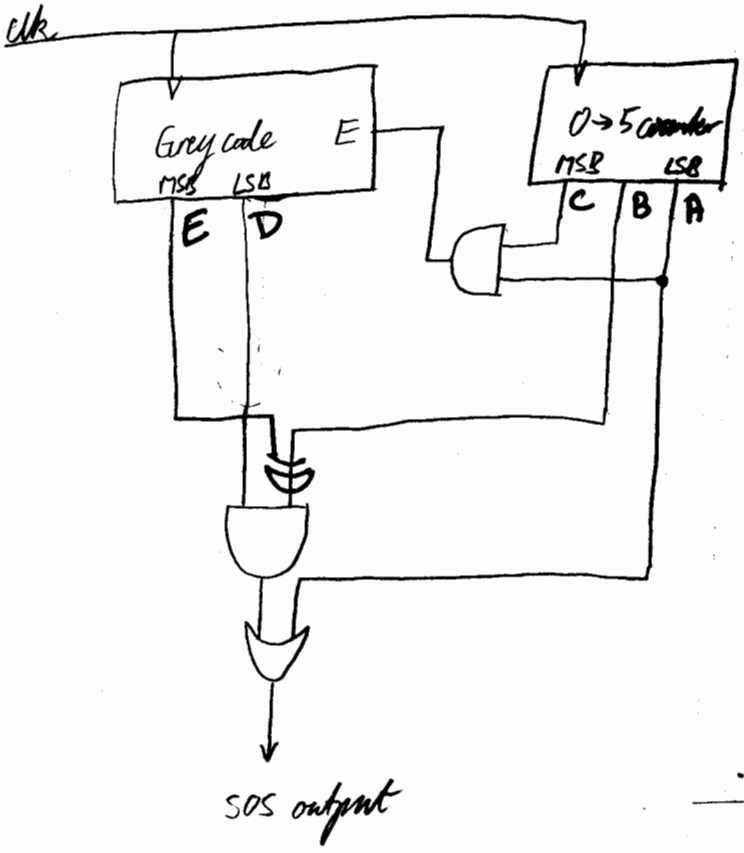
Computer Science Tripos Part II (General) 2005

Paper 11 Question 1

SWM — Digital Electronics

P2Q2 2005 cont...

(c)



SOS output = 1 when A = 1

When A = 0, SOS output =

D \ E \ B C	00	01	11	10
00	0	0	X	0
01	0	1	X	0
11	0	0	X	1
10	0	0	X	0

$= \bar{B}DE + BDE$

$= D(B \oplus E)$

$\therefore$ SOS output $= A + D(B \oplus E)$

This question covers lecture 3 (logic minimisation), 5 (flip-flops) and 6 & 7 (state machines).