SOLUTION NOTES

Computer Design 2003 Paper 6 Question 2 (IAP)

(*a*) Briefly describe the differences between a microprocessor's interface bus, a system I/O bus (such as PCI), and a peripheral interface. Consider the bandwidth characteristics and physical implementation of each. [8 marks]

CPU bus: 32-40 address, 32-64 data lines (unless a multiplexed address/data bus is used). A MREQ signal to indicate when the CPU wishes to issue an external cycle. A Read/nWrite signal. A Wait signal to allow peripherals to allow stall cycles to be inserted for 'slow' peripherals. Other possible signals include one to indicate when accesses are to Sequential memory locations, and BusRequest/Grant signals to allow multi processor systems. Clocked at 100-400MHz, bandwidth of perhaps over a GB/s. Latency just a few clock cycles. Implemented on a PCB, possibly just point-to-point connections.

PCI: multiplexed 32/66bit AD bus, multiplexed control signals. Supports bus mastering by different devices. Clocked at 33-133MHz. Allows plug in cards, hence variable but limited number of loads. Has to autodetect and support 32/64bit and different speed cards.

SCSI: 8/16 bit plus control signals. Differential signalling enables bus to be quite long. May be logically a bus, but electrically is point to point links. 50-300MB/s.

(*b*) Show how four 64Mbit byte-wide DRAM chips could be interfaced to a simple 32bit microprocessor. Give a schematic diagram showing the connections, and a timing diagram to demonstrate the operation of the control signals. [8 marks]

32MB DRAM in total. Connect each chip's Data line's to a different byte of the processor's 32bit data bus.

DRAM chip has 23 address bits in total. Assume 13 col bits and 12 row bits. Use a 12 bit 2:1 multiplexer to select address bits 2-14 (col) or bits A15-A26 (row) onto the DRAM's address bus. Connect R/nW. Address decode logic for all chip select lines (ignore byte writes).

Timing diagram will show a wait states being inserted, RAS and CAS being strobed, and control signal for multiplexer.

(*c*) Why might accesses to sequential DRAM addresses be treated differently from non-sequential ones? [4 marks]

Once a Row has been read and latched by the sense amplifiers, rapid random access to

entries within the row is potentially possible (RAS is held low, CAS repeatedly strobed). Rather than figuring out exactly which accesses are to the same row, it is common just to detect sequential accesses (often the CPU identifies these), and allow them to proceed without wait state insertion.) Some modern DRAMs support burst mode whereby the low address bits are auto-incremented.