SOLUTION NOTES

Structured Hardware Design 2002 Paper 2 Question 1e (4-mark question) (DJG)

The question relates to a situation that is quite common where one part of a design needs to be implemented in high-performance technology and this part will generate the clock for the lower-speed remainder.

Normally, the clock should be generated from a flip-flop output in the high-speed section, rather than a gate, to avoid glitches. Typically there is also data passing from the higher-speed section to the lower-speed section, and if this too has come out of flip-flop outputs, it will tend to violate the setup and hold times of the flip-flops it drives in the lower-speed section.. Therefore the state diagram of the high-speed section must have the property that the clock and output data never change at the same time.

If transfers are made at a slower rate, perhaps requiring a wider bus to transfer the same amount of data, then there is more tolerance to parametric variations in the speed of the two logic families.

[A sketched diagram might be faster than writing this out in English.]