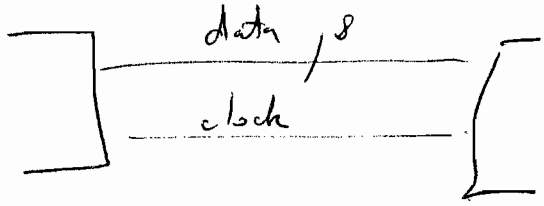
Structured Hardware Design

SHD 2003 20 Mark Q

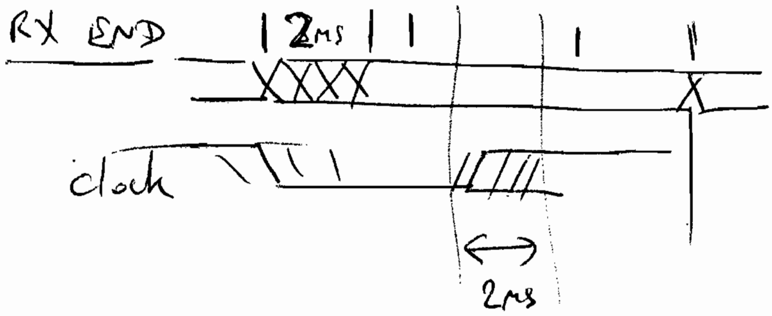
a)



Sending end

We take the clock low as we change the data. Clock active edge has maximal skew margin.

b) Assume all pipes between two nodes are roughly the same length, so tolerance is 1ms at both ends, which is 2ms total. Add a further 1ms for safety.



Margins needed when clock is slow and data fast and vice versa.

So total period is $2+1+2+1 = 6ms$

Data rate $8/6ms = 1.3$ kbps.

~~c) ...~~ Here we assume multiple pulses can be in transit in each pipe at one time (as sound waves) so delay down the pipe does not alter the result ~~half duplex~~ during simplex operation).

SHD 2003 20 Mark Q (continued)

c) The start of a packet could be indicated in a number of ways.

One way is that a dummy byte of all ones is added to the start, so that pressure in the data pipes is detected in advance of the first clock edge, but we could just wait for the clock edge.

End of packet can be found by counting clock pulses.

d) If both ends start at once, a collision might happen with data being corrupted. To avoid this, one could start the packet with a random bit pattern and check it is stable on the bus before asserting the first clock.

I would not use an extra pipe. Better would be a CRC byte on the end.

(The 10ns delay time down a pipe means that some contention will occur in any solution – even token passing will have contention for token creation.)

Five marks per part.

I would expect an answer of this level of detail for full marks.