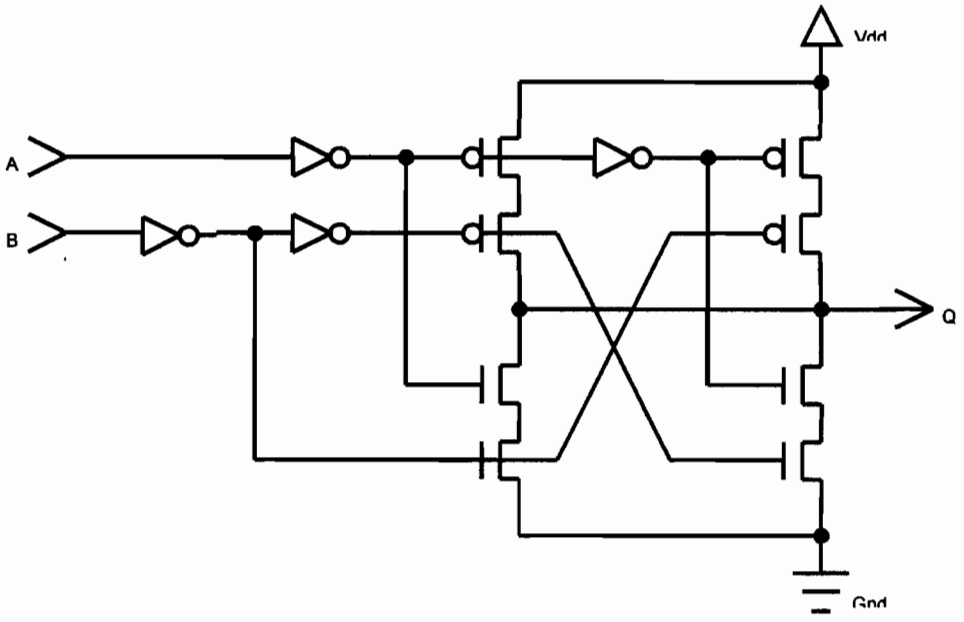
VLSI 2003

P8q2
PR

Solution A

Pulls up when A=1 & B=0 or when A=0 & B=1. Pulls down when A=B=0 or when A=B=1.

Each input is controlling four transistors which imposes a heavy load.
Using nFET pull-ups and pFET pull-downs restricts the voltage swing on the output, which will be exacerbated when gates are cascaded.



Invertors buffer inputs and allow pFET pull-ups and nFET pull-downs.

Use two invertors on each of three inputs, pull up on AB'C', A'BC', A'B'C and ABC, pull down on A'B'C', A'BC, AB'C and ABC'. Revised circuit uses 16 transistors so cascaded pair uses 32 and suffers 6 gate delays. Complex circuit uses 36 transistors but only suffers 3 gate delays.

Use an extended C element for each of Q_0 and Q_1. Preliminary circuit has A_0, A_1, B_0 & B_1 feeding pFETs in series for pull-up and two parallel pull-downs, one with A_0 & B_1 feeding nFETs in series, the other with A_1 & B_0. This drives invertor to give Q_1 with week feed-back invertor to hold state.

The question relates to the CMOS design part of the course. The last part expects knowledge of self-timed circuit design.