1999 Digital Communication I

~~p5q3~~
p6q3
IML
p13q3

of a transmitter keeping a large than permitted congestion window or possibly retransmitting on shorter timeouts.

Detecting non conformant applications is nontrivial. One would have to construct a TCP implementation which modelled the implementation being monitored, passing the times and TCP headers of all packets going to and from the monitored implementation. Moreover, some knowledge about the path between the monitor and monitored would have to be acquired. The potential for route oscillation (or asymmetric routes) would have to eliminated. For all of these reasons the ISP would want to monitor the implementation at the point of attachment to the ISP and this would only be sensible for directly attached customers.

An ISP wanting to monitor traffic originating from another domain would only be able to monitor the frequency and rate of retransmissions (but were getting well beyond the course here…)

Digital Communication I

Question 1

a) In circuit switching, higher layer channels (circuits) appear strictly periodically on a lower layer channel. Typically a repeating frame structure is transmitted on the underlying channel and each circuit is assigned the same timeslot in each frame. In packet switching the higher layer channels appear sporadically; access to the underlying channel is demand driven. Because of this, there is no need to identify a circuit with symbols in the channel whereas with packets there is. Thus packets must contain addressing information. Circuits are identified by their temporal location within a multiplex of several circuits. Note that the address to which a circuit is connected is a different concept to the allocation (eg time slots) which the circuit receives on various links between the two end points of the circuit.

A circuit switch must demultiplex links each containing a number of circuits and transfer timeslots of a incoming circuit to the timeslots of the correct outgoing circuit. It must perform this with constant delay for each timeslot within a circuit connection. There will be no contention for resource on outgoing links since each circuit connection will have a periodic set of time slots allocated to them.

A packet switch has the same task of demultiplexing incoming links, but instead of using temporal information, addresses within packets must be examined. A determination of which out going link that the packet should be sent on is made. Now however there can be contention for the outgoing link and some sort of packet scheduling will be necessary.

Circuit switching is advantageous when the user of the channel wants to see constant capacity and constant delay. Packet switching is useful when the each user of the channel is making bursty demands on the channel.

b) Packet switching provides rate decoupling between source and destination. Individual workstations tend to send bursty traffic to any particular destination, so packet switching will always have a place here. As traffic is aggregated up however it will be less bursty and circuit switching in the middle of a network will be more appropriate. [This is a fairly open ended question.]

Question 2

a) A hierarchical address space is one in which the address is composed of a number of components arranged in a hierarchy. Lower components only need to be examined within the domain of the higher level components. Such addresses conform to our intuitive concept of address and aid the routing process. An example is the IP address space in which addresses are divided into network and host numbers. The Ethernet address space is nonhierarchical.

b) The Address Resolution Protocol (ARP) is protocol which can be used to map network level addresses onto link level addresses. It generally takes advantage of the broadcast nature of shared media LANs. In the case of IP to Ethernet ARP, a sender A with IP address Aip, and Ethernet address Aet wishing to send to B with IP address Bip but not knowing B's Ethernet address, broadcasts an ARP Request :

ARP Request
Aip
Aet
Bip

to which B (assuming it received the requrest) responds with an ARP Reply sent to Aet:

ARP Reply
Aip
Aet
Bip
Bet

Other hosts which receive the ARP Request and which had store an address mapping for A will update the mapping. They can't for the reply sent by B since this was sent only to A.

- Hosts will only remember mappings for a few minutes and then throw them away. This ensures that the state which is retained is always up to date. A host rebooting will, with its first ARP Request cause all hosts which have an interest in it to have their mappings up dated.

c) Let the delay down the channel be d and the date rate be r. Simple ARQ means that we are only sending one packet at a time, so we can transmit a packet onto the channel in 1000/r and then start another in 2d (waiting for the packet to reach the end and for an acknowledgement to return) in the absence of errors. Lets assume that a corrupt packet is detected as such an a negative acknowledgement is sent immediately when this occurs.
If we assume with an error rate of 10^{-4} that one in ten packets will be corrupt and ignoring errors in acks, then very roughly we will transmit 11 packets for every 10 we want to send.
Applying the same approximations, with an error rate of 10^{-5} we will send 101 packets for every 100 we want to send. So we can just compare 110 transmissions with no coding with 101 transmissions with coding on.
Transmission time no coding 100 microseconds, with coding 200 microseconds, so (times in microseconds) for coding on to be better:

$$101\,(200 + 2d) < 110\,(100 + 2d)$$

from which d a little over 500 microseconds (have to divide 9200 by 18) makes coding on better.

p2q2
p11q12

Digital Electronics

~~Question 1~~

~~a) Inputs: req1, req2, busy (optional)~~
~~Outputs: grant1, grant2~~
~~b) Obvious policies are round robin and strict priority but the latter arguable requires no state about previous requests. So round robin and a hogging policy would be better~~
~~c) Straightforward; eg round robin requires four states to remember who last had the resource and whether they currently have it or not.~~
~~d) Follows from c)~~

~~Question 2~~

~~a) Inputs x0,x1,..., x7, control inputs a,b,c, output z.~~

~~z = abc x7 + ab NOT (c) x6 + ... + NOT (a) NOT(b) NOT (c) x0~~

~~b) Build a tree with 8 first stage 8:1 multiplexors producing the inputs to a second stage multiplexor. Use the first three control inputs on all of the first stage multiplexors, the second three control inputs on the second stage multiplexor.~~
~~c) Inputs a,b,c, outputs z0,z1,...,z7~~
~~Eg z2 = NOT(a) b NOT(c)~~
~~d) Read only memories have word lines for each location in the memory. A decoder on the address lines to a memory can be used to drive the word lines, ensuring that only the word addressed has its word line asserted.~~