Solution notes

Computer Design 2005 – Paper 5 Question 2 (SWM)

(*a*) Book work.

(*b*) N-105 has no data hazards since all new values can be written back to the register file every clock cycle and will, therefore, be ready on the next clock cycle. However, branch instructions will cause a control hazard. This design uses delayed branches to resolve the hazard (i.e. the hazard is indicated in the programmer's model).

The ARM9 processor has data hazards since the execute and memory access stages can both produce results which will not be immediately written back to the register file. Feed forward (bypass) paths can be used to resolve some of the hazards. However, a data hazard caused by load instruction can only be resolved by stalling the pipeline. The ARM9 pipeline also exhibits a control hazard on branches, but the hazard is removed by flushing the pipeline (i.e. the hazard is not apparent in the programmer's model).

(*c*) Book work.

(*d*) A TLB is a translation look-aside buffer. It caches recent virtual to physical address translations and associated protection information.

(*e*) A TLB miss means that a TLB entry needs to be found from the translation table in main memory. This is performed by the hardware on ARM processors, so it can be handled like a load miss. But on most processors an exception is raised which causes a content switch to the operating system which then performs the translation lookup before restoring the application. This exception process is a control hazard (see earlier description for the impact of a control hazard on the pipeline).

This material is covered in lectures 9, 10, 14 and 15.