SHD 2004

a) 512×512 transmit elements $= 2^9 \times 2^9$

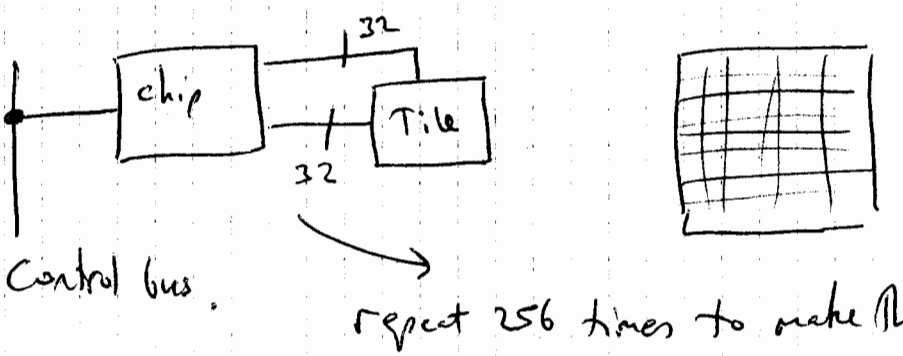
100 pin chip — use 32×32 scan multiplex = 64 pins.

Total number of chips $= 2^9 \times 2^9 / 2^5 \times 2^5 = 2^4 \times 2^4$

$= 16 \times 16$ sub arrays

$= 256$ chips.

Each chip does a scan mpx of a sub array $2^5 \times 2^5$ tile.



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b) Each chip is going to deliver 1024 bits of info to each of 64 wires $1024 \times 1\mu s > 1ms$

So 64 Kbit = 8 K byte.

The data will be totally raw — just the values to go out of the rows and cols. This is more flexible than having hardwired scanners.

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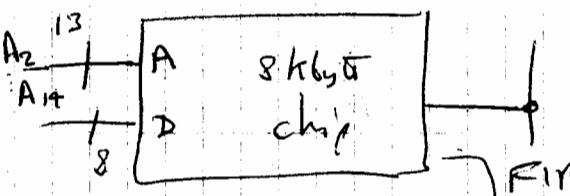
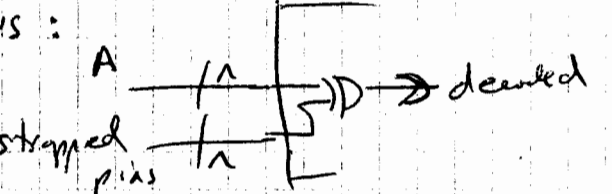
c) Suppose A32, D32 control CPU, like ARM

Each chip could have A13 D8 and a = 21 pins



Need 512 chips for 6-Th arrays. Wire 4 chips in each word, so need to address decode $512/4 = 128$ — another 7 address lines

→ could feed some of these in on A_{14} to A_{20} or some other pins to help the decode process:



Also, likely to need a control and status registers in each chip?

d) SHD 2004 continued