## SOLUTION NOTES

### Digital Communication II 2002 Paper 8 Question 3 (IAP)

($a$) Current generation routers use "smart" line cards attached via point to point connections to a space division switch fabric. There may also be a controller CPU card which performs control-plane functions such as calculating forwarding tables and distributing them to line cards.

When a packet is received, the line card will verify the header checksum, and check whether the packet has any kind of strange header (e.g. options) that can't be handled in hardware. Next, an IP destination address lookup is performed, typically using a 24-8 direct lookup trie. The 24 msb's of the address are used to index a $2^24$ entry table. The table indicates whether a longer prefix lookup is necessary, or in the common case, returns information about which output port and line card the packet should be sent to. The router may also support more advanced "layter4" routeing and firewall functions.

The packet is then queued for transmission across the fabric. A "virtual output buffered" design is likely to be used to reduce the blocking potential of input buffered designs while avoiding the wiring impracticality of output buffered designs. Each input port contains a virtual queue per output port. Each queue containing packets indicates to the arbiter that it is has data to send to that output port. The arbiter's job is to maximise fabric utilization by granting one non-conflicting request to as many input ports as possible. Because each virtual queue is FIFO order, data belonging to the same flow does not re-order.

Scheduling the fabric is typically easier if it is done in "rounds" in which a fixed size chunk of data is transferred. Hence for an IP router, simple hardware may be required to segment packets at the input port and then reassemble them at the output port. The output port will have to maintain a reassembly buffer for each input port.

The virtual queues in front of the fabric may be implemented with a combination of DRAM and SRAM, DRAM providing the necessary capacity (one b/w delay product), with SRAM accommodating the ends of the queue where more rapid random access is required.

The outport port will contain another buffer to match the fabric rate to to the line rate, but this is usually a simple FIFO queue. The output port may also be responsible for decrementing the TTL and rewriting the header CRC (though sometimes the input side does this).

Line cards contain MAC and PHY components for the relevant link technology.

(*b*) The overall design of an ATM switch and router is quite similar except:

- the ATM switch does not need the IP address lookup logic. A simple SRAM table indexed by VPI or VCI will suffice. This is fortunate as the small cell size means these lookups are frequent (though routers should deal with the potential for lots of small packets e.g. voice over IP too).
- the ATM switch requires no exception path for spotting and dealing with packets that can not be dealt with by the forwarding hardware.
- Routers often schedule their switch fabrics in terms of fixed size slots anyway, so there is no major difference here. ATM cells are likely to be slightly smaller though, and if complex fabric arbitration logic is used it could conceivably put pressure on its design.
- ATM switches are typically expected to support "QoS" functions so require multiple priority queues, and potentially hardware to perform traffic shaping/policing.
- Modern ATM switches are expected to support ABR, requiring hardware to monitor queues and perform header re-writing to set congestion fields etc.

(*c*) Single channel line rates are currently at 100Gb/s and growing at 70% p.a.

WDM line rates are increasing at 180%p.a.

Meanwhile, routers are improving at about 70% p.a., beating Moore's Law due to improved architectures and the highly parallelizable nature of routeing.

Large DRAM buffer memories are a major component of most routers. Although data rates are improving, DRAM access latencies are increasing very slowly in comparison (7%p.a.), which is leading to requirements for complex hybrid SRAM / DRAM queues.