Answer for Digital Electronics Paper 2 Question 3 2005

SWM

(a)

E	G	F'
0	0	0
0	1	0
1	0	1
1	1	F

This is an RS flip-flop with inverted inputs

$E = \overline{R}$

$G = \overline{S}$

$F = Q$

(b)

H	J	K'
0	0	0
0	1	k
1	0	1
1	1	k

ie

H	J	K'
D	0	D
x	1	K

This is a level sensitive D-latch

$H = D$ (data)

$J = \overline{E}$ (enable)

$K = Q$ (output)

(c)

L	M	N'
0	0	0
0	1	N
1	0	N
1	1	1

This is a Muller C-element

The inputs L & M are often called A & B and the output N is often called C

(d) Analysis: label internal nodes of first $\overline{R}\overline{S}$ flip-flop V & W (V on top)

When $Q = 0 \Rightarrow$ V & W are memorised, $S = V$, $T = W$

$Q = 1 \Rightarrow$ S & T are memorised, $V = P.T$, $W = R.S$

so inputs P & R influence the output on the falling edge of Q

Q = clock

if $S = Q$ & $T = \overline{Q}$

then $P = J$

$Q = K$

This is a JK flip-flop

P	R	Q	S	T
0	0	↓	S	T
0	1	↓	0	1
1	0	↓	1	0
1	1	↓	T	S
x	x	0	S	T
x	x	1	S	T

$= \overline{S}, \overline{T}$