VLSI design – question A

PR — VLSI Design

Sketch the circuit of a dynamic CMOS gate controlled by a clock φ that precharges when φ = 0 and evaluates the function $\overline{A + B \cdot C}$ when φ = 1. [4 marks]

Explain how it works and describe two advantages and two disadvantages when compared with static CMOS. [6 marks]

Present two ways of designing cascaded logic in dynamic CMOS and explain how they work. [2×4 marks]

Present a further modification to the circuit so that its output is retained when the clock stops. [2 marks]

Solution

[4]

Precharge output to 1, evaluate low or leave alone. [2]
Smaller, faster rise time. [2]
Signal only available half the time, minimum clock speed, internal race. [2]

Domino: invertor on output [4]
NORA: alternate p- and n-type stages [4]

Static feedback inverter on output of Domino circuit. [2]

This relates to the part of the course covering dynamic logic.