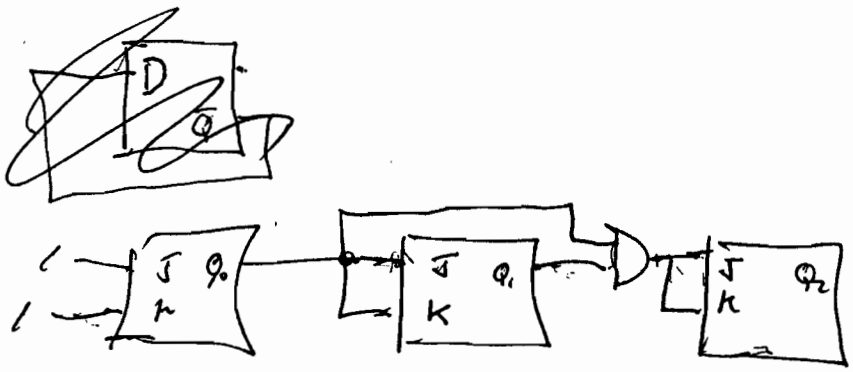
9

p10 q#6 Dig Elec 2000
IML

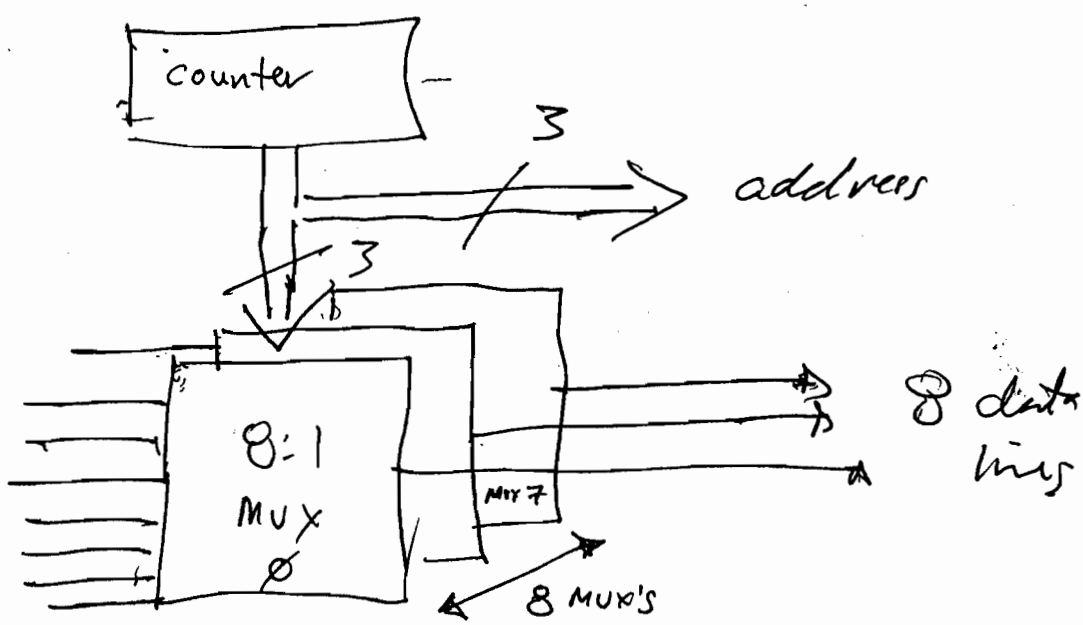
a)



(with common clock)

b) output = $a_2 a_1 a_0 i_7 + a_2 a_1 \bar{a}_0 i_6 + \ldots \bar{a}_2 \bar{a}_1 \bar{a}_0 i_0$

c)



connect bit j of sensor k to k^{th} input of mux j.

d) Have a signal with a transition when count resets to zero. ~~Reading end can't count~~

Instead of sending address lines and clock and this signal. Receive can't count.