1999

p2q3
IML

Question 3

a) Hold time is the time for which the data input(s) have to be held constant after the clock edge. Setup time is the time for which the data inputs(s) have to be held constant prior to the clock edge. The delay time from the clock to the output is the time after the clock edge for which the output is guaranteed not to change (minimum). There is also a maximum time after the clock edge at which time the output is guaranteed to be in its stable state.
b) Minimum delay time must be greater than hold time so that two flip flops in series with a common clock will operate correctly, ie the delay time of the first will ensure that the hold time of the second is not violated.
c) Negative hold times are clearly possible by having delay in the data path. They are good because they allow the minimum delay to be zero.
d) Straightforward, eg:
   i) xNOT(y) + xNOT(z) + NOT(y)NOT(w)z
   ii) NOT(w)NOT(y) + yw + xy + wzNOT(x)
e) First note that the minterms in f will never combine. (Say a minterm Ax for some expression A and variable x is in f. Ax has k variables true. ANOT(x) cannot be in f since it has only k-1 variables true. So all we need is the number of minterms in f which is clearly n chose k.

Tiny questions

1. This is a CMOS Nand gate.
2. ab + NOT(a)NOT(b)