1999

P7 & R
PR

# VLSI Design

## *Question 1*

Describe how a collection of Boolean functions expressed as the sum of products of a given set of input signals can be implemented as a programmable logic array in nMOS. Illustrate your example by showing the stick diagram layout for the following pair of functions:

F = A.B + B'.C + C'.A'
G = C.A + A'.B + B'.C'

[It is not necessary to expand the full detail of any invertors used in the circuit.] [12 marks]

Explain how the depletion mode pull-up transistors might be replaced in CMOS by:

1. p-channel transistors used as passive pull-ups. [4 marks]
2. dynamic logic based on NORA [4 marks]

[It is not necessary to give the detailed stick diagram for these.]

### Answer

Observe G = A.B' + B.C + C'.A' so the C'A' term can be shared.

Rewrite F = (A'+B')' + (B+C')' + (C+A)' and G = (A'+B)' + (B'+C')' + (C+A)' for an implementation in NOR gates.

Standard picture with three inputs and their inverses, ~~two~~ five min-terms and two final outputs (which will need to be inverted).

p-FETs with their gates tied low as static pull-ups.

AND plane implemented as dynamic NOR pre-charged on $\varphi$=0, OR plane implemented as dynamic OR in p-FETs with inverted inputs pre-charged low on $\varphi$=1.