


(a)  $\frac{1}{10} \times 6 = 0.6$

- (a) (i) Devices (and humans) operate far more slowly than processors.  
eg. Many millions of instructions can be executed while a character is being typed.

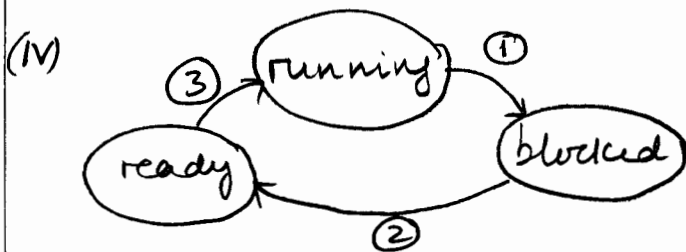
(ii) UART:   
typical registers. data-in status data-out control...includes interrupt enable.

(ii) The software checks the status bits in the UART periodically

- is there a character in data-in?
- is data-out free for the next output character?

checking period - likely to cycle around all polled devices and be time-driven.

- (iii) The UART sends an interrupt signal to the processor - recorded in a CPU register. When this becomes of highest priority (c.f. interrupt level at which CPU is executing) there is an automatic transfer of control to the ISR. PC & CPU status are saved (& restored).



- ① the process must wait until the next char is ready on input or the device is ready on output. Process marked as blocked in PSD and event awaited is recorded. Process removed from ready queue + recorded as awaiting event in event structure (system-dep.)

- ② character (or device) ready + VART signal interrupt. ISK records process status as ready in PSD and adds process to ready queue.

- ③ OS scheduler selects process to run.

- (b) (i) Independently scheduled processes require access to shared data. The data structures would be corrupted by uncontrolled access.

- (ii) A process acquires access to the buffer then finds it cannot proceed  
eg. buffer full on input - driver waits for app. to remove  
eg. " " " output - app. " " driver " "  
eg. buffer empty on output - driver waits for app. to insert  
" " " " - app. " " driver " "

- (iii) The driver first acquires buffer-lock then tests the state of the buffer. If it finds it cannot proceed it Waits for the required condition but does not first release buffer-lock.

DEADLOCK - both processes are blocked indefinitely.

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The buffer lock/unlock should be around the read + write only.