p9q2
PR

## Solution VLSI 2003

Sum $s_i = a_i + b_i + c_i$
Carry out $c_{i+1} = a_i\, b_i + a_i\, c_i + b_i\, c_i$

Carry-skip breaks the adder into $b$ blocks of $k$ bits each. Ripple carry is used inside each block. A carry skip signal for each block is calculated as the product of the individual propagate signals:
$p_i = a_i + b_i$
$S_{i-k+1,i} = p_{i-k+1}\, p_{i-k+2} \ldots p_i$
Carry out of each block is the sum of the ripple carry from within the block and the product of the carry-in with the skip signal for the block.

Delay for ripple carry is $n\,\tau$.

Delay for ripple carry out of lowest block is $k\,\tau$, delay for carry through $(b-2)$ middle blocks is $(b-2)\,\tau$, delay for most significant bit of sum is further $k\,\tau$. So delay to sum is $(2k+b-2)\,\tau$ and delay to carry out is $(k+b-1)\,\tau$.

Assuming $k > 1$, the sum is the critical delay. $T = (2k+b-2)\,\tau = (2k+n/k-2)\,\tau$ which is minimized when $k \approx \sqrt{(n/2)}$.

Variably sized blocks are smaller for the low order bits to reduce delay in generating ripple carry out of the blocks, large in the middle and smaller again for the high order bits to reduce delay in rippling carry in to calculate the sum. To a first approximation the blocks should be 1 2 3 4 5 … 5 4 3 2 1 long.

Fixed blocks should be 5-6 bits long, so the adder would divide as $5 + 9\times6 + 5$, giving a total delay of $(5+9+5)\,\tau = 19\,\tau$. Variably sized blocks would ramp in size from 1 up to 8 in the middle, giving a total delay of $15\,\tau$.

$S_{0,15} = S_{0,3}\, S_{4,7}\, S_{8,11}\, S_{12,15}$.

$c_4$ is generated after $4\tau$ and $c_8$ is available at $5\tau$. Then $c_{24}$ is available at $6\tau$, $c_{40}$ at $7\tau$ and $c_{56}$ at $8\tau$ using the higher level skips. $c_{60}$ is available at $9\tau$, so the top bit of the sum is available after $13\tau$.

*The question relates to the part of the course on adder design. The last part is hard, requiring synthesis of ideas, and should be marked generously.*