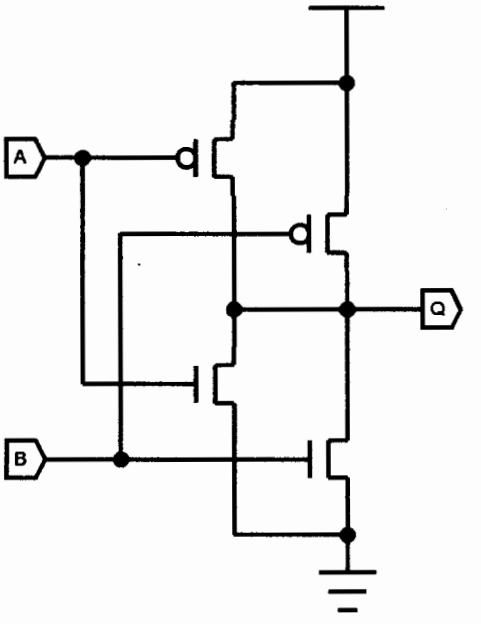
VLSI design – question A

(a) Sketch the circuit of a 2-input NOR gate in static CMOS, and explain how it works. [4 marks]

Johnson's alternative design has the following circuit:



(b) Explain how it works. [4 marks]

(c) Correct operation relies on careful choice of the transistor sizes. Assuming that a conducting p-channel has a resistance γ times that of a similarly sized n-channel, calculate suitable widths for the transistors, and explain the reasons for their values. [2 marks]

(d) Calculate the logical effort and parasitic delay for both designs when $\gamma = 2$. [10 marks]

Solution

and that the threshold voltage is ½ the operating voltage,

(a) Circuit [2]
Explanation [2]

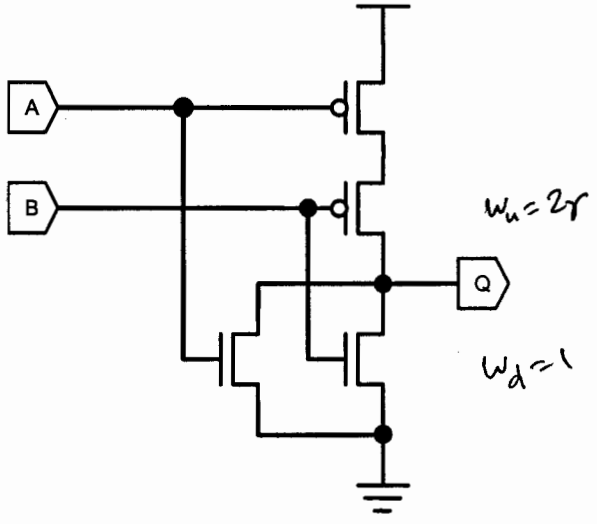
(b) Four input patterns [4×1]

Require $R_u:R_d = 4:1$ when the inputs differ. So $w_u:w_d = \gamma:4$. [2]

Static NOR has $w_u = 2\gamma$ and $w_d = 1$, so $g = (2\gamma+1)/(\gamma+1) =$ ~~5/6~~, 5/3. [2]
and $p =$ ~~$(4\gamma+2)/(\gamma+1) = 9/3 = 3$~~ $(2\gamma+2)/(\gamma+1) = 2$ [2]
Johnson NOR has $w_d=4/3$ as in pseudo-nMOS, so $w_u=\gamma/3$ [1]
and $g_d = (\gamma+4)/3(\gamma+1)$ [1]
But rising output uses both pull-ups so $g_u = 3g_d/2 = (\gamma+4)/2(\gamma+1)$ [1]
so $g = (g_u+g_d)/2 = 5(\gamma+4)/12(\gamma+1) = 5/6$ [1]
and $p = 2(\gamma+4)/3(\gamma+1) = 4/3$ [2]

This relates to the parts of the course covering logic design and logical effort.

(a) A 2-input CMOS NOR gate can be made with two n-type pull-down transistors in parallel and two p-type transistors in series as an active pull-up:



[2]

The complementary Boolean circuits in the pull-up and pull-down networks give the technology its name. When either A or B is high, the pull-down circuit conducts and the pull-up does not. When both A and B are low, the pull-up circuit conducts and the pull-down does not. [2]

(b) In Johnson's circuit, when both A and B are high, the pull-down circuit conducts and the pull-up does not. When both A and B are low, the pull-up circuit conducts and the pull-down does not. If A and B differ, there will be one pFET conducting in the pull-up and one nFET conducting in the pull-down. The output Q will have a voltage determined by the relative resistances of the conducting n- and p-channels. If the p-channel has four times the resistance of the n-channel, the voltage at Q will fall to one fifth of the supply voltage, which should be sufficiently low to be interpreted correctly be any ensuing logic. [4]