SOLUTION NOTES FOR EXAMINERS AND SUPERVISORS ONLY

Computer Design 2000 Paper 6 Question 2 (SWM)

(*a*) "MIPS is an accurate measure for comparing performance among computers" is a fallacy because the number of instructions per second does not indicate the amount of work being undertaken. Some instruction sets only provide very simple operations which can be executed quickly but many instructions are required to complete a task. On the other hand, some instruction sets have more complex instructions which take more time to execute but which perform more work per instruction.

(*b*) "A benchmark is a typical program which accurately predicts the performance of all other applications." This is clearly a fallacy since different applications have very different processing and I/O requirements. For example, an application writing a CD will be largely I/O bound where as a statistical analysis program might be memory or processor bound.

(*c*) "Complex instruction set computers minimise the semantic gap between machine code and high-level languages, thereby making applications run more quickly."

A quantitative approach to processor design indicates that the common case should be made fast. Complex instruction sets are difficult to decode and execute so many common simple operations are not executed efficiently and quickly. Thus, the danger with CISCs is that the performance of the common case will be sacrificed by the need to execute "cleaver" instructions which are infrequently used in practice.

(*d*) "Data caches always improve processor throughput."

Data caches only work efficiently if cache predictors (usually temporal and spatial locality) are efficient. If data isn't reused (e.g. in the case of manipulating video streams) then a large proportion of memory accesses will cause cache misses. On a miss, checking the cache before accessing memory is more expensive than just accessing the memory directly. Thus, data caches don't always improve performance.