

~~SRAM chips are not used.~~

Structured Hardware Design

Answer:

4 MARKS

2005

p2q1a
DTG

$$\begin{aligned} 1 \text{ Mbyte} &= 2^{20} \text{ locations of 8 bits} \\ &= 2^{17} \text{ locations of } 2^3 \times 8 \text{ bits} \end{aligned}$$

32K x 8 SRAM has 15 address lines, 2^{15} locations

Need array 8 chips wide, 4 chips long.

1p

1p

~~1p~~

