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MJCG

Solution notes for SV2.1 2000

DFF(q,d,clk,ce,ar,spare) defines q to be F (false) at time 0.
Whenever there is a posiyive edge on clk or on ar, the value
of ar is tested and if true then q is set to false at the end of the
edge. If ar is false, then ce is tested and if it is true d is copied
into q, otherwise q retains its value. The port spare is not used.

Circuits are modelled by representing each component by a predicate on the values of its inputs and outputs (ports). For example D(x,y) would represent a device with two ports, x and y, and the definition of D would map to true exactly those (x,y) that could be observed as values at the ports. Logic variables are used to name wires and connection is indicated by coincidence of wire names (a diagram of an example would help). A circuit consisting of several components connected together is represented by the conjunction of formulae (e.g. D(x,y)) for each component. Hiding (internalisation) is represented by existential quantification.

The device D(q,d,clk) consists of DFF(q,d,clk,ce,ar,spare) with
ce connected to power and ar to ground and spare hidden. The
formula corresponding to this is:

```
  D(q,d,clk) = ?ce ar spare. Pwr(ce) /\ Gnd(ar) /\ DFF(q,d,clk,ce,ar,spare)

Assuming  Pwr ce  =  All t. ce t = T
          Gnd ar  =  All t. ar t = F
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then routine (bookwork) calculations show:

```
  D(q, d, clk)
   =  (q 0 = F)
      /\
      !t. if ((rise clk t) \/ F)
            then (if F
                    then q(t+1) = F
                    else if T then q(t+1) = d t else q(t+1) = q t)
            else (q(t+1) = q t)
   =  (q 0 = F)
      /\
      !t. if rise clk t then q(t+1) = d t else q(t+1) = q t
```