VLSI design – question B

(a) Sketch designs for memory cells for:

- (i) Read-only memory
- (ii) Static memory
- (iii) Dynamic memory using standard CMOS
- (iv) Dynamic memory for dense layout [4×3 marks]

(b) Compare the designs in terms of speed, size, power consumption. [6 marks]

(c) What further factors affect the comparison as feature sizes decrease? [2 marks]

Solution

Bookwork [4×3]

	Speed	Size	Power
ROM	Fast	Small	Low
Static	Fast	Large	High
Dynamic	Medium	Medium	Medium
Dense	Slow	Small	High

[6]

The 'memory gap' between the speed of a processor and its main memory widens.
The number of electrons representing a bit becomes very low. [2]

This relates to the parts of the course covering memory design and fundamental limitations.

The actual exam question was rather different from this suggestion.

(a) Asked for stick diagrams.
Marks for • storage
• orthogonal control and data lines
• storing 0/1 (in (i)), and read/write (in others)

(b) Asked for extensions to multi-port read versions of (ii) & (iii)
One mark each for idea and implementation.
and reasons why (iv) would not extend
Two marks for limited amount of charge.

(c) Accepted other trends such as wire capacitance.