Digital Electronics Paper 1 Question 2 2005

p10q1
SWM

Computer Science Tripos Part II (General) 2005

Paper 10 Question 1

SWM — Digital Electronics

(a) book work 3 of 3

(b) $C_1 = A_0 B_0 + A_0 C_0 + B_0 C_0$ 3 of 6

$S_0 = A_0 B_0 C_0 + A_0 \bar{B}_0 \bar{C}_0 + \bar{A}_0 B_0 \bar{C}_0 + \bar{A}_0 \bar{B}_0 C_0$ 3 of 6

(c) $S_0 = A_0 \oplus B_0 \oplus C_0$ 2 of 2

(d) $C_3 = A_2 B_2 + (A_2 + B_2) C_2$

$= A_2 B_2 + (A_2 + B_2)(A_1 B_1 + (A_1 + B_1) C_1)$

$= A_2 B_2 + (A_2 + B_2)[A_1 B_1 + (A_1 + B_1)(A_0 B_0 + A_0 C_0 + B_0 C_0)]$

$= A_2 B_2 + A_2 A_1 B_1 + A_2 A_1 A_0 B_0 + A_2 A_1 A_0 C_0 + A_2 A_1 B_0 C_0$
$+ A_2 B_1 A_0 B_0 + A_2 B_1 A_0 C_0 + A_2 B_1 B_0 C_0$
$+ B_2 A_1 B_1 + B_2 A_1 A_0 B_0 + B_2 A_1 A_0 C_0 + B_2 A_1 B_0 C_0$
$+ B_2 B_1 A_0 B_0 + B_2 B_1 A_0 C_0 + B_2 B_1 B_0 C_0$ 6 of 6

will also accept the case where $C_0 = 0$ since the question asked for C_3 in terms of A_2 & B_2

(e) Implementing C_3 already requires multi-level logic since the 15 input OR gate required is not typically found in a digital logic family. We can also see that the number of terms is growing rapidly. The sum-of-products form for C_8 will be far too large to implement in 2-level logic. Therefore a multi-level logic implementation is essential. 3 of 3

This material is covered in lectures 1 to 4.