VLSI design – question B

Sketch designs for an n-input NAND gate in CMOS using:

- static CMOS
- dynamic CMOS
- pseudo-nMOS [3×2 marks]

Assuming that a conducting p-channel has a resistance γ times that of a similarly sized n-channel, annotate your circuit diagrams with suitable widths for the transistors, and explain the reasons for their values. [3×2 marks]

Calculate the logical effort and the parasitic delay of each design. [3×2 marks]

Which is likely to be fastest for the case when $n = 4$ and $\gamma = 3$? What difference would it make if the circuit were driving a large capacitative load? [2 marks]

Solution

[3×2]

Static: pull-ups each γ wide in parallel, pull-downs each n wide in series. [2]
Dynamic: pull-up $\gamma/2$ wide, pull-downs and evaluate each $n+1$ wide in series [2]
Pseudo-nMOS: pull-up $\gamma/3$, pull-downs each $4n/3$ wide in series. [2]

Static: $g = (\gamma+n)/(\gamma+1)$, $p = (n\gamma+n)/(\gamma+1) = n$. [2]
Dynamic: $g = (n+1)/(\gamma+1)$, $p = (\gamma/2+n+1)/(\gamma+1)$. [2]
Pseudo-nMOS: rising $g = 4n/(\gamma+1)$, falling $g = 4n/3(\gamma+1)$, average $g = 8n/3(\gamma+1)$, $p = (4n+\gamma)/3(\gamma+1)$. [2]

Dynamic CMOS has the lowest unitless delay. It also has the lowest effort delay. [2]

This relates to the part of the course covering logical effort.