ECAD (2004) Paper 3 Question 2 (SWM)

Sketch Answer

(a) Three D-type flip-flops are required to store the state bits s[2:0]. The c input will provide the clock to these flip-flops. The r input will be connected to the asynchronous reset on the flip-flops.

(b) Whenever r=1, the state will be reset to 0. I will not include this on my diagram. State transition diagram.... simple - see state transition table in the next part.

(c) Let's start with a state transition table:

	Inputs			Outputs		
a	s[2]	s[1]	s[0]	s[2]'	s[1]'	s[0]'
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	0	0	1
0	0	1	1	0	1	0
0	1	0	0	0	1	1
0	1	0	1	1	0	0
0	1	1	0	1	0	1
0	1	1	1	1	1	0
1	0	0	0	0	0	1
1	0	0	1	0	1	0
1	0	1	0	0	1	1
1	0	1	1	1	0	0
1	1	0	0	1	0	1
1	1	0	1	1	1	0
1	1	1	0	1	1	1
1	1	1	1	1	1	1

The K-map for next state s[0]:

		s[1]			
		s[0]			
		0	0	0	1
	s[3]	1	0	0	1
a		1	0	1	1
		1	0	0	1

From this we can see that $s'_0 = \overline{s_0}.s_1 + \overline{s_1}.s_2 + \overline{s_0}.a + s_1.s_2.a$

The K-map for next state s[1]:

		s[1]		
		s[0]		
	s[3]	0	0	1	0
		1	0	1	0
a		0	1	1	1
		0	1	0	1

From this we can see that there are three possibilities a minimum sum of products for s_1':

1. $s_1' = s_0.s_1.\overline{a} + s_0.\overline{s_1}.a + \overline{s_0}.s_1.a + \overline{s_0}.\overline{s_1}.s_2.\overline{a} + s_0.s_2.a$
2. $s_1' = s_0.s_1.\overline{a} + s_0.\overline{s_1}.a + \overline{s_0}.a.s_1 + \overline{s_0}.\overline{s_1}.s_2.\overline{a} + s_1.s_2.a$
3. $s_1' = s_0.s_1.\overline{a} + s_0.\overline{s_1}.a + \overline{s_0}.a.s_1 + \overline{s_0}.\overline{s_1}.s_2.\overline{a} + s_0.s_1.s_2$

The K-map for next state s[2]:

		s[1]		
		s[0]		
	s[3]	0	0	0	0
		0	1	1	1
a		1	1	1	1
		0	0	1	0

From this we can see that $s_2' = s_0.s_2 + s_1.s_2 + s_2.a + s_0.s_1.a$