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DJG

2001 Examination Question - Structured Hardware Design

Question:

a) Explain the basic operation of the 'parallel port' found on most computers. Include a description of the main signals and give their purpose. [4 Marks]

b) Similarly, explain the basic operation of the RS232 'serial port' found on most computers. [4 Marks]

c) What sets the max and min rate of transfer of data for each type of port? What happens if the receiver cannot consume data as quickly as the source would like to send it ? [4 Marks]

d) Both types of port allow data to flow from one piece of equipment to another and these items will normally have independent clock domains. How can synchronization be achieved ? [4 Marks]

e) When might it be sensible to communicate data using a large number of wires in parallel but with each one behaving more like an individual serial port ? [4 Marks]

Acceptable Answer For More Than Full Marks (typed in 10 minutes)

a) The parallel port has 8 data wire and three control wires called strobe, busy and ack. The basic version of the port is unidirectional and the sender places data on the 8 lines and asserts strobe. When the receiver asserts ack, the data has been read and can be removed. The sender is not allowed to send any more data while the receiver asserts busy.

b) The serial port consists of only one data wire and both the source and destination must have first somehow agreed on a common baud period, such as 1/9600th of a second. The line is a one when idle and the source sends data a word at a time by first sending a start bit of duration one baud interval and value zero and then the bits of the word, one after the next, in successive baud periods. A word is often 8 bits (i.e. a byte). Sometimes a parity bit is appended. A stop bit of one follows before the next start bit can start.

c) In the parallel port, the busy line can be used to slow down the sender. The maximum speed is determined by how fast the signals can swing, the skew in the cable and the delays at each end.

For the serial port, the maximum speed is set simply by the agreed baud rate and the receiver quenches the source either be deasserting the hardware flow control lines or using a software Xon / Xoff protocol that uses up two of the possible data values that can be sent on the reverse link.

d) The serial receiver port normally samples the input line using a high quality flip-flop at 16 times the baud rate. After detecting the start or the start bit it can wait 24 clock times (1.5 baud) before sampling the first data bit, and then counting 16 steps further each time. There is a sure risk of metastability in the sampling flip-flop, but this is the only place and hence a good quality flip-flop should be used.

The parallel port has the strobe and acknowledge lines to qualify the data on the actual data lines, so there is no problem of synchronisation with these. Again, good quality flip-flops are needed to process the handshake lines at each end.

e) When a large number of wires need to be used at very high rates, such as the databus to a large RAM array, the skew in the lines and drivers can mean that the data arrives perhaps a whole clock tick earlier on some lines than on others. Handshake lines can be used to control the overall operation, but the bits can be transferred using serial techniques, with each wire defining its own data arrival window. (For mega credit, one could add: Fully synchronous, phase-coherent teqchniques using PLLs or similar would have to be used rather than the simple sampling discussed above for the serial port receiver).