Dy au Digital Electronics 2003 IML pzg3

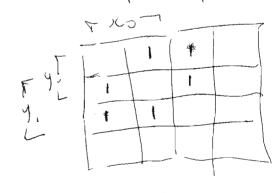
(0)

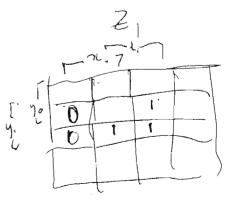
$$Z_{3} = \chi_{1} \chi_{0} y_{1} y_{0}$$

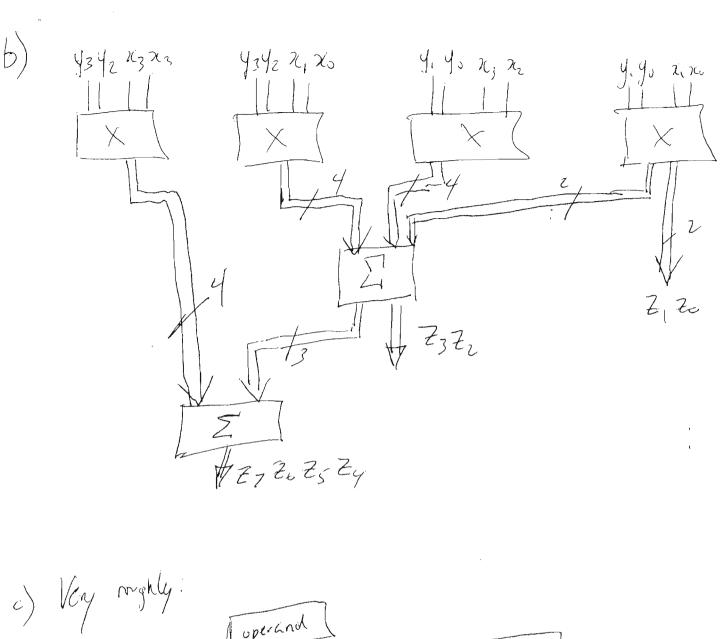
$$Z_{3} = \chi_{0} y_{0}$$

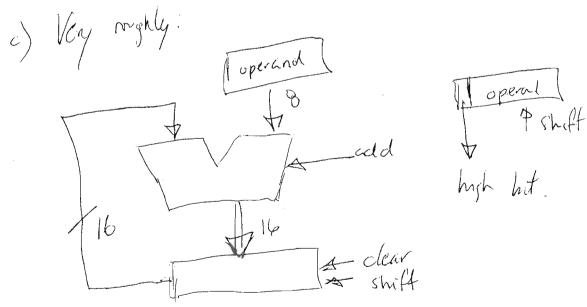
$$Z_{1} = y_{1} \overline{\chi}_{1} \chi_{0} + y_{1} \overline{y}_{0} \chi_{0} + y_{1} \overline{\chi}_{0} \chi_{1}$$

$$+ \overline{y}_{1} y_{0} \chi_{1} + \overline{y}_{0} \overline{\chi}_{0} \chi_{1}$$









A done.

Start clear

Cach state: add = high bit, shift each reg.

d) Very much like i, but need comparator to dead if to subtract.

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