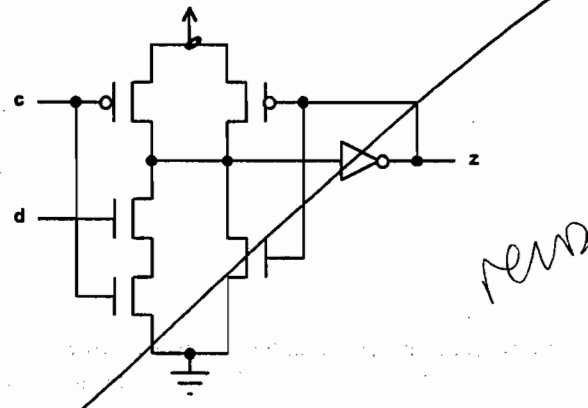
Question B

Give transistor level designs for 2-input NAND gates using static and dynamic CMOS, explaining how the latter is controlled by a clock. [10 marks]

Comment on the relative merits of the two methods for evaluating more complicated combinatorial functions, including transistor count, wiring complexity, speed and implications for cascaded logic. [5 marks]

Consider the following circuit for a set-reset latch in a form of Domino logic:



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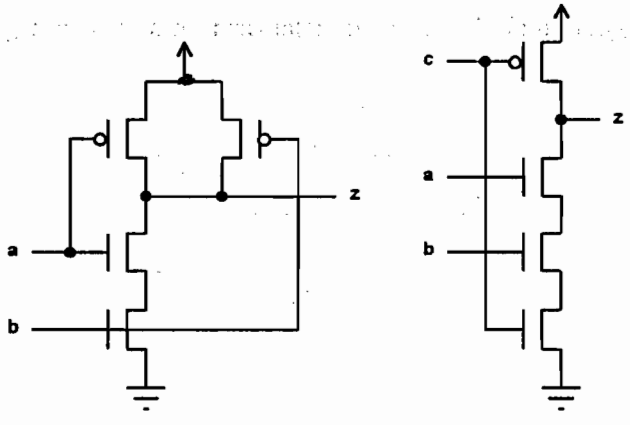
Explain its operation and specify carefully the sense of the input and output signals. [5 marks]

Answer



Dynamic logic precharges when the clock, *c*, is low and evaluates when it is high.

Replace the two transistors implementing the AND function by an arbitrary piece of combinational logic. For *n* inputs, static uses $2n$ transistors and dynamic $n+2$ with simpler wiring. Dynamic logic is generally faster, but the output is only available when *c* is high. The dynamic version has problems with an internal race when gates are cascaded, requiring the use of Domino or Nora logic.

When *c* is low, the output is reset low. When *c* is high, raising *d* sets the output high. The invertor and two additional transistors provide weak feed-back to retain the state.