Digital Electronics 2004 – Paper 2 Question 3 (SWM)

This question covers lectures:

1 – binary
2 – Boolean algebra and addition
3 – logic minimisation
4 – more on adders
5 – flip-flops
6 – sync state machines

Sketch Answer

First, let's start with a state transition table:

Inputs				Outputs		
A	D2	D1	D0	D2'	D1'	D0'
0	0	0	0	1	1	1
0	0	0	1	0	0	0
0	0	1	0	0	0	1
0	0	1	1	0	1	0
0	1	0	0	0	1	1
0	1	0	1	1	0	0
0	1	1	0	1	0	1
0	1	1	1	1	1	0
1	0	0	0	0	0	1
1	0	0	1	0	1	0
1	0	1	0	0	1	1
1	0	1	1	1	0	0
1	1	0	0	1	0	1
1	1	0	1	1	1	0
1	1	1	0	1	1	1
1	1	1	1	0	0	0

[4 marks]

Equation for D0 One can see from the state transition table that whatever the control input is, D0'= D0

[4 marks]

Equation for D1 This is a little more difficult. We could go back to basic adder designs, or simply determine the equation from a K-map vis:

		D1			
		D0			
		1	0	1	0
	D2	1	0	1	0
A		0	1	0	1
		0	1	0	1

From this K-map, it can be seen that $D1' = \overline{D0 \oplus D1 \oplus A}$

[4 marks]

Equation for D2 Similarly, for D2 we could just determine the equation from a K-map:

		D1			
		D0			
		1	0	0	0
	D2	0	1	1	1
A		1	1	0	1
		0	0	1	0

$$
\begin{array}{rcccc}
D2' = & \overline{A} & \overline{D_0} & \overline{D_1} & \overline{D_2} \; + \\
 & \overline{A} & D_0 & D_2 & \; + \\
 & \overline{D_0} & D_1 & D_2 & \; + \\
 & A & \overline{D_1} & D_2 & \; + \\
 & A & D_0 & D_1 & \overline{D_2}
\end{array}
$$

[4 marks]

4 marks for the circuit diagram.