NU1680: Low Cost, None-firmware, High Integration Wireless Power Receiver

1 Feature

- Ultra-simple circuit structure with total only 12pcs components
- Low Cost and very simple application without extra firmware
- I²C programmability
- Integrated Low-Dropout LDO to Provide Regulated Output Programmable V_{out} from 3.5V to 9V with 39mV step
- Or Output V_{out} real-time tracking external Battery Voltage to optimize the efficiency
- Programmable and Configurable FOD gain and offset by I²C or Resisters
- Integrated high-efficiency synchronous rectifier without bootstrap capacitors
- Robust OVP, OCP, SCP and OTP Protection
- 10 Bits ADC for Battery voltage, Output current and temperature measurement
- INT Output for external interrupt
- Small Size with 16-QFN 3.0mm x 3.0mm, 0.5mm pitch

2 Applications

- WPC 5W BPP Compliant Receiver with Maximum 5W Received Power
- Wireless Power Receiver for TWS, Electric Toothbrush, Electric Shaver, E-Cigarette and others Consumer Equipment

3 Descriptions

NU1680 is a highly integrated wireless power receiver, which requires less quantity of surrounding components compared with NU1610. It gives the benefit of the very low total system cost and less PCB area for wireless power receiver solution. Also, since requires no firmware to program, it will much simplify the design effort and consolidate the solution more easily and quickly. It integrates a synchronous rectifier without bootstrap capacitors designed for a high efficiency purpose and low cost. The regulator can provide a wide range regulated voltage from 3.5V to 9V compliable with different applications. Furthermore, it can regulate the output voltage tracking the battery voltage to further lower down the charging system power loss.

NU1680 can conduct communication with a transmitter system through ASK. The communication is compliant with WPC V1.2.4. FOD parameters can be configured by I²C interface or external resisters to pass the FOD test.

NU1680 also support to be connected to a main AP, communicated by I²C interface. It provides external interrupt, ADC value of battery voltage and output current etc.

NU1680 also includes standard protection functions such as overcurrent protection, short-circuit protection, overvoltage protection and thermal shutdown. These provisions further enhance the reliability of the system solution.

The device is housed in a compact 3.0mm×3.0mm QFN package.

Content

4 Pin Configuration and Functions

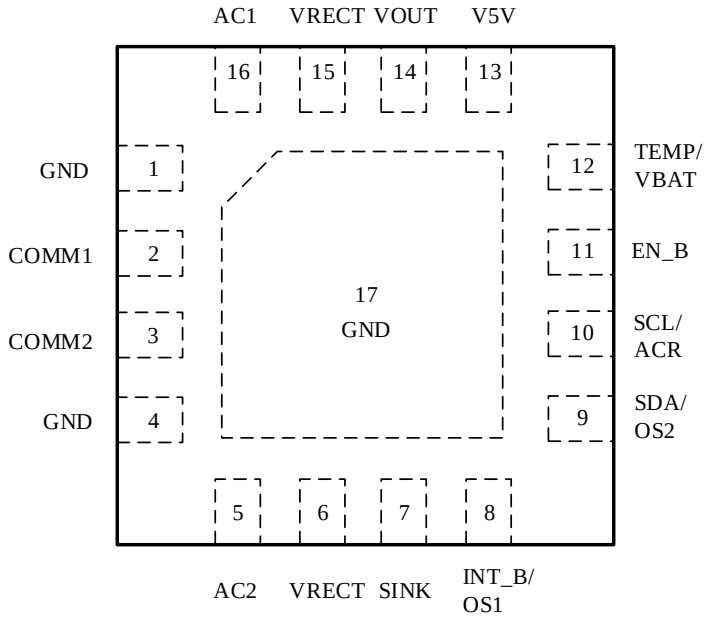


Figure 1. NU1680-QFN Top View

Pin		I/O	Description
Name	No.		
GND	1, 4, 17	GND	System power and analog ground.
COMM1/COMM2	2/3	O	Open-drain output used to communicate with the transmitter. Connect a capacitor between this pin and AC1/AC2.
AC1/AC2	5/16	I	AC input power. Connect to the resonant circuit loop of L and C.
VRECT	6, 15	O	Output of the synchronous rectifier. Connect capacitor between this pin and ground.
SINK	7	O	Open-drain output for controlling the rectifier clamp. Connect a resistor between this pin and the VRECT pin.
INT_B/OS1	8	I/O	Open-drain, active low interrupt output. Pull up to V5V voltage with 10-kΩ resistor. Normally high, the device asserts low to report status and faults. If configured as FOD_RES_MODE, this PIN function as the input of the Offset of FOD parameter at load #0. If not use, connect to ground.
SDA/OS2	9	I/O	I²C data pin. If configured as FOD_RES_MODE, this PIN function as the input of the Offset of FOD parameter at load #1 and #2. Leave it floating if no use.
SCL/ACR	10	I	I²C clock pin. If configured as FOD_RES_MODE, this PIN function as the input of the ACR of FOD parameter. Leave it floating if no use.

EN_B	11	I	A logic high input for power LDO output disable. There is internal pull down, keeping it floating if no use.
TEMP/VBAT	12	I	Temp sensing pin. Connect a R_{25} = 100K, beta = 4250 NTC resistor to ground. Or it can be configured as battery voltage sensing pin to make V_{out} being capable of tracking external Battery voltage. Leave it floating if no use.
V5V	13	O	5V power supply for IC internal use. Connect a typical 1uF/10V capacitor between this pin and ground.
VOUT	14	O	Output pin for load.

5 Specifications

5.1 Absolute Maximum Ratings

Pins	Rating	Units
AC1, AC2, COMM1, COMM2	-0.3~17	V
VRECT, SINK	-0.3~17	V
V5V, SCL/ACR, SCL/OS2, INT_B/OS1, EN_B, TEMP/VBAT	-0.3~6	V
VOUT	-0.3~10	V
Max Current on SINK	500	mA
Max Current on COMM1/2	500	mA
Max RMS Current on AC1/AC2	2	A
Operating Junction Temperature, T_J	-40~125	°C
Ambient Operating Temperature, T_A	-40~85	°C
Storage Temperature, T_{stg}	-55~125	°C

5.2 ESD Ratings

		UNIT
Human Body Model	+/-2000	V
Charged Device Model	+/-500	V

5.3 Package Thermal Ratings

		UNIT
Junction-to-ambient thermal resistance, $R_{\Theta JA}$ (FR4 double layer, 2oz, 1.9mm*1.9mm size of copper on IC layer and 8mm*8mm size of copper on another side)	38	°C/W

5.4 Electrical Characteristics

V_{RECT}=5.2V, T_j=-40 °C to 125°C (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power supply						
$V_{UVLO\_RECT\_RISE}$	V_{RECT} Under-voltage lock out threshold	V_{RECT} ramps up	2.9	3.05	3.2	V
$V_{UVLO\_RECT\_FALL}$		V_{RECT} ramps down		2.83		V
V_{UVLO_V5V}	Under-voltage lock out threshold	V5V ramps up	2.9	3.05	3.2	V
$V_{UVLO\_V5V\_HYS}$	Under-voltage lock out hysteresis voltage	V5V ramps down	80	220	360	mV
I_{Q_RECT}	Quiescent operating current into V_{RECT}	EN_B=low, no switching		2		mA
V5V LDO						
V_{V5V}	5V supplier	I_{V5V}=10mA	4.6	4.83	5.1	V
I_{V5V}	5V supply current limit	V_{V5V}=4.6V			80	mA
I_{SHORT}	5V short current	V_{V5V}=1V			360	mA
OUTPUT REGULATION (POWER LDO)						
V_{OUT}	Output voltage range		3.5		9	V
V_{OUT_STEP}	Output voltage step	V_{out}=3.5V to 9V		39		mV
V_{OUT_ACC}	Output voltage accuracy	V_{OUT}=5V, I_{OUT}=1mA	4.85	5	5.15	V
V_{OUT_REG}	Output voltage regulation	V_{OUT}=5V, I_{OUT}=1A	-3		3	%
I_{LIM_RANGE}	Current limit range (Sending EPT packet)	V_{OUT}=5V	1.2	1.4	1.6	A
Synchronous Rectifier Bridge						
R_{DSON}	ON impedance of Rectifier MOSFET	VRECT=6V		100		mΩ
TMOT	minimum ON time			350		ns
Protection						
T_{OTP}	Thermal Shut Down	Temp rising threshold		150		°C
T_{OTP_HYS}	Thermal Shut Down hysteresis	Temp falling threshold		25		°C
V_{SC}	Output short protection			1		V

V_{OVP1}	VRECT Low-Level over voltage protection threshold	SINK ON and soft protection	12.1	12.8	13.5	V
V_{OVP1_HYS}	VRECT over voltage recovery hysteresis		0.4	0.6	0.9	V
V_{OVP2}	VRECT High-Level over voltage protection threshold	SINK ON and internal hard protection	14.6	15.4	16.2	V
V_{OVP2_HYS}	VRECT over voltage recovery		6.7	8.5	9.5	V
SINK						
R_{SINK}	Pulldown resistance of SINK pin	I=100mA			7	Ω
I_{LKG_SINK}	SINK pin leakage current	SINK=5.5V	-1		1	μA
EN_B						
V_{IH_ENB}	Input voltage logic high	Input rising	1.5			V
V_{IL_ENB}	Input voltage logic low	Input falling			0.6	V
R_{ENB}	Logic pin input impedance	Pull down to GND		2		MΩ
INT_B/OS1						
V_{OL_INTB}	INT_B/OS1 pin output low	I=1mA			0.2	V
I_{LKG_INT}	INT_B/OS1 leakage current	V=0V and 5V	-1		1	μA
I²C INTERFACE (SCL/ACR, SCL/OS2)						
V_{IH}	Input voltage logic high	Input rising	1.4			V
V_{IL}	Input voltage logic low	Input falling			0.6	V
f_{SCL}	Clock frequency				400	kHz
V_{OL_SDA}	Pull down voltage low level	5mA sink current			0.2	V
I_{LKG_I2C}	Input Leakage Current	V=0V and 5V	-1		1	μA
BIAS Current for FOD parameters configure and Temperature sense						
I_{Bias}	Current flow through pins and resister (TEMP, SDA, SCL/ACR, INT_B/OS1)	Tested on TEMP/VBAT, SDA, SCL/ACR, INT_B/OS1 pins.	3.8	4	4.2	μA

Note: * means performance is guaranteed by design.

6 Register Maps

6.1 General Purpose Registers

Address and Bit	Register Field Name	R/W	Reset or Default	Function and Description
0x00[7:0]	CHIP_ID_H [7:0]	R	0x16	Chip ID information high byte
0x01[7:0]	CHIP_ID_L [7:0]	R	0x80	Chip ID information low byte
0x02[2:0]	CHIP_REV [2:0]	R	0x00	Chip hardware reversion
0x03[7:0]	STATUS [7:0]	R	0x00	Current status
0x03[0]	LDO_ON	R	0	0 = Power LDO OFF; 1 = Power LDO ON
0x03[1]	RECT_ON	R	0	0 = Rectifier MOSFETs disabled; 1 = Rectifier MOSFETs enabled
0x03[2]	Reserved			
0x03[3]	OCP	R	0	0 = None over current occurrence; 1 = Over current occurrence
0x03[4]	OVP2	R	0	0 = None of VRECT over high-level voltage occurrence; 1 = VRECT over high-level voltage occurrence
0x03[5]	OVP1	R	0	0 = None of VRECT over low-level voltage occurrence; 1 = VRECT over low-level voltage occurrence
0x03[6]	OTP	R	0	0 = None of IC junction over temperature occurrence; 1 = IC junction over temperature occurrence
0x03[7]	TEMP	R	0	0 = None of TEMP/VBAT over temperature occurrence; 1 = TEMP/VBAT over temperature occurrence
0x04[4:0]	CONTROL [4:0]	R/W	0x00	Control register
0x04[0]	FORCE_LDO_ON	R/W	0	0 = Normal Power LDO ON/OFF operation; 1 = Force turning on Power LDO regardless of other conditions except FORCE_LDO_OFF=1
0x04[1]	FORCE_RECT_ON	R/W	0	0 = Normal Rectifier MOSFET ON/OFF operation; 1 = Enable Rectifier MOSFETs at any load except FORCE_RECT_OFF=1

0x04[2]	FORCE_LDO_OFF	R/W	0	0 = Normal Power LDO ON/OFF operation; 1 = Force turning off Power LDO regardless of other conditions
0x04[3]	FORCE_RECT_OFF	R/W	0	0 = Rectifier MOSFET ON/OFF depending on FORCE_RECT_ON bit; 1 = Force turning off all four rectifier MOSFETs regardless of other conditions
0x04[4]	FORCE_VBAT_TRK_OFF	R/W	0	0 = Tracking VBAT function depending on MTP_VBAT_TRK_EN in MTP_OPTION; 1 = Turning off the tracking function regardless of MTP_VBAT_TRK_EN.
0x05[7:0]	AP_EPT [7:0]	R/W	0x00	EPT Control register
0x05[0:6]	EPT_MESSAGE	R/W	0	Message content included in EPT packet
0x05[7]	AP_EPT_EN	R/W	0	0 = Disable including the message of EPT_MESSAGE into the EPT package; 1 = Enable including the message of EPT_MESSAGE into the EPT package
0x06[7:0]	INT_FLAG [7:0]	R	0x00	Interrupt and protection event flag register. If AP/MCU get the interrupt signal, read this register first before any operation on other registers. Otherwise this byte will be cleared.
0x06[0]	Reserved.			
0x06[1]	STARTUP_FLAG	R	0	After V5V rise across UVLO, the bit will be set and INT send out. Reading it will clear the bit.
0x06[2]	Reserved.			
0x06[3]	OCP_FLAG	R	0	OCP event set this bit and INT send out, transmit EPT to Tx. Reading it will clear the bit.
0x06[4]	OVP2_FLAG	R	0	OVP2 event set this bit and INT send out, transmit EPT to Tx. Reading it will clear the bit.
0x06[5]	OVP1_FLAG	R	0	OVP1 event set this bit and INT send out, transmit EPT to Tx if MTP_OVP1_EPT_EN = 1. Reading it will clear the bit.
0x06[6]	OTP_FLAG	R	0	OTP (IC die over temperature protection) event set this bit and INT

				send out, transmit EPT to Tx. Reading it will clear the bit.
0x06[7]	TEMP_FLAG	R	0	TEMP/VBAT (sensing external component) over temperature event set this bit and INT send out, transmit EPT to Tx. Reading it will clear the bit.

6.2 Parameter Configure Registers

Address and Bit	Register Field Name	R/W	Reset or Default	Function and Description
0x10 [7:0]	MFG_CODE_H [7:0]	R/W	0x00	Manufacture information high byte
0x11 [7:0]	MFG_CODE_L [7:0]	R/W	0x5C	Manufacture information low byte
0x12 [7:0]	DEVICE_ID_B6 [7:0]	R/W	0x00	Device ID information
0x13 [0:0]	INFO1_LOCK [0:0]	R/W	0x00	Lock bit for OTP program
0x14 [5:0]	MTP_ACR [5:0]	R/W	0x16	Equivalent resister of LC resonant loop (ACR) for FOD parameter. ACR = refer to the design tool.
0x15 [4:0]	MTP_OPTION [4:0]	R/W	0x12	
0x15 [0]	MTP_VBAT_TRK_EN	R/W	0	0 = Disable output tracking VBAT function; 1 = Enable output tracking VBAT function
0x15 [1]	MTP_TEMP_EPT_EN	R/W	1	0 = Disable sending EPT when TEMP/VBAT over temperature; 1 = Enable sending EPT when TEMP/VBAT over temperature
0x15 [2]	MTP_TEMP_LOW_EN	R/W	0	0 = Disable low temperature protection; 1 = Enable low temperature protection
0x15 [3]	MTP_OVP1_EPT_EN	R/W	0	0 = Disable sending EPT when OVP1 occurrence and sending CE more quickly; 1 = Enable sending EPT when OVP1 occurrence
0x15 [4]	MTP_CE_LARGE	R/W	1	0 = Define CE = 0 at (VRECT-VRECT_Target) between [+40mV, -40mV]; 1 = Define CE = 0 at (VRECT-VRECT_Target) between [+80mV, -40mV];
0x16 [1:0]	MTP_VBAT_DELTA [1:0]	R/W	0x00	The difference between V_{out} and the TEMP/VBAT Pin voltage. 00: 500mV 01: 400mV 10: 300mV

				11: 600mV
0x17 [1:0]	MTP_VBAT_LOWLMT [1:0]	R/W	0x00	The minimum limit of V_{out} when using tracking VBAT function. 00: 4.5V 01: 4.3V 10: 4.1V 11: 4.7V
0x18 [3:0]	MTP_OFFSET [3:0]	R/W	0x02	Received power offset for FOD parameter.
0x19	Reserved.			
0x1A	Reserved.			
0x1B	Reserved.			
0x1C [3:0]	MTP_DUMMY [3:0]	R/W	0x03	Dummy load at load #0. Dummy = MTP_DUMMY [3:0] *3.5 mA
0x1D [7:0]	MTP_VOUT_SET [7:0]	R/W	0x7F	V_{out} output set. V_{out} = MTP_VOUT_SET [7:0] * 39.06 mV
0x1E [2:0]	MTP_ILIM_SET [2:0]	R/W	0x00	The limit of over current protection. 000: 1.4A 001: 1.65A 010: 1.1A 011: 0.74A 100: 0.365A 101: 0.45A 110: 0.29A 111: 0.215A
0x1F [1:0]	MTP_TEMP_TH [1:0]	R/W	0x00	If configure this pin as temperature sensing, connect a R_{25} = 100K, beta = 4250 NTC to the PIN of TEMP/VBAT. 00: 80°C 01: 60°C 10: 50°C 11: 42°C
0x20	Reserved.			
0x21 [1:0]	MTP_VDELTA [1:0]	R/W	0x00	Set the difference between V_{rect} and V_{out} at load #2. 00: 200mV 01: 280mV 10: 360mV 11: 150mV
0x22 [1:0]	MTP_VLIGHT [1:0]	R/W	0x00	1. Set the additional difference between V_{rect} and V_{out} at load #0 and #1. So V_{rect} = V_{out} + MTP_VDELTA + MTP_VLIGHT. 00: 2.00V (load #0), 1.00V (load #1) 01: 2.50V (load #0), 1.25V (load #1) 10: 1.00V (load #0), 0.50V (load #1) 11: 0.50V (load #0), 0.25V (load #1)

				2. Threshold and Hysteresis for load state area definition. 00: Load #0 to Load #1: 50mA, Hysteresis 10mA; Load #1 to Load #2: 100mA, Hysteresis 20mA; 01: Load #0 to Load #1: 80mA, Hysteresis 16mA; Load #1 to Load #2: 160mA, Hysteresis 32mA; 10: Load #0 to Load #1: 100mA, Hysteresis 20mA; Load #1 to Load #2: 200mA, Hysteresis 40mA; 11: Load #0 to Load #1: 40mA, Hysteresis 8mA; Load #1 to Load #2: 80mA, Hysteresis 16mA;
0x23 [1:0]	MTP_CE_LIMIT [1:0]	R/W	0x00	The limit of maximum of control error. 00: 50 01: 30 10: 12 11: 100
0x24 [0:0]	INFO2_LOCK [0:0]	R/W	0x00	Lock bit for MTP1 program
0x25 [0:0]	INFO3_LOCK [0:0]	R/W	0x00	Lock bit for MTP2 program
0x72 [7:0]	I2C_OTP_CTRL [7:0]	R/W	0x00	Password for program, only available at test mode. 0x3D: OTP 0x3E: MTP1 0x3F: MTP2

6.3 ADC Channel Registers

Address and Bit	Register Field Name	R/W	Reset or Default	Function and Description
0x30 [1:0]	IOUT_FILT [1:0]	R	0x00	Current of I_{out}

0x31 [7:0]	IOUT_FILT [9:2]	R	0x00	I_{out} = IOUT_FILT [9:0] *1.953 mA
0x32 [1:0]	VBAT_FILT [1:0]	R	0x00	Voltage of TEMP/VBAT V_{BAT} = VBAT_FILT [9:0] *9.766 mV
0x33 [7:0]	VBAT_FILT [9:2]	R	0x00	
0x34 [1:0]	VRECT_FILT [1:0]	R	0x00	Voltage of V_{rect} V_{rect} = VRECT_FILT [9:0] *9.766 mV
0x35 [7:0]	VRECT_FILT [9:2]	R	0x00	
0x36	Reserved.			
0x37	Reserved.			
0x38 [1:0]	TEMP_CONV [1:0]	R	0x00	Resistor of NTC. Internal 4uA going through the TEMP/VBAT Pin. R_{NTC} = TEMP_CONV [9:0] *0.488 KΩ
0x39 [7:0]	TEMP_CONV [9:2]	R	0x00	
0x3A [1:0]	INTB_CONV [1:0]	R	0x00	Configure the offset of FOD at load #0 with internal 4uA going through the INT_B/OS1 Pin during start up. Code_OFFSET = 0.128 *R_INT_B/OS1 (KΩ)
0x3B [7:0]	INTB_CONV [9:2]	R	0x00	
0x3C [1:0]	SDA_CONV [1:0]	R	0x00	Configure the offset of FOD at load #1 and #2 with internal 4uA going through the SDA Pin during start up. Code_OFFSET = 0.128 *R_SDA (KΩ)
0x3D [7:0]	SDA_CONV [9:2]	R	0x00	
0x3E [1:0]	SCL/ACR_CONV [1:0]	R	0x00	Configure the ACR of FOD with internal 4uA going through the SCL/ACR Pin during start up. Code_ACR = 0.256 *R_SCL/ACR (KΩ)
0x3F [7:0]	SCL/ACR_CONV [9:2]	R	0x00	

7 Functional Block Diagram

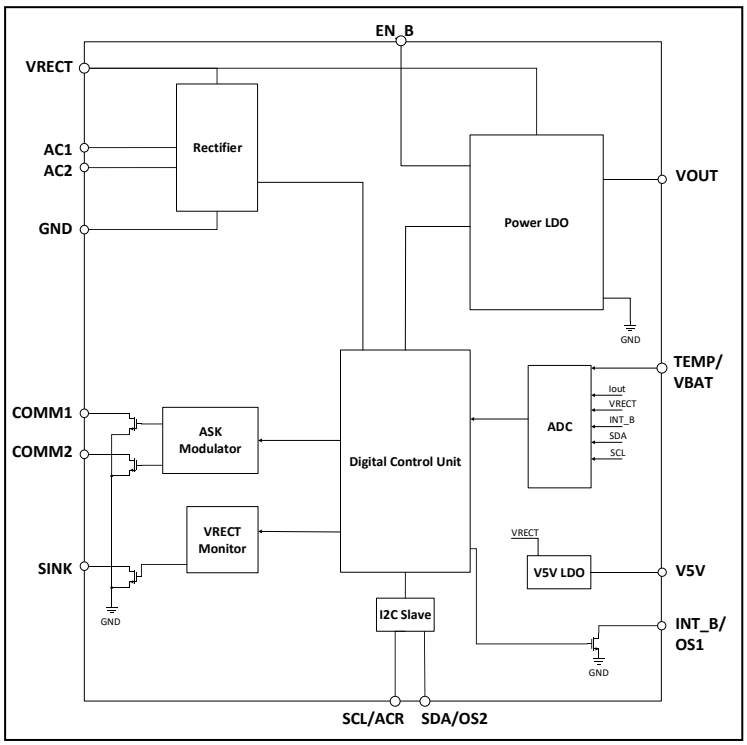


Figure 2. Function Block Diagram

8 Typical Characteristics

The following testing is using NU1020+NU1513 wireless transmitter EVM with MPA2 Tx Coil.

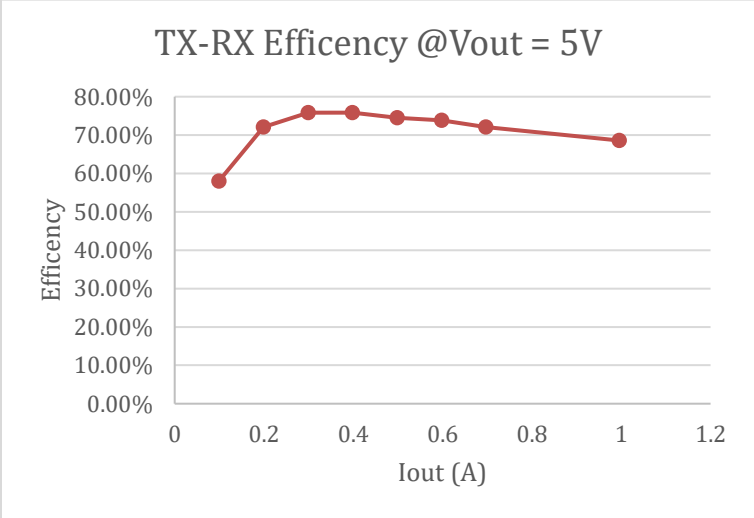


Figure 3. Efficiency: VOUT=5V

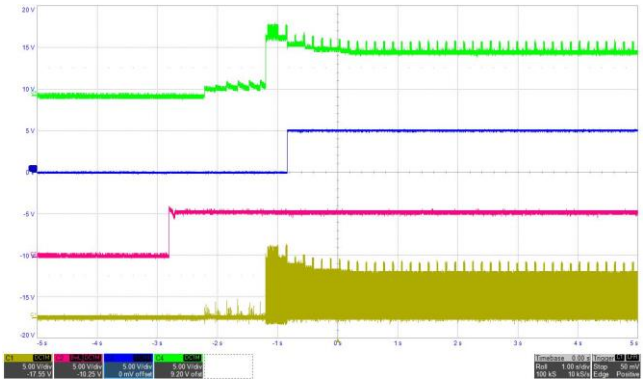


Figure 4. Start up by Adapter: VOUT=5V, IOUT=0.5A

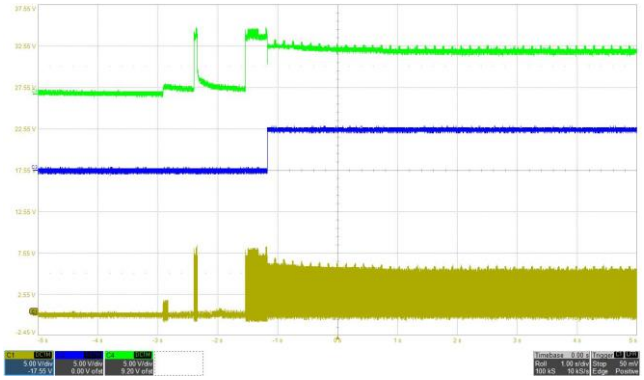


Figure 5. Start up by Rx: VOUT=5V, IOUT=0.5A

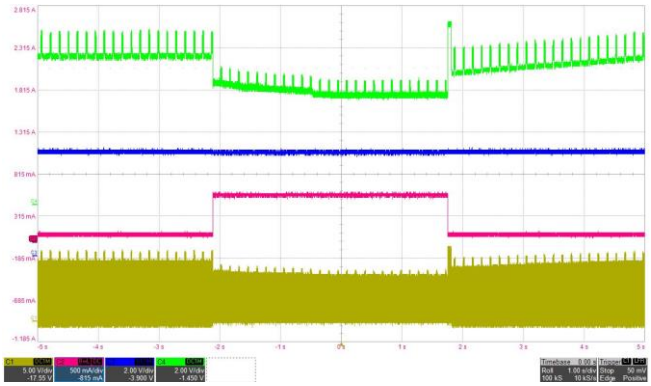


Figure 6. Transient Response: VOUT=5V, IOUT=0A to 0.5A; 0.5A to 0A

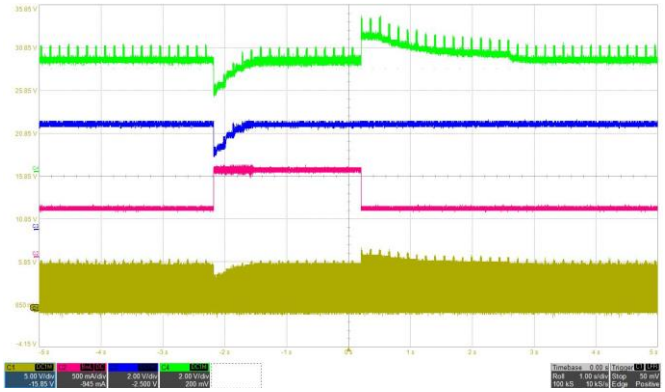


Figure 7. Transient Response: VOUT=5V, IOUT=0.5A to 1A; 1A to 0.5A

Note: (1) Figure 4: CH1-AC1; CH2-VIN_Adapter; CH3-V_{out}; CH4-V_{rect}
(2) Figure 5: CH1-AC1; CH2-N/A; CH3-V_{out}; CH4-V_{rect}
(3) Figure 6~7: CH1-AC1; CH2-I_{out}; CH3- V_{out}; CH4-V_{rect}
(4) The typical characteristics were tested at TA = 25°C, unless otherwise noted

9 Application Descriptions

9.1 System Overview

In a wireless power transfer system, the transmitter system generates magnetic field by feeding AC current into a transmitting coil. The magnetic field is coupled to a receiving side coil and the coupled energy is further maximized by matching the transmitter side impedance. The outputs of the resonant circuit are connected to the AC1 and AC2 pin of the IC which are the inputs to the on-chip synchronous rectifier. The rectifier output is an unregulated voltage connected to the VRECT pin of the IC. To provide a well-regulated voltage source or current source to the downstream circuit, an ultra-low dropout LDO is connected between the VRECT pin and the OUT pin.

The communication between the transmitter side (Tx) and receiver side (Rx) is needed to provide feedback on the power requirement from the receiver to the transmitter. NU1680 is equipped with amplitude modulated communication compliant with WPC standard. The Rx to Tx communication is implemented by turning on the COMM1 and COMM2 internal switches and inserting additional capacitance to the Rx resonant circuit. This modulation of Rx impedance can be detected on the Tx side as amplitude modulation of its coil voltage and current waveform.

Protection is a critical requirement to wireless power receivers, especially the over-voltage protection on the VRECT pin. The coupling factor between Tx and Rx, hence the coupled energy between Tx and Rx, can change suddenly and significantly as the proximity between Rx and Tx coils is altered by end users without notice. When the coupled energy increases rapidly, the VRECT voltage can rise and potentially exceed its maximum voltage rating to cause IC damage. NU1680 incorporates comprehensive two levels of over-voltage protection against any transient conditions.

9.2 Power Supply

When the receiving coil is placed in the magnetic field created by the transmitter analog ping, DC voltage is established on the VRECT pin through the body diode of the rectifier MOSFET initially. V5V follows VRECT voltage through an inner start up circuit. When V5V is above UVLO, the 5V LDO, which provides IC internal bias voltage, is powered up to turn on internal circuit blocks, such as Digital Control Unit, protection circuits and rectifier switches. In addition, the communication from Rx to Tx takes place to instruct Tx to deliver power. Two capacitors of typical value of 4.7uF to 10uF should be placed at the VRECT pin to provide DC voltage to the IC.

When the receiving coil is removed from the magnetic field, or the transmitter is turned off, the voltage of the VRECT pin is discharged by the load connected to the OUT pin and IC operating current. If the V5V voltage drops below UVLO, the IC enters shutdown mode.

9.3 Synchronous Rectifier

The NU1680 has an integrated synchronous rectifier to ensure efficient AC-to-DC conversion, especially for the heavy output load. It has built in a reliable and efficient switch control algorithm to minimize the dead-time while eliminating the possibility of the shoot-through inside the rectifier.

9.4 Power LDO

The output voltage of the Power LDO can be programed through I²C interface. The programmable voltage range is from 3.5V to 9V with 39mV step.
During start up, the Power LDO will turn on when the voltage on VRECT Pin ramp up to $V_{OUT}+V_{LIGHT}+V_{DELTA}$, which can be programmed by related registers.
The output current limit of the LDO can also be programed through I²C interface, the detail range is listed in Register table.
The LDO is protected by the over-current protection. During the over-current protection, SINK switches are turned on to limit the coupled energy. And an interrupt will be triggered to AP/MCU for more action.
LDO has a soft-start feature to prevent in-rush current caused by charging output capacitor during the startup. The soft start gradually turns on the LDO to control and limit its current.

9.5 Over-Voltage Protection

Since the feedback loop between Rx and Tx is inherently slow, the transmitter is unable to reduce the power output instantly when the overvoltage condition occurs on the receiver side. The delay can be in the range of tens or even hundreds of milli-seconds which is a long time enough to damage the IC. The over-voltage protection circuit engages immediately upon the occurrence of the over-voltage condition. There are two level over voltage protection. Firstly, reach the low level OVP1 threshold, the protection circuit will create a 'bleeding' resistor (One 220Ω resistors in 0805 packages are recommended) to the VRECT pin to dissipate the power through the resistor by SINK Pin. And,

- MTP_OVP1_EPT_EN=0, Disable sending EPT and sending CE more quickly;
- MTP_OVP1_EPT_EN=1, Sending EPT;

Secondly, if it reaches the high level OVP2, Sending EPT and trig the hard protection which cut off the energy charging into the VRECT circuit immediately.

9.6 Over-Current Protection

NU1680 integrates a reliable over current protection circuit. Current of the LDO is sensed and compared to the over-current protection threshold. If the current exceeds the threshold, the internal the over-current protection circuit is triggered, and the Power LDO will limit the output current and send EPT to Tx to turn off the wireless transmitting. The OCP threshold can be set through I²C, refer to the Register table.

9.7 Short-Circuit Protection

NU1680 integrates a reliable short-circuit protection. If the output of power LDO is lower than 1V, the internal protection circuit is triggered, and the Power LDO will be turned off to protect the IC.

9.8 External Temperature Protection

NU1680 integrates a high and low temperature protection for Battery or other external components. To use this function, connect a R_{25} = 100K, beta = 4250 NTC resistor between TEMP/VBAT and ground and clear MTP_VBAT_TRK_EN=0.
For high temperature protection, there are four levels of temperature threshold configured by MTP_TEMP_TH. if the temperature rises to the configured threshold, IC will trig the temperature protection and send EPT to Tx.
For low temperature protection, MTP_TEMP_LOW_EN should be set. Then if the temperature of target component is below zero degree, IC will trig the temperature protection and send EPT to Tx.
For above two protections, if MTP_TEMP_EPT_EN=0, the EPT package will not be sent out to Tx.

9.9 IC Over-Temperature Protection

To avoid the junction of NU1680 being higher than 150°C, when the die of IC temperature reaches this point, the IC will send EPT to Tx to cut off the wireless charging.

9.10 Tracking Battery Voltage

Setting MTP_VBAT_TRK_EN=1 will enable NU1680 the function of regulating V_{out} to track the Battery voltage by implementing the battery voltage connected to TEMP/VBAT Pin. This function is capable to simply the backward charging circuit design. The detail parameter setting refer to the Register table.

9.11 I²C, INT_B/OS1, SINK, EN_B

NU1680 allows for the I²C communication by SCL/ACR and SCL/OS2, suggest to pull up by 2.2K resister to 5V. I2C address is 0x60, One-byte address mode. Leave the two Pins floating if not use.
INT_B/OS1 pin is an open-drain and low active pin. Connect a resistor (e.g. 10K) between this pin and V5V. This pin is pulled high during normal mode. Under any protection, the INT_B/OS1 pin is pulled low to indicate a fault condition. The fault mode can be read through the I²C interface. If not use this pin, connect this pin to ground.
Recommend connecting a SMD0805 package of 220R between SINK Pin and VRECT Pin to dissipate the over energy during some extreme condition. The pull-down duration time of SINK Pin is typical 200ms when over voltage occurrence.
EN_B is LOW active pin to enable or disable the power LDO of NU1680. Leave this pin floating if not use.

9.12 ADC

NU1680 integrates an accurate 10bit ADC which takes inputs from internal signals such as VRECT voltage, output current. These signals are used to calculate the proper received power to report to Tx during power transfer stage.
NU1680 samples the signal on NTC or Battery voltage by TEMP/VBAT Pin to realize the temperature protection and battery voltage tracking function.

Also, during power on start-up, ADC will sense the resisters connected to INT_B/OS1, SCL/OS2 and SCL/ACR to enter into FOD_RES_MODE mode to configure the FOD parameters.

9.13 FOD Configuration by SCL/OS2, SCL/ACR, INT_B/OS1 Multiplex

NU1680 provide the 2nd function of SCL/OS2, SCL/ACR and INT_B/OS1 for configuration of FOD parameters. During IC power on start-up, a 4uA current will flow through the three Pins to external resisters and first sense the voltage signal on INT_B/OS1, if the voltage is between 0.15~1.15V the IC will set FOD_RES_MODE and enter into the FOD configuration mode. It uses the ADC to configure the related parameters to registers. 4uA current will stop after completes this configuration. Resister on SCL/ACR Pin configures ACR parameter, resister on INT_B/OS1 configures OFFSET at load #0, resister on SCL/OS2 configures OFFSET at load #1 and #2. Refer to the design tool for detail FOD parameter design.

10 Layout Guidelines

Top Layer shown as Figure 8,

- Resonant capacitor C7/C8/C9/C21, COMM capacitor C1/C2 should be placed on the left side of IC, more close more better.
- The trace to coil L1 should be large width.
- Two VRECT capacitors should be placed on each side respectively.
- Place some Via on IC thermal pad pin for good thermal conduction.

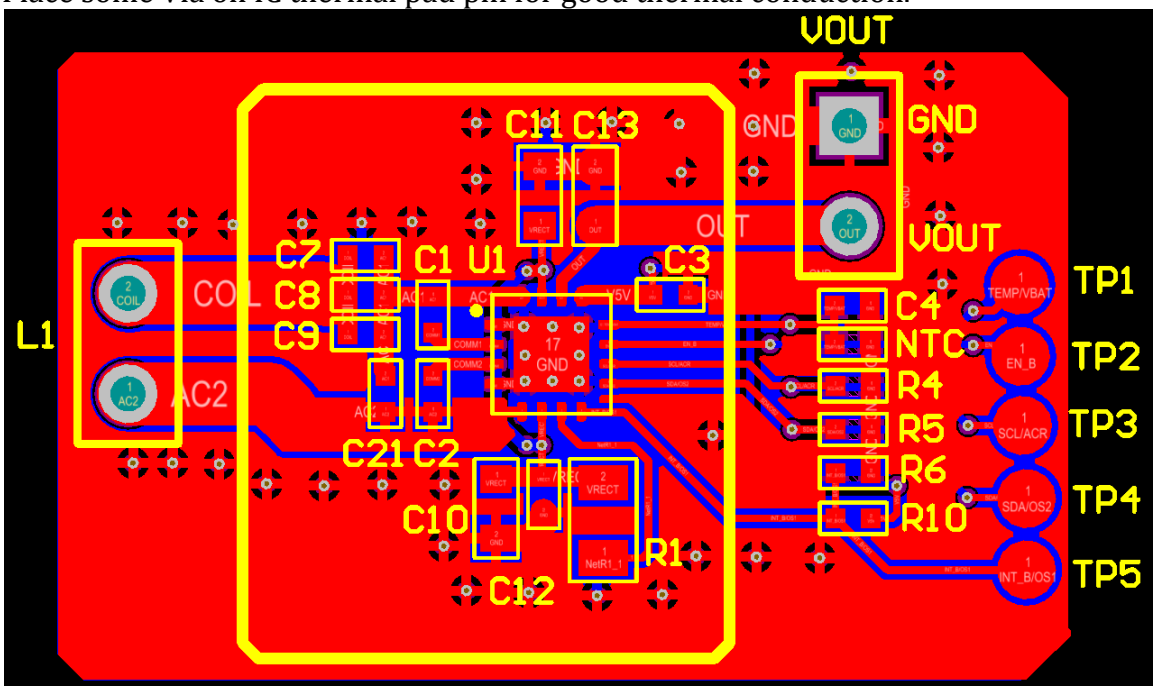


Figure 8: Top layer

Bottom Layer partly shown as Figure 9, Only one consideration needs to be taken care of that at least >=0.3mm width copper connect two VRECT Pins and place at least two Via on each side.

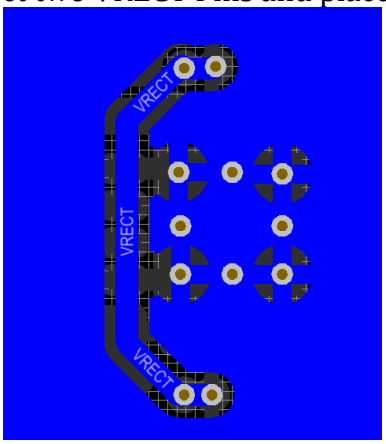
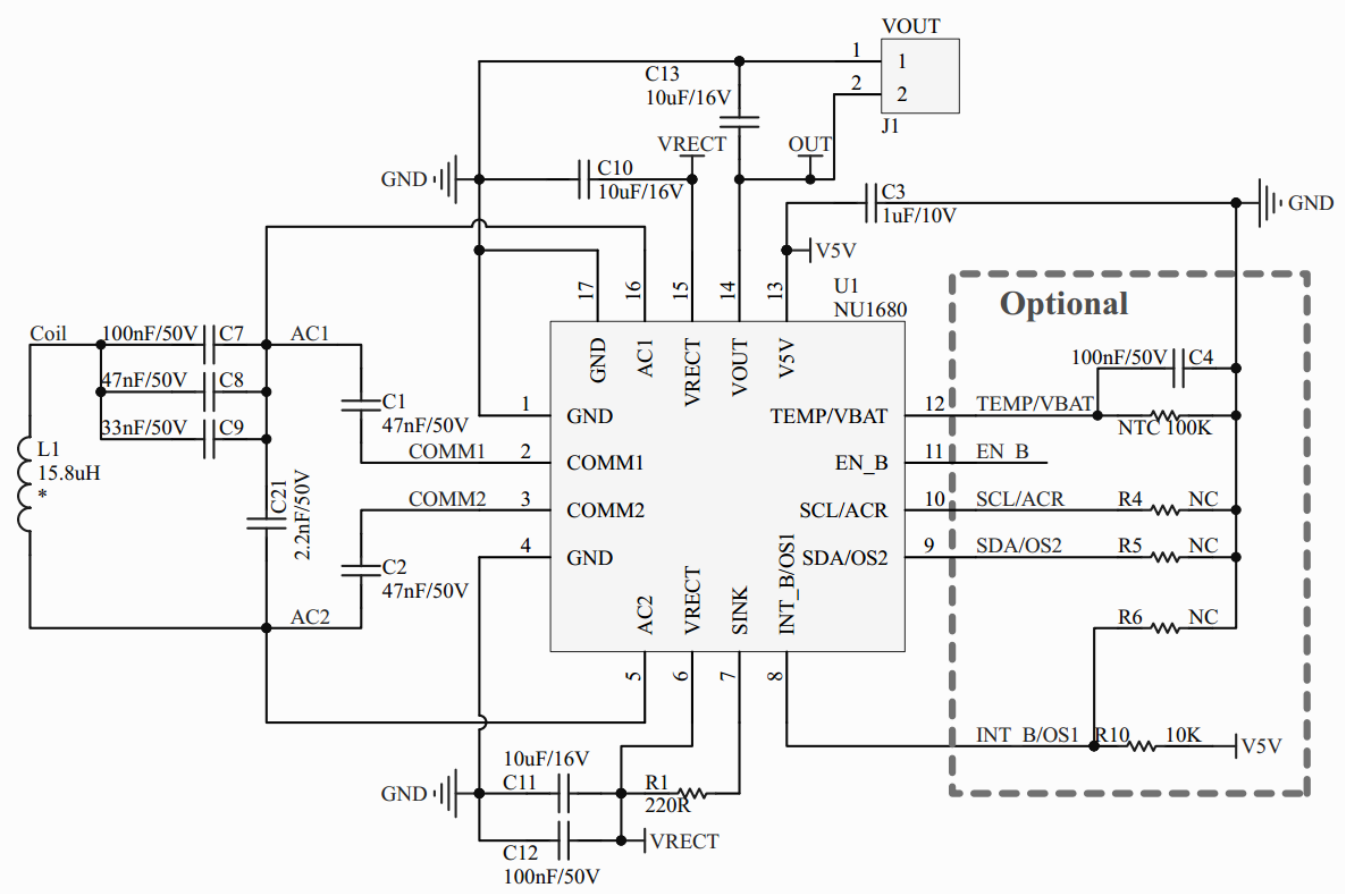


Figure 9: Bottom layer

Note: Make the resonant power routing loop as small as possible and keep away from another signal circuit.

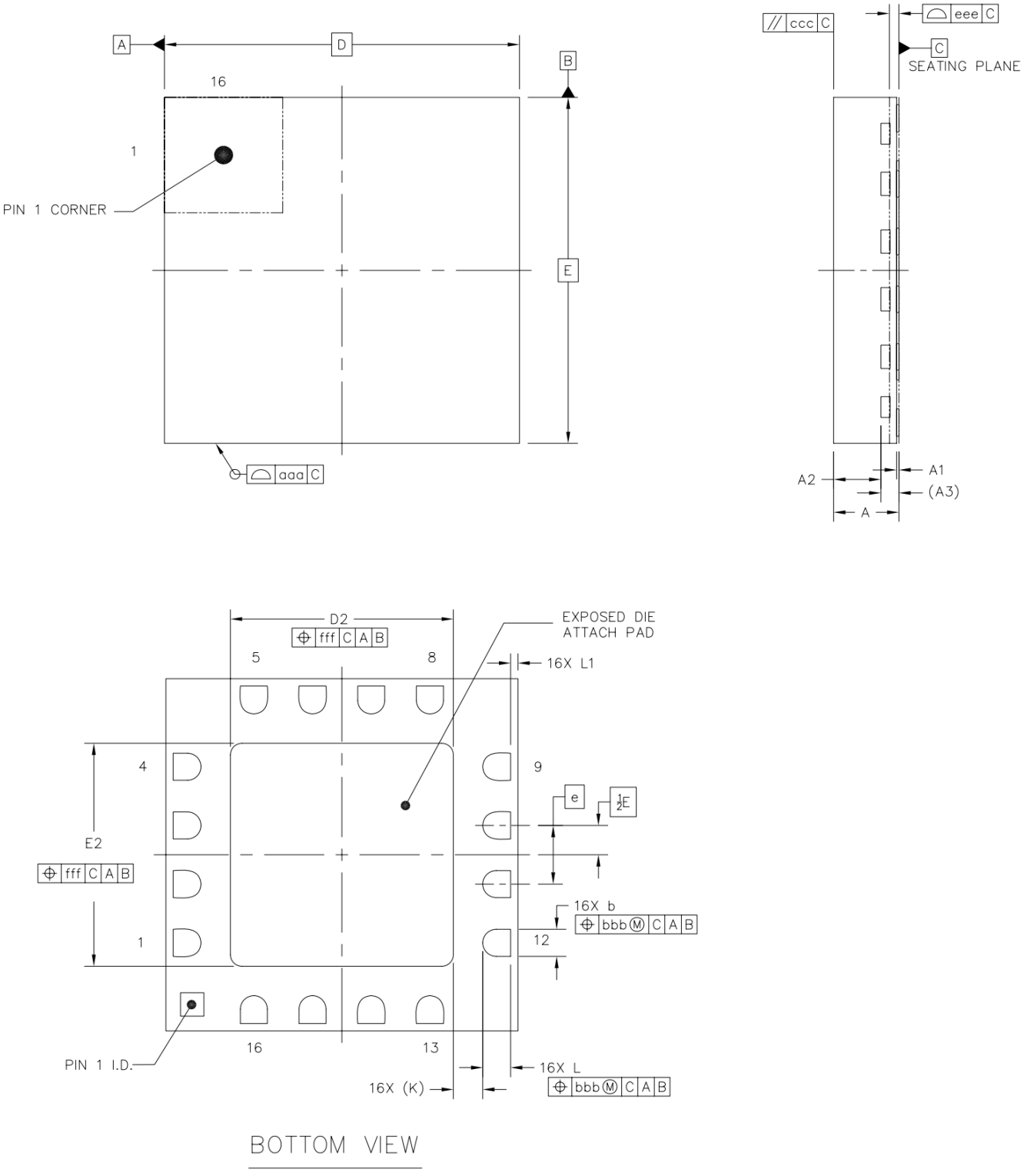
11 Typical application circuit



12 Package Information

Orderable Device	Status	Package Type	Package Drawing	Pins	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp©	Device Marking
NU1680QDHB	Release	QFN	QDH	16	Green(RoHS & No Sb/Br	Cu/Sn Ag Cu	Level-2	-40 to 125	NU1680QDHB

13 Mechanical Data



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.5	0.55	0.6
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.4	---
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.18	0.23	0.28
BODY SIZE	X	D		3 BSC	
	Y	E		3 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	1.8	1.9	2
	Y	E2	1.8	1.9	2
LEAD LENGTH		L	0.1375	0.2375	0.3375
LEAD EDGE TO PKG EDGE		L1		0.0625 REF	
LEAD TIP TO EXPOSED PAD EDGE		K		0.25 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
EXPOSED PAD OFFSET		fff		0.1	

14 Revision Histories

	Date	Changes
V1.0	Oct/26/2019	First release.
V1.1	Nov/7/2019	Tx NU1620 correct to NU1020. Update some parameters in the EC table.
V1.2	Dec/20/2019	Move some parameters from EC table to Application Description.