# LSM303DLHC

## Ultra compact high performance e-compass 3D accelerometer and 3D magnetometer module

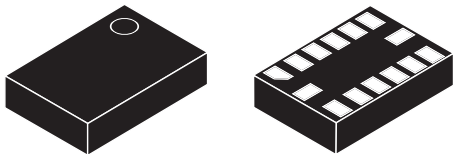
**Preliminary data**

## Features

- 3 magnetic field channels and 3 acceleration channels
- From ±1.3 to ±8.1 gauss magnetic field full-scale
- ±2g/±4g/±8g/±16g selectable full-scale
- 16 bit data output
- $I^2C$ serial interface
- Analog supply voltage 2.16 V to 3.6 V
- Power-down mode/ low-power mode
- 2 independent programmable interrupt generators for free-fall and motion detection
- Embedded temperature sensor
- Embedded FIFO
- 6D/4D orientation detection
- ECOPACK® RoHS and “Green” compliant

## Applications

- Compensated compass
- Map rotation
- Position detection
- Motion-activated functions
- Free-fall detection
- Click/double click recognition
- Pedometer
- Intelligent power-saving for handheld devices
- Display orientation
- Gaming and virtual reality input devices
- Impact recognition and logging
- Vibration monitoring and compensation



**LGA-14 (3x5x1mm)**

## Description

The LSM303DLHC is a system-in-package featuring a 3D digital linear acceleration sensor and a 3D digital magnetic sensor.

LSM303DLHC has linear acceleration full-scales of ±2*g* / ±4*g* / ±8*g* / ±16*g* and a magnetic field full-scale of ±1.3 / ±1.9 / ±2.5 / ±4.0 / ±4.7 / ±5.6 / ±8.1 gauss. All full-scales available are fully selectable by the user.

LSM303DLHC includes an $I^2C$ serial bus interface that supports standard and fast mode 100 kHz and 400kHz. The system can be configured to generate interrupt signals by inertial wake-up/free-fall events as well as by the position of the device itself. Thresholds and timing of interrupt generators are programmable by the end user on the fly. Magnetic and accelerometer parts can be enabled or put into power-down mode separately.

The LSM303DLHC is available in a plastic land grid array package (LGA) and is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

**Table 1. Device summary**

| Part number | Temperature range [°C] | Package | Packing |
|---|---|---|---|
| LSM303DLHC | -40 to +85 | LGA-14 | Tray |
| LSM303DLHCTR | -40 to +85 | LGA-14 | Tape and reel |

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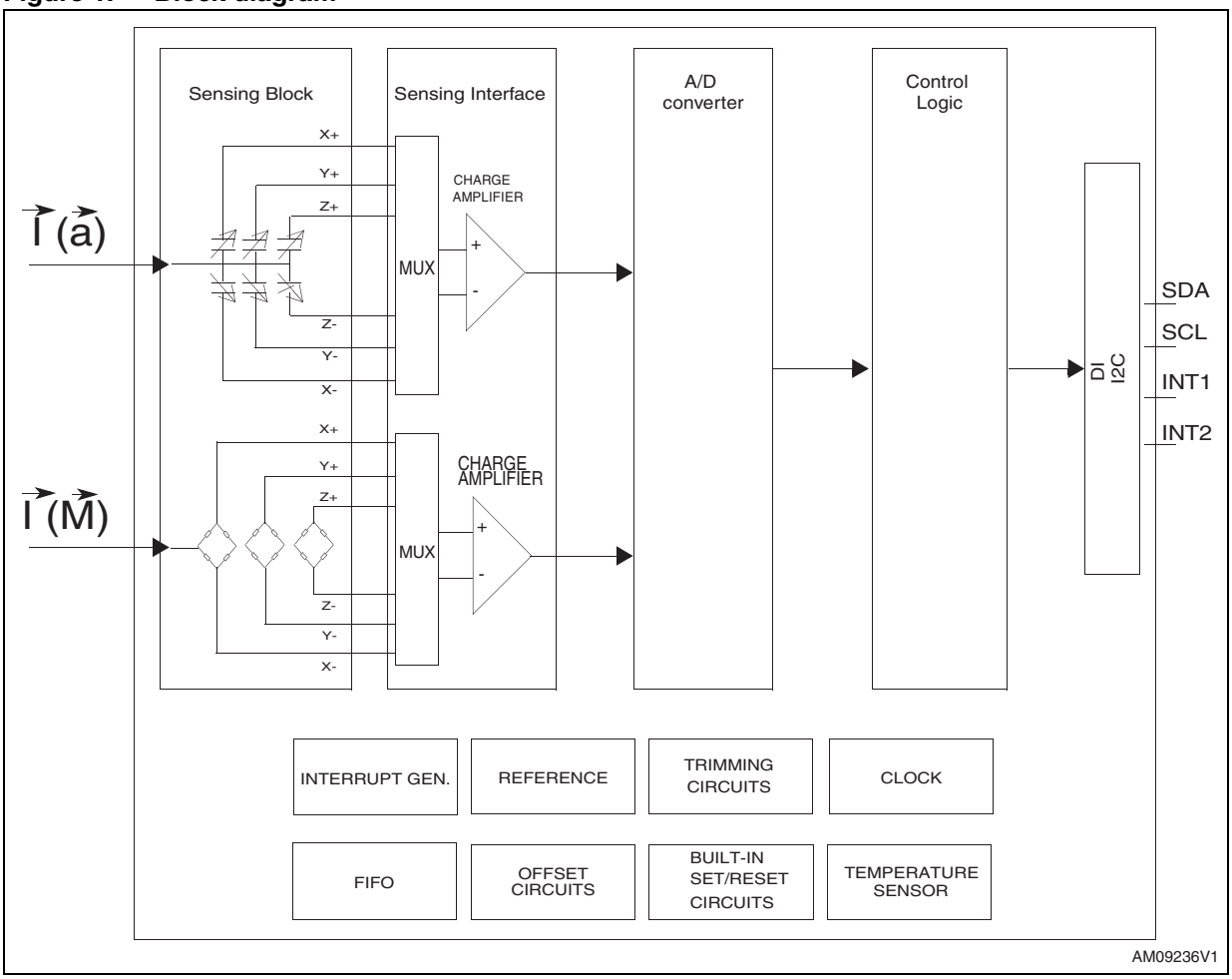
# 1 Block diagram and pin description

## 1.1 Block diagram

**Figure 1. Block diagram**



## 1.2 Pin description

**Figure 2. Pin connection**

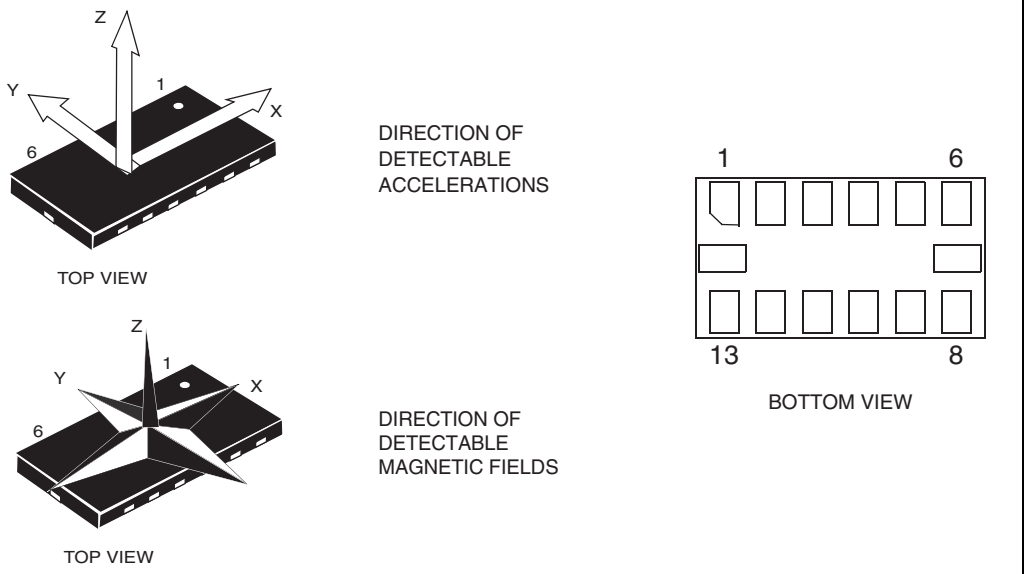



**Table 2. Pin description**

| Pin# | Name | Function |
|---|---|---|
| 1 | Vdd_IO | Power supply for I/O pins |
| 2 | SCL | Signal interface $I^2C$ serial clock (SCL) |
| 3 | SDA | Signal interface $I^2C$ serial data (SDA) |
| 4 | INT2 | Inertial Interrupt 2 |
| 5 | INT1 | Inertial Interrupt 1 |
| 6 | C1 | Reserved capacitor connection (C1) |
| 7 | GND | 0 V supply |
| 8 | Reserved | Leave unconnected |
| 9 | DRDY | Data ready |
| 10 | Reserved | Connect to GND |
| 11 | Reserved | Connect to GND |
| 12 | SETP | S/R capacitor connection (C2) |
| 13 | SETC | S/R capacitor connection (C2) |
| 14 | Vdd | Power supply |

# 2 Module specifications

## 2.1 Sensor characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted[a].

**Table 3. Sensor characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ.[1] | Max. | Unit |
|---|---|---|---|---|---|---|
| LA_FS | Linear acceleration measurement range[2] | FS bit set to 00 | | ±2 | | *g* |
| | | FS bit set to 01 | | ±4 | | |
| | | FS bit set to 10 | | ±8 | | |
| | | FS bit set to 11 | | ±16 | | |
| M_FS | Magnetic measurement range | GN bits set to 001 | | ±1.3 | | gauss |
| | | GN bits set to 010 | | ±1.9 | | |
| | | GN bits set to 011 | | ±2.5 | | |
| | | GN bits set to 100 | | ±4.0 | | |
| | | GN bits set to 101 | | ±4.7 | | |
| | | GN bits set to 110 | | ±5.6 | | |
| | | GN bits set to 111 | | ±8.1 | | |
| LA_So | Linear acceleration sensitivity | FS bit set to 00 | | 1 | | mg/LSB |
| | | FS bit set to 01 | | 2 | | |
| | | FS bit set to 10 | | 4 | | |
| | | FS bit set to 11 | | 12 | | |
| M_GN | Magnetic gain setting | GN bits set to 001 (X,Y) | | 1100 | | LSB/ gauss |
| | | GN bits set to 001 (Z) | | 980 | | |
| | | GN bits set to 010 (X,Y) | | 855 | | |
| | | GN bits set to 010 (Z) | | 760 | | |
| | | GN bits set to 011 (X,Y) | | 670 | | |
| | | GN bits set to 011 (Z) | | 600 | | |
| | | GN bits set to 100 (X,Y) | | 450 | | |
| | | GN bits set to 100 (Z) | | 400 | | |
| | | GN bits set to 101 (X,Y) | | 400 | | |
| | | GN bits set to 101 (Z) | | 355 | | |
| | | GN bits set to 110 (X,Y) | | 330 | | |
| | | GN bits set to 110 (Z) | | 295 | | |
| | | GN bits set to 111[2] (X,Y) | | 230 | | |
| | | GN bits set to 111[2] (Z) | | 205 | | |

a. The product is factory calibrated at 2.5 V. The operational power supply range is from 2.16 V to 3.6 V.

**Table 3. Sensor characteristics (continued)**

| Symbol | Parameter | Test conditions | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|---|
| LA_TCSo | Linear acceleration sensitivity change vs. temperature | FS bit set to 00 | | ±0.01 | | %/°C |
| LA_TyOff | Linear acceleration typical Zero-*g* level offset accuracy(3),(4) | FS bit set to 00 | | ±60 | | m*g* |
| LA_TCOff | Linear acceleration Zero-*g* level change vs. temperature | Max. delta from 25 °C | | ±0.5 | | m*g*/°C |
| LA_An | Acceleration noise density | FS bit set to 00, normal mode(*Table 8.*), ODR bit set to 1001 | | 220 | | ug/ sqrt(Hz) |
| M_R | Magnetic resolution | | | 2 | | mgauss |
| M_CAS | Magnetic cross-axis sensitivity | Cross field =.0.5 gauss H applied = ±3 gauss | | ±1 | | %FS/ gauss |
| M_EF | Maximum exposed field | No permitting effect on zero reading | | | 10000 | gauss |
| M_DF | Disturbing field | Sensitivity starts to degrade. Use S/R pulse to restore sensitivity | | | 20 | gauss |
| Top | Operating temperature range | | -40 | | +85 | °C |

1. Typical specifications are not guaranteed.
2. Verified by wafer level test and measurement of initial offset and sensitivity.
3. Typical Zero-*g* level offset value after MSL3 preconditioning.
4. Offset can be eliminated by enabling the built-in high pass filter.

## 2.2 Temperature sensor characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted [b].

**Table 4. Temperature sensor characteristics**

| Symbol | Parameter | Test condition | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|---|
| TSDr | Temperature sensor output change vs. temperature | - | | 8 | | LSB/°C(2) |
| TODR | Temperature refresh rate | | | ODR(3) | | Hz |
| Top | Operating temperature range | | -40 | | +85 | °C |

1. Typical specifications are not guaranteed.
2. 12-bit resolution.
3. For ODR configuration refer to *Table 72*.

b. The product is factory calibrated at 2.5 V.

## 2.3 Electrical characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted.

**Table 5. Electrical characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|---|
| Vdd | Supply voltage | - | 2.16 | | 3.6 | V |
| Vdd_IO | Module power supply for I/O | | 1.71 | 1.8 | Vdd+0.1 | |
| Idd | Current consumption in normal mode(2) | | | 110 | | µA |
| IddSL | Current consumption in sleep-mode(3) | | | 1 | | µA |
| Top | Operating temperature range | | -40 | | +85 | °C |

1. Typical specifications are not guaranteed.
2. Magnetic sensor setting ODR = 7.5 Hz, Accelerometer sensor ODR = 50 Hz.
3. Linear accelerometer in sleep-mode and magnetic sensor in power-down mode.

## 2.4 Communication interfaces characteristics

External pull-up resistors are required to support I²C standard and fast speed modes.

### 2.4.1 Sensor I²C - inter IC control interface

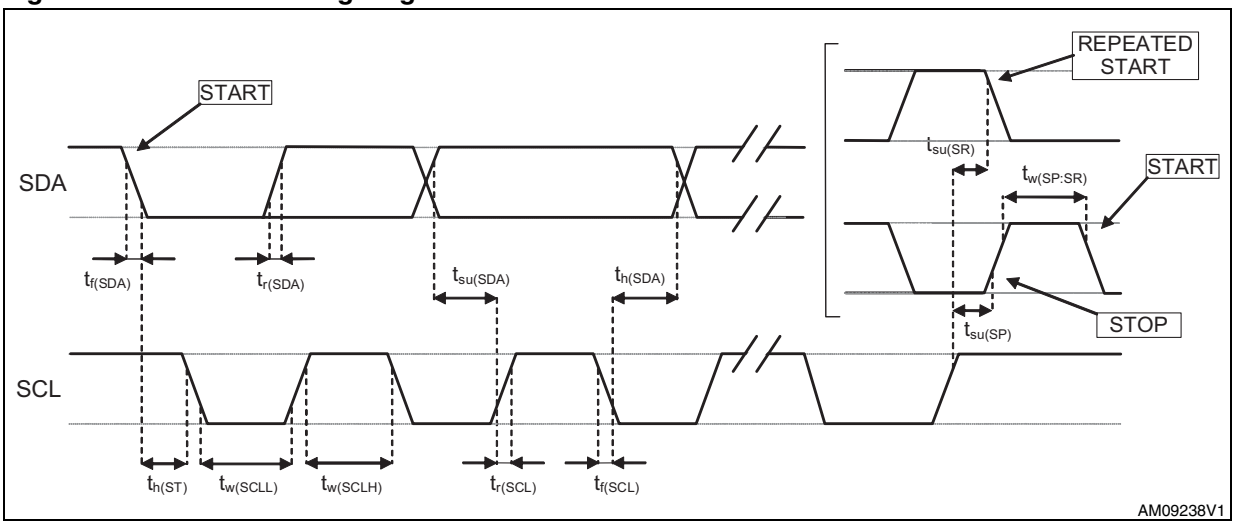
Subject to general operating conditions for Vdd and Top.

**Table 6. I²C slave timing values**

| Symbol | Parameter | I²C standard mode (1) | | I²C fast mode (1) | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $f_{(SCL)}$ | SCL clock frequency | 0 | 100 | 0 | 400 | KHz |
| $t_{w(SCLL)}$ | SCL clock low time | 4.7 | | 1.3 | | µs |
| $t_{w(SCLH)}$ | SCL clock high time | 4.0 | | 0.6 | | |
| $t_{su(SDA)}$ | SDA setup time | 250 | | 100 | | ns |
| $t_{h(SDA)}$ | SDA data hold time | 0.01 | 3.45 | 0.01 | 0.9 | µs |
| $t_{r(SDA)}$ $t_{r(SCL)}$ | SDA and SCL rise time | | 1000 | $20 + 0.1C_b$ (2) | 300 | ns |
| $t_{f(SDA)}$ $t_{f(SCL)}$ | SDA and SCL fall time | | 300 | $20 + 0.1C_b$ (2) | 300 | |
| $t_{h(ST)}$ | START condition hold time | 4 | | 0.6 | | µs |
| $t_{su(SR)}$ | Repeated START condition setup time | 4.7 | | 0.6 | | |
| $t_{su(SP)}$ | STOP condition setup time | 4 | | 0.6 | | |
| $t_{w(SP:SR)}$ | Bus free time between STOP and START condition | 4.7 | | 1.3 | | |

1. Data based on standard I²C protocol requirement, not tested in production.
2. Cb = total capacitance of one bus line, in pF.

**Figure 3. I²C slave timing diagram (c)**



## 2.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 7. Absolute maximum ratings**

| Symbol | Ratings | Maximum value | Unit |
|---|---|---|---|
| Vdd | Supply voltage | -0.3 to 4.8 | V |
| Vdd_IO | I/O pins supply voltage | -0.3 to 4.8 | V |
| Vin | Input voltage on any control pin (SCL, SDA) | -0.3 to Vdd_IO +0.3 | V |
| $A_{POW}$ | Acceleration (any axis, powered, Vdd = 2.5 V) | 3,000 for 0.5 ms | *g* |
| | | 10,000 for 0.1 ms | *g* |
| $A_{UNP}$ | Acceleration (any axis, unpowered) | 3,000 for 0.5 ms | *g* |
| | | 10,000 for 0.1 ms | *g* |
| $T_{OP}$ | Operating temperature range | -40 to +85 | °C |
| $T_{STG}$ | Storage temperature range | -40 to +125 | °C |

This is a mechanical shock sensitive device, improper handling can cause permanent damage to the part.

This is an ESD sensitive device, improper handling can cause permanent damage to the part.

c. Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

## 2.6 Terminology

### 2.6.1 Linear acceleration sensitivity

Linear acceleration sensitivity describes the gain of the accelerometer sensor and can be determined by applying 1 *g* acceleration to it. As the sensor can measure DC accelerations, this can be done easily by pointing the axis of interest towards the center of the Earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and also very little over time. The sensitivity tolerance describes the range of sensitivities of a large population of sensors.

### 2.6.2 Zero-g level

Zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady-state on a horizontal surface measures 0 *g* in the X axis and 0 *g* in the Y axis whereas the Z axis measures 1 *g*. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as 2's complement number). A deviation from the ideal value in this case is called Zero-*g* offset. Offset is, to some extent, a result of stress to the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Zero-*g* level change vs. temperature". The Zero-*g* level tolerance (TyOff) describes the standard deviation of the range of Zero-*g* levels of a population of sensors.

# 3 Functionality

The LSM303DLHC is a system-in-package featuring a 3D digital linear acceleration and 3D digital magnetic field detection sensor.

The system includes specific sensing elements and an IC interface capable of measuring both the linear acceleration and magnetic field applied on it and to provide a signal to the external world through an $I^2C$ serial interface with separated digital output.

The sensing system is manufactured using specialized micromachining processes, while the IC interfaces are realized using a CMOS technology that allows to design a dedicated circuit which is trimmed to better match the sensing element characteristics.

The LSM303DLHC features two data-ready signals (RDY) which indicate when a new set of measured acceleration data and magnetic data are available, therefore simplifying data synchronization in the digital system that uses the device.

The LSM303DLHC may also be configured to generate a free-fall interrupt signal according to a programmed acceleration event along the enabled axes.

### Linear acceleration operating mode

LSM303DLHC provides two different acceleration operating modes, respectively reported as “normal mode” and “low-power mode”. While normal mode guarantees high resolution, low-power mode reduces further the current consumption.

*Table 8* summarizes how to select the operating mode.

**Table 8. Accelerometer operating mode selection**

| Operating mode | CTRL_REG1[3] (LPen bit) | CTRL_REG4[3] (HR bit) | BW [Hz] | Turn-on time [ms] |
|---|---|---|---|---|
| Low-power mode | 1 | 0 | ODR/2 | 1 |
| Normal mode | 0 | 1 | ODR/9 | 7/ODR |

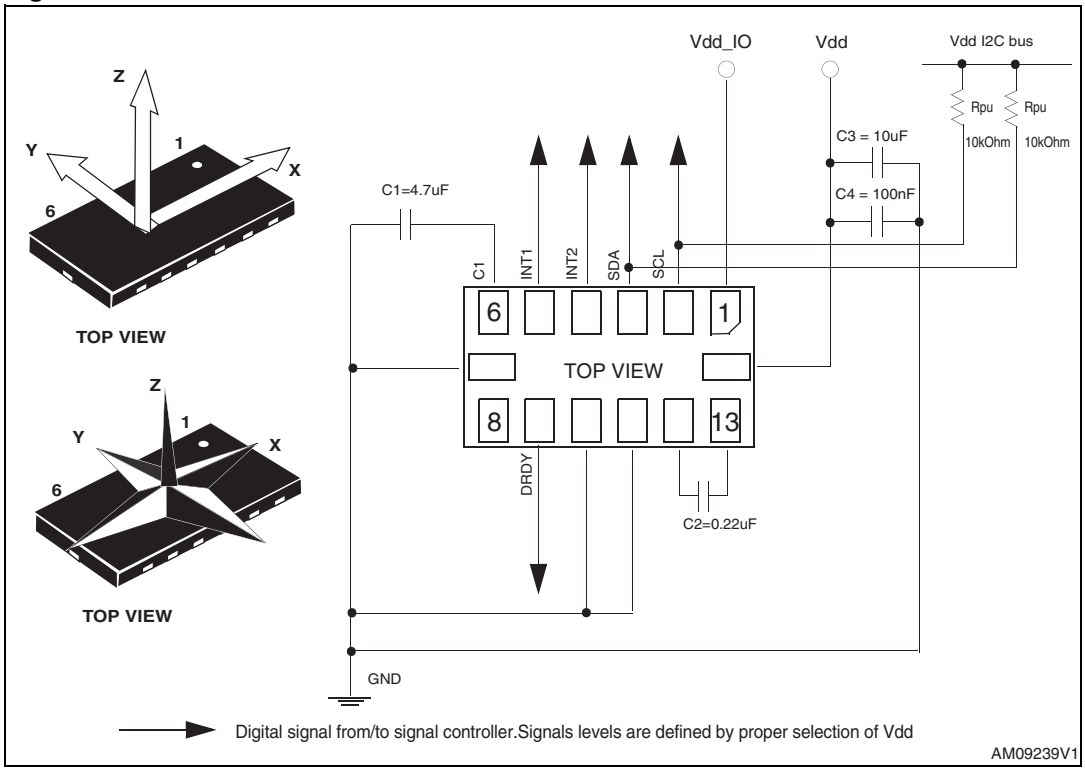
## 3.1 Factory calibration

The IC interface is factory calibrated for linear acceleration sensitivity (LA_So), and linear acceleration Zero-g level (LA_TyOff).

The trimming values are stored inside the device by a non-volatile memory. Any time the device is turned on, the trimming parameters are downloaded into the registers to be used during the normal operation. This allows the user to use the device without further calibration.

# 4 Application hints

**Figure 4. LSM303DLHC electrical connection**




## 4.1 capacitors

The C1 and C2 external capacitors should be low SR value ceramic type constructions (typ. suggested value 200 mOhm). Reservoir capacitor C1 is nominally 4.7 µF in capacitance, with the set/reset capacitor C2 nominally 0.22 µF in capacitance.

The device core is supplied through the Vdd line. Power supply decoupling capacitors (C4=100 nF ceramic, C3=10 µF Al) should be placed as near as possible to the supply pin of the device (common design practice). All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to *Figure 4*).

The functionality of the device and the measured acceleration/magnetic field data is selectable and accessible through the $I^2C$ interface.

The functions, the threshold, and the timing of the two interrupt pins (INT 1 and INT 2) can be completely programmed by the user through the $I^2C$ interface.

## 4.2 Pull-up resistors

Pull-up resistors (suggested value 10 kOhm) are placed on the two $I^2C$ bus lines.

## 4.3 Digital interface power supply

This digital interface, dedicated to the linear acceleration and to the magnetic field signal, is capable of operating with a standard power supply (Vdd) or using a dedicated power supply (Vdd_IO).

## 4.4 Soldering information

The LGA package is compliant with the ECOPACK®, RoHS, and “Green” standard.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at www.st.com/mems.

## 4.5 High current wiring effects

High current in the wiring and printed circuit trace can be culprits in causing errors in magnetic field measurements for compassing.

Conductor generated magnetic fields add to the Earth’s magnetic field, causing errors in compass heading computation.

Keep currents higher than 10 mA a few millimeters further away from the sensor IC.

# 5 Digital interfaces

The registers embedded inside the LSM303DLHC are accessible through two separate $I^2C$ serial interfaces, one for the accelerometer core and one for the magnetometer core.

**Table 9. Serial interface pin description**

| PIN Name | PIN Description |
|---|---|
| SCL | $I^2C$ serial clock (SCL) |
| SDA | $I^2C$ serial data (SDA) |

## 5.1 $I^2C$ serial interface

The LSM303DLHC $I^2C$ is a bus slave. The $I^2C$ is employed to write the data into the registers whon also be read back.

The relevant $I^2C$ terminology is given in the table below.

**Table 10. Serial interface pin description**

| Term | Description |
|---|---|
| Transmitter | The device which sends data to the bus |
| Receiver | The device which receives data from the bus |
| Master | The device which initiates a transfer, generates clock signals, and terminates a transfer |
| Slave | The device addressed by the master |

There are two signals associated with the $I^2C$ bus, the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface.

### 5.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and bit 8 tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the LSM303DLHC behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted; the 7 LSBs represent the actual register address while the MSB enables address auto-increment. If the MSB of the SUB field is '1', the SUB (register address) is automatically increased to allow multiple data Read/Write.

**Table 11. Transfer when master is writing one byte to slave**

| Master | ST | SAD + W | | SUB | | DATA | | SP |
|---|---|---|---|---|---|---|---|---|
| Slave | | | SAK | | SAK | | SAK | |

**Table 12. Transfer when master is writing multiple bytes to slave:**

| Master | ST | SAD + W | | SUB | | DATA | | DATA | | SP |
|---|---|---|---|---|---|---|---|---|---|---|
| Slave | | | SAK | | SAK | | SAK | | SAK | |

**Table 13. Transfer when master is receiving (reading) one byte of data from slave:**

| Master | ST | SAD + W | | SUB | | SR | SAD + R | | | NMAK | SP |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Slave | | | SAK | | SAK | | | SAK | DATA | | |

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSB) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left HIGH by the slave. The master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

### 5.1.2 Linear acceleration digital interface

**For linear acceleration the default (factory) 7-bit slave address is 0011001b.**

The slave address is completed with a Read/Write bit. If the bit is '1' (read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is '0' (write) the master transmits to the slave with the direction unchanged. *Table 14* explains how the ead/write bit pattern is composed, listing all the possible configurations.

**Table 14. SAD+Read/Write patterns**

| Command | SAD[7:1] | R/W | SAD+R/W |
|---|---|---|---|
| Read | 0011001 | 1 | 00110011 (33h) |
| Write | 0011001 | 0 | 00110010 (32h) |

In order to read multiple bytes, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of the first register to be read.

In the presented communication format, MAK is master acknowledge and NMAK is no master acknowledge.

**Table 15. Transfer when master is receiving (reading) multiple bytes of data from slave**

| Master | ST | SAD +W | | SUB | | SR | SAD +R | | | MAK | | MAK | | NMAK | SP |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Slave | | | SAK | | SAK | | | SAK | DATA | | DATA | | DATA | | |

### 5.1.3 Magnetic field digital interface

**For magnetic sensors the default (factory) 7-bit slave address is 0011110xb.**

The slave address is completed with a Read/Write bit. If the bit is '1' (read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is '0' (write) the master transmits to the slave with the direction unchanged. *Table 16* explains how the SAD is composed.

**Table 16. SAD**

| Command | SAD[6:0] | R/W | SAD+R/W |
|---|---|---|---|
| Read | 0011110 | 1 | 00111101 (3Dh) |
| Write | 0011110 | 0 | 00111100 (3Ch) |

#### Magnetic signal interface reading/writing

The interface uses an address pointer to indicate which register location is to be read from or written to. These pointer locations are sent from the master to this slave device and succeed the 7-bit address plus 1 bit Read/Write identifier.

To minimize the communication between the master and magnetic digital interface of LSM303DLHC, the address pointer updates automatically without master intervention.

This automatic address pointer update has two additional features. First, when address 12 or higher is accessed, the pointer updates to address 00, and secondly, when address 08 is reached, the pointer rolls back to address 03. Logically, the address pointer operation functions as shown below.

If (address pointer = 08) then the address pointer = 03

Or else, if (address pointer >= 12) then the address pointer = 0

Or else, (address pointer) = (address pointer) + 1

The address pointer value itself cannot be read via the $I^2C$ bus.

Any attempt to read an invalid address location returns 0, and any write to an invalid address location, or an undefined bit within a valid address location, is ignored by this device.

# 6 Register mapping

*Table 17* provides a listing of the 8-bit registers embedded in the device and the related addresses:

**Table 17. Register address map**

| Name | Slave address | Type | Register address | | Default | Comment |
|---|---|---|---|---|---|---|
| | | | Hex | Binary | | |
| Reserved (do not modify) | *Table 14* | | 00 - 1F | -- | -- | Reserved |
| CTRL_REG1_A | *Table 14* | rw | 20 | 010 0000 | 00000111 | |
| CTRL_REG2_A | *Table 14* | rw | 21 | 010 0001 | 00000000 | |
| CTRL_REG3_A | *Table 14* | rw | 22 | 010 0010 | 00000000 | |
| CTRL_REG4_A | *Table 14* | rw | 23 | 010 0011 | 00000000 | |
| CTRL_REG5_A | *Table 14* | rw | 24 | 010 0100 | 00000000 | |
| CTRL_REG6_A | *Table 14* | rw | 25 | 010 0101 | 00000000 | |
| REFERENCE_A | *Table 14* | rw | 26 | 010 0110 | 00000000 | |
| STATUS_REG_A | *Table 14* | r | 27 | 010 0111 | 00000000 | |
| OUT_X_L_A | *Table 14* | r | 28 | 010 1000 | output | |
| OUT_X_H_A | *Table 14* | r | 29 | 010 1001 | output | |
| OUT_Y_L_A | *Table 14* | r | 2A | 010 1010 | output | |
| OUT_Y_H_A | *Table 14* | r | 2B | 010 1011 | output | |
| OUT_Z_L_A | *Table 14* | r | 2C | 010 1100 | output | |
| OUT_Z_H_A | *Table 14* | r | 2D | 010 1101 | output | |
| FIFO_CTRL_REG_A | *Table 14* | rw | 2E | 010 1110 | 00000000 | |
| FIFO_SRC_REG_A | *Table 14* | r | 2F | 010 1111 | | |
| INT1_CFG_A | *Table 14* | rw | 30 | 011 0000 | 00000000 | |
| INT1_SOURCE_A | *Table 14* | r | 31 | 011 0001 | 00000000 | |
| INT1_THS_A | *Table 14* | rw | 32 | 011 0010 | 00000000 | |
| INT1_DURATION_A | *Table 14* | rw | 33 | 011 0011 | 00000000 | |
| INT2_CFG_A | *Table 14* | rw | 34 | 011 0100 | 00000000 | |
| INT2_SOURCE_A | *Table 14* | r | 35 | 011 0101 | 00000000 | |
| INT2_THS_A | *Table 14* | rw | 36 | 011 0110 | 00000000 | |
| INT2_DURATION_A | *Table 14* | rw | 37 | 011 0111 | 00000000 | |
| CLICK_CFG_A | *Table 14* | rw | 38 | 011 1000 | 00000000 | |
| CLICK_SRC_A | *Table 14* | rw | 39 | 011 1001 | 00000000 | |
| CLICK_THS_A | *Table 14* | rw | 3A | 011 1010 | 00000000 | |
| TIME_LIMIT_A | *Table 14* | rw | 3B | 011 1011 | 00000000 | |

**Table 17. Register address map (continued)**

| Name | Slave address | Type | Register address | | Default | Comment |
|---|---|---|---|---|---|---|
| | | | Hex | Binary | | |
| TIME_LATENCY_A | *Table 14* | rw | 3C | 011 1100 | 00000000 | |
| TIME_WINDOW_A | *Table 14* | rw | 3D | 011 1101 | 00000000 | |
| Reserved (do not modify) | *Table 14* | | 3E-3F | -- | -- | Reserved |
| CRA_REG_M | *Table 16* | rw | 00 | 00000000 | 0001000 | |
| CRB_REG_M | *Table 16* | rw | 01 | 00000001 | 0010000 | |
| MR_REG_M | *Table 16* | rw | 02 | 00000010 | 00000011 | |
| OUT_X_H_M | *Table 16* | r | 03 | 00000011 | output | |
| OUT_X_L_M | *Table 16* | r | 04 | 00000100 | output | |
| OUT_Z_H_M | *Table 16* | r | 05 | 00000101 | output | |
| OUT_Z_L_M | *Table 16* | r | 06 | 00000110 | output | |
| OUT_Y_H_M | *Table 16* | r | 07 | 00000111 | output | |
| OUT_Y_L_M | *Table 16* | r | 08 | 00001000 | output | |
| SR_REG_Mg | *Table 16* | r | 09 | 00001001 | 00000000 | |
| IRA_REG_M | *Table 16* | r | 0A | 00001010 | 01001000 | |
| IRB_REG_M | *Table 16* | r | 0B | 00001011 | 00110100 | |
| IRC_REG_M | *Table 16* | r | 0C | 00001100 | 00110011 | |
| Reserved (do not modify) | *Table 16* | | 0D-30 | -- | -- | Reserved |
| TEMP_OUT_H_M | *Table 16* | | 31 | 00000000 | output | |
| TEMP_OUT_L_M | *Table 16* | | 32 | 00000000 | output | |
| Reserved (do not modify) | *Table 16* | | 33-3A | -- | -- | Reserved |

Registers marked as “reserved” must not be changed. The writing to these registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibrated values. Their content is automatically restored when the device is powered up.

# 7 Register description

The device contains a set of registers which are used to control its behavior and to retrieve acceleration data. The register address, made up of 7 bits, is used to identify them and to write the data through the serial interface.

## 7.1 Linear acceleration register description

### 7.1.1 CTRL_REG1_A (20h)

**Table 18. CTRL_REG1_A register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| ODR3 | ODR2 | ODR1 | ODR0 | LPen | Zen | Yen | Xen |

**Table 19. CTRL_REG1_A description**

| | |
|---|---|
| ODR3-0 | Data rate selection. Default value: 0<br>(0000: power-down, others: refer to *Table 20*.) |
| LPen | Low-power mode enable. Default value: 0<br>(0: normal mode, 1: low-power mode) |
| Zen | Z axis enable. Default value: 1<br>(0: Z axis disabled, 1: Z axis enabled) |
| Yen | Y axis enable. Default value: 1<br>(0: Y axis disabled, 1: Y axis enabled) |
| Xen | X axis enable. Default value: 1<br>(0: X axis disabled, 1: X axis enabled) |

**ODR<3:0>** is used to set the power mode and ODR selection. In *Table 20* all frequencies resulting in a combination of ODR<3:0> are listed.

**Table 20. Data rate configuration**

| ODR3 | ODR2 | ODR1 | ODR0 | Power mode selection |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Power-down mode |
| 0 | 0 | 0 | 1 | Normal / low-power mode (1 Hz) |
| 0 | 0 | 1 | 0 | Normal / low-power mode (10 Hz) |
| 0 | 0 | 1 | 1 | Normal / low-power mode (25 Hz) |
| 0 | 1 | 0 | 0 | Normal / low-power mode (50 Hz) |
| 0 | 1 | 0 | 1 | Normal / low-power mode (100 Hz) |
| 0 | 1 | 1 | 0 | Normal / low-power mode (200 Hz) |
| 0 | 1 | 1 | 1 | Normal / low-power mode (400 Hz) |

Table 20. Data rate configuration (continued)

| ODR3 | ODR2 | ODR1 | ODR0 | Power mode selection |
|---|---|---|---|---|
| 1 | 0 | 0 | 0 | Low-power mode (1.620 KHz) |
| 1 | 0 | 0 | 1 | Normal (1.344 kHz) / low-power mode (5.376 KHz) |

### 7.1.2 CTRL_REG2_A (21h)

Table 21. CTRL_REG2_A register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| HPM1 | HPM0 | HPCF2 | HPCF1 | FDS | HPCLICK | HPIS2 | HPIS1 |

Table 22. CTRL_REG2_A description

| | |
|---|---|
| HPM1 -HPM0 | High pass filter mode selection. Default value: 00<br>(refer to *Table 23*) |
| HPCF2 - HPCF1 | High pass filter cut-off frequency selection |
| FDS | Filtered data selection. Default value: 0<br>(0: internal filter bypassed, 1: data from internal filter sent to output register and FIFO) |
| HPCLICK | High pass filter enabled for CLICK function.<br>(0: filter bypassed, 1: filter enabled) |
| HPIS2 | High pass filter enabled for AOI function on Interrupt 2,<br>(0: filter bypassed, 1: filter enabled) |
| HPIS1 | High pass filter enabled for AOI function on Interrupt 1,<br>(0: filter bypassed, 1: filter enabled) |

Table 23. High pass filter mode configuration

| HPM1 | HPM0 | High pass filter mode |
|---|---|---|
| 0 | 0 | Normal mode (reset reading HP_RESET_FILTER) |
| 0 | 1 | Reference signal for filtering |
| 1 | 0 | Normal mode |
| 1 | 1 | Autoreset on interrupt event |

### 7.1.3 CTRL_REG3_A (22h)

Table 24. CTRL_REG3_A register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| I1_CLICK | I1_AOI1 | I1_AOI2 | I1_DRDY1 | I1_DRDY2 | I1_WTM | I1_OVERRUN | -- |

**Table 25. CTRL_REG3_A description**

| | |
|---|---|
| I1_CLICK | CLICK interrupt on INT1. Default value 0.<br>(0: disable, 1: enable) |
| I1_AOI1 | AOI1 interrupt on INT1. Default value 0.<br>(0: disable, 1: enable) |
| I1_AOI2 | AOI2 interrupt on INT1. Default value 0.<br>(0: disable, 1: enable) |
| I1_DRDY1 | DRDY1 interrupt on INT1. Default value 0.<br>(0: disable, 1: enable) |
| I1_DRDY2 | DRDY2 interrupt on INT1. Default value 0.<br>(0: disable, 1: enable) |
| I1_WTM | FIFO watermark interrupt on INT1. Default value 0.<br>(0: disable, 1: enable) |
| I1_OVERRUN | FIFO overrun interrupt on INT1. Default value 0.<br>(0: disable, 1: enable) |

### 7.1.4 CTRL_REG4_A (23h)

**Table 26. CTRL_REG4_A register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| BDU | BLE | FS1 | FS0 | HR | 0(1) | 0(1) | SIM |

1. This bit must be set to '0' for correct working of the device.

**Table 27. CTRL_REG4_A description**

| | |
|---|---|
| BDU | Block data update. Default value: 0<br>(0: continuos update, 1: output registers not updated until MSB and LSB reading |
| BLE | Big/little endian data selection. Default value 0.<br>(0: data LSB @ lower address, 1: data MSB @ lower address) |
| FS1-FS0 | Full-scale selection. Default value: 00<br>(00: +/- 2G, 01: +/- 4G, 10: +/- 8G, 11: +/- 16G) |
| HR | High resolution output mode: Default value: 0<br>(0: high resolution disable, 1: high resolution enable) |
| SIM | SPI serial interface mode selection. Default value: 0<br>(0: 4-wire interface, 1: 3-wire interface). |

### 7.1.5 CTRL_REG5_A (24h)

**Table 28. CTRL_REG5_A register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| BOOT | FIFO_EN | -- | -- | LIR_INT1 | D4D_INT1 | LIR_INT2 | D4D_INT2 |

Table 29. CTRL_REG5_A description

| | |
|---|---|
| BOOT | Reboot memory content. Default value: 0<br>(0: normal mode, 1: reboot memory content) |
| FIFO_EN | FIFO enable. Default value: 0<br>(0: FIFO disable, 1: FIFO enable) |
| LIR_INT1 | Latch interrupt request on INT1_SRC register, with INT1_SRC register cleared by reading INT1_SRC itself. Default value: 0.<br>(0: interrupt request not latched, 1: interrupt request latched) |
| D4D_INT1 | 4D enable: 4D detection is enabled on INT1 when 6D bit on INT1_CFG is set to 1. |
| LIR_INT2 | Latch interrupt request on INT2_SRC register, with INT2_SRC register cleared by reading INT2_SRC itself. Default value: 0.<br>(0: interrupt request not latched, 1: interrupt request latched) |
| D4D_INT2 | 4D enable: 4D detection is enabled on INT2 when 6D bit on INT2_CFG is set to 1. |

### 7.1.6 CTRL_REG6_A (25h)

Table 30. CTRL_REG6_A register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| I2_CLICKen | I2_INT1 | I2_INT2 | BOOT_I1 | P2_ACT | - - | H_LACTIVE | -- |

Table 31. CTRL_REG6_A description

| | |
|---|---|
| I2_CLICKen | CLICK interrupt on PAD2. Default value 0.<br>(0: disable, 1: enable) |
| I2_INT1 | Interrupt 1 on PAD2. Default value 0.<br>(0: disable, 1: enable) |
| I2_INT2 | Interrupt 2 on PAD2. Default value 0.<br>(0: disable, 1: enable) |
| BOOT_I1 | Reboot memory content on PAD2. Default value: 0<br>(0: disable, 1: enable) |
| P2_ACT | Active function status on PAD2. Default value 0.<br>(0: disable, 1: enable) |
| H_LACTIVE | Interrupt active high, low. Default value 0.<br>(0: active high, 1: active low) |

### 7.1.7 REFERENCE/DATACAPTURE_A (26h)

Table 32. REFERENCE_A register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Ref7 | Ref6 | Ref5 | Ref4 | Ref3 | Ref2 | Ref1 | Ref0 |

**Table 33. REFERENCE_A register description**

| | |
|---|---|
| Ref 7-Ref0 | Reference value for interrupt generation. Default value: 0 |

### 7.1.8 STATUS_REG_A (27h)

**Table 34. STATUS_A register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| ZYXOR | ZOR | YOR | XOR | ZYXDA | ZDA | YDA | XDA |

**Table 35. STATUS_A register description**

| | |
|---|---|
| ZYXOR | X, Y, and Z axis data overrun. Default value: 0<br>(0: no overrun has occurred, 1: a new set of data has overwritten the previous ones) |
| ZOR | Z axis data overrun. Default value: 0<br>(0: no overrun has occurred, 1: a new data for the Z-axis has overwritten the previous one) |
| YOR | Y axis data overrun. Default value: 0<br>(0: no overrun has occurred,<br>1: a new data for the Y-axis has overwritten the previous one) |
| XOR | X axis data overrun. Default value: 0<br>(0: no overrun has occurred,<br>1: a new data for the X-axis has overwritten the previous one) |
| ZYXDA | X, Y, and Z axis new data available. Default value: 0<br>(0: a new set of data is not yet available, 1: a new set of data is available) |
| ZDA | Z axis new data available. Default value: 0<br>(0: a new data for the Z-axis is not yet available,<br>1: a new data for the Z-axis is available) |
| YDA | Y axis new data available. Default value: 0<br>(0: a new data for the Y-axis is not yet available,<br>1: a new data for the Y-axis is available) |
| XDA | X axis new data available. Default value: 0<br>(0: a new data for the X-axis is not yet available,<br>1: a new data for the X-axis is available) |

### 7.1.9 OUT_X_L_A (28h), OUT_X_H_A (29h)

X-axis acceleration data. The value is expressed in 2’s complement.

### 7.1.10 OUT_Y_L_A (2Ah), OUT_Y_H_A (2Bh)

Y-axis acceleration data. The value is expressed in 2’s complement.

### 7.1.11 OUT_Z_L_A (2Ch), OUT_Z_H_A (2Dh)

Z-axis acceleration data. The value is expressed in 2’s complement.

### 7.1.12 FIFO_CTRL_REG_A (2Eh)

**Table 36. REFERENCE_A register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FM1 | FM0 | TR | FTH4 | FTH3 | FTH2 | FTH1 | FTH0 |

**Table 37. REFERENCE_A register description**

| | |
|---|---|
| FM1-FM0 | FIFO mode selection. Default value: 00 (see *Table 38*) |
| TR | Trigger selection. Default value: 0<br>0: trigger event linked to trigger signal on INT1<br>1: trigger event linked to trigger signal on INT2 |
| FTH4:0 | Default value: 0 |

**Table 38. FIFO mode configuration**

| FM1 | FM0 | FIFO mode configuration |
|---|---|---|
| 0 | 0 | Bypass mode |
| 0 | 1 | FIFO mode |
| 1 | 0 | Stream mode |
| 1 | 1 | Trigger mode |

### 7.1.13 FIFO_SRC_REG_A (2Fh)

**Table 39. FIFO_SRC_A register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| WTM | OVRN_FIFO | EMPTY | FSS4 | FSS3 | FSS2 | FSS1 | FSS0 |

### 7.1.14 INT1_CFG_A (30h)

**Table 40. INT1_CFG_A register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| AOI | 6D | ZHIE/ ZUPE | ZLIE/ ZDOWNE | YHIE/ YUPE | YLIE/ YDOWNE | XHIE/ XUPE | XLIE/ XDOWNE |

**Table 41. INT1_CFG_A description**

| | |
|---|---|
| AOI | AND/OR combination of interrupt events. Default value: 0 (refer to *Table 42*) |
| 6D | 6-direction detection function enabled. Default value: 0 (refer to *Table 42*) |
| ZHIE/ ZUPE | Enable interrupt generation on Z high event or on direction recognition. Default value: 0 (0: disable interrupt request, 1: enable interrupt request) |
| ZLIE/ ZDOWNE | Enable interrupt generation on Z low event or on direction recognition. Default value: 0 (0: disable interrupt request, 1: enable interrupt request) |

Table 41. INT1_CFG_A description (continued)

| | |
|---|---|
| YHIE/ YUPE | Enable interrupt generation on Y high event or on direction recognition. Default value: 0 (0: disable interrupt request, 1: enable interrupt request.) |
| YLIE/ YDOWNE | Enable interrupt generation on Y low event or on direction recognition. Default value: 0 (0: disable interrupt request, 1: enable interrupt request.) |
| XHIE/ XUPE | Enable interrupt generation on X high event or on direction recognition. Default value: 0 (0: disable interrupt request, 1: enable interrupt request.) |
| XLIE/XDOWNE | Enable interrupt generation on X low event or on direction recognition. Default value: 0 (0: disable interrupt request, 1: enable interrupt request.) |

Content of this register is loaded at boot. Write operation at this address is possible only after system boot.

Table 42. Interrupt mode

| AOI | 6D | Interrupt mode |
|---|---|---|
| 0 | 0 | OR combination of interrupt events |
| 0 | 1 | 6-direction movement recognition |
| 1 | 0 | AND combination of interrupt events |
| 1 | 1 | 6-direction position recognition |

Difference between AOI-6D = ‘01’ and AOI-6D = ‘11’.

AOI-6D = ‘01’ is movement recognition. An interrupt is generated when orientation moves from unknown zone to known zone. The interrupt signal stays for a duration ODR.

AOI-6D = ‘11’ is direction recognition. An interrupt is generated when orientation is inside a known zone. The interrupt signal stays until orientation is inside the zone.

### 7.1.15 INT1_SRC_A (31h)

Table 43. INT1_SRC_A register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | IA | ZH | ZL | YH | YL | XH | XL |

1. This bit must be set to ‘0’ for correct working of the device.

Table 44. INT1_SRC_A description

| | |
|---|---|
| IA | Interrupt active. Default value: 0<br>(0: no interrupt has been generated, 1: one or more interrupts have been generated) |
| ZH | Z high. Default value: 0<br>(0: no interrupt, 1: Z high event has occurred) |
| ZL | Z low. Default value: 0<br>(0: no interrupt, 1: Z low event has occurred) |
| YH | Y high. Default value: 0<br>(0: no interrupt, 1: Y high event has occurred) |

Table 44. INT1_SRC_A description (continued)

| | |
|---|---|
| YL | Y low. Default value: 0<br>(0: no interrupt, 1: Y low event has occurred) |
| XH | X high. Default value: 0<br>(0: no interrupt, 1: X high event has occurred) |
| XL | X low. Default value: 0<br>(0: no interrupt, 1: X low event has occurred) |

Interrupt 1 source register. Read only register.

Reading at this address clears the INT1_SRC IA bit (and the interrupt signal on the INT 1 pin) and allows the refreshing of data in the INT1_SRC register if the latched option was chosen.

### 7.1.16 INT1_THS_A (32h)

Table 45. INT1_THS_A register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | THS6 | THS5 | THS4 | THS3 | THS2 | THS1 | THS0 |

1. This bit must be set to '0' for correct working of the device.

Table 46. INT1_THS_A description

| | |
|---|---|
| THS6 - THS0 | Interrupt 1 threshold. Default value: 000 0000 |

### 7.1.17 INT1_DURATION_A (33h)

Table 47. INT1_DURATION_A register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

1. This bit must be set to '0' for correct working of the device.

Table 48. INT1_DURATION_A description

| | |
|---|---|
| D6 - D0 | Duration value. Default value: 000 0000 |

**D6 - D0** bits set the minimum duration of the Interrupt 1 event to be recognized. Duration steps and maximum values depend on the ODR chosen.

### 7.1.18 INT2_CFG_A (34h)

Table 49. INT2_CFG_A register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| AOI | 6D | ZHIE | ZLIE | YHIE | YLIE | XHIE | XLIE |

**Table 50. INT2_CFG_A description**

| | |
|---|---|
| AOI | AND/OR combination of interrupt events. Default value: 0<br>(see *Table 51*) |
| 6D | 6-direction detection function enabled. Default value: 0 (refer to *Table 51*) |
| ZHIE | Enable interrupt generation on Z high event. Default value: 0<br>(0: disable interrupt request,<br>1: enable interrupt request on measured accel. value higher than preset threshold) |
| ZLIE | Enable interrupt generation on Z low event. Default value: 0<br>(0: disable interrupt request,<br>1: enable interrupt request on measured accel. value lower than preset threshold) |
| YHIE | Enable interrupt generation on Y high event. Default value: 0<br>(0: disable interrupt request,<br>1: enable interrupt request on measured accel. value higher than preset threshold) |
| YLIE | Enable interrupt generation on Y low event. Default value: 0<br>(0: disable interrupt request,<br>1: enable interrupt request on measured accel. value lower than preset threshold) |
| XHIE | Enable interrupt generation on X high event. Default value: 0<br>(0: disable interrupt request,<br>1: enable interrupt request on measured accel. value higher than preset threshold) |
| XLIE | Enable interrupt generation on X low event. Default value: 0<br>(0: disable interrupt request,<br>1: enable interrupt request on measured accel. value lower than preset threshold) |

**Table 51. Interrupt mode**

| AOI | 6D | Interrupt mode |
|---|---|---|
| 0 | 0 | OR combination of interrupt events |
| 0 | 1 | 6-direction movement recognition |
| 1 | 0 | AND combination of interrupt events |
| 1 | 1 | 6-direction position recognition |

Difference between AOI-6D = ‘01’ and AOI-6D = ‘11’.

AOI-6D = ‘01’ is movement recognition. An interrupt is generated when orientation moves from unknown zone to known zone. The interrupt signal stays for a duration ODR.

AOI-6D = ‘11’ is direction recognition. An interrupt is generated when orientation is inside a known zone. The interrupt signal stays until orientation is inside the zone.

### 7.1.19 INT2_SRC_A (35h)

**Table 52. INT2_SRC_A register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | IA | ZH | ZL | YH | YL | XH | XL |

1. This bit must be set to ‘0’ for correct working of the device.

**Table 53. INT2_SRC_A description**

| | |
|---|---|
| IA | Interrupt active. Default value: 0<br>(0: no interrupt has been generated, 1: one or more interrupts have been generated) |
| ZH | Z high. Default value: 0<br>(0: no interrupt, 1: Z high event has occurred) |
| ZL | Z low. Default value: 0<br>(0: no interrupt, 1: Z low event has occurred) |
| YH | Y high. Default value: 0<br>(0: no interrupt, 1: Y high event has occurred) |
| YL | Y low. Default value: 0<br>(0: no interrupt, 1: Y low event has occurred) |
| XH | X high. Default value: 0<br>(0: no interrupt, 1: X high event has occurred) |
| XL | X Low. Default value: 0<br>(0: no interrupt, 1: X low event has occurred) |

Interrupt 2 source register. Read only register.

Reading at this address clears INT2_SRC IA bit (and the interrupt signal on the INT 2 pin) and allows the refreshing of data in the INT2_SRC register if the latched option was chosen.

### 7.1.20 INT2_THS_A (36h)

**Table 54. INT2_THS_A register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | THS6 | THS5 | THS4 | THS3 | THS2 | THS1 | THS0 |

1. This bit must be set to '0' for correct working of the device

**Table 55. INT2_THS_A description**

| | |
|---|---|
| THS6 - THS0 | Interrupt 1 threshold. Default value: 000 0000 |

### 7.1.21 INT2_DURATION_A (37h)

**Table 56. INT2_DURATION_A register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

1. This bit must be set to '0' for correct working of the device

**Table 57. INT2_DURATION_A description**

| | |
|---|---|
| D6-D0 | Duration value. Default value: 000 0000 |

**D6 - D0** bits set the minimum duration of the Interrupt 2 event to be recognized. Duration time steps and maximum values depend on the ODR chosen.

### 7.1.22 CLICK_CFG_A (38h)

**Table 58. CLICK_CFG_A register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| -- | -- | ZD | ZS | YD | YS | XD | XS |

**Table 59. CLICK_CFG_A description**

| | |
|---|---|
| ZD | Enable interrupt double CLICK on Z axis. Default value: 0<br>(0: disable interrupt request, 1: enable interrupt request on measured accel. value higher than preset threshold) |
| ZS | Enable interrupt single CLICK on Z axis. Default value: 0<br>(0: disable interrupt request, 1: enable interrupt request on measured accel. value higher than preset threshold) |
| YD | Enable interrupt double CLICK on Y axis. Default value: 0<br>(0: disable interrupt request, 1: enable interrupt request on measured accel. value higher than preset threshold) |
| YS | Enable interrupt single CLICK on Y axis. Default value: 0<br>(0: disable interrupt request, 1: enable interrupt request on measured accel. value higher than preset threshold) |
| XD | Enable interrupt double CLICK on X axis. Default value: 0<br>(0: disable interrupt request, 1: enable interrupt request on measured accel. value higher than preset threshold) |
| XS | Enable interrupt single CLICK on X axis. Default value: 0<br>(0: disable interrupt request, 1: enable interrupt request on measured accel. value higher than preset threshold) |

### 7.1.23 CLICK_SRC_A (39h)

**Table 60. CLICK_SRC_A register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| -- | IA | DCLICK | SCLICK | Sign | Z | Y | X |

**Table 61. CLICK_SRC_A description**

| | |
|---|---|
| IA | Interrupt active. Default value: 0<br>(0: no interrupt has been generated, 1: one or more interrupts have been generated) |
| DCLICK | Double CLICK-CLICK enable. Default value: 0 (0:double CLICK-CLICK detection disable, 1: double CLICK-CLICK detection enable) |
| SCLICK | Single CLICK-CLICK enable. Default value: 0 (0:Single CLICK-CLICK detection disable, 1: single CLICK-CLICK detection enable) |
| Sign | CLICK-CLICK Sign. 0: positive detection, 1: negative detection |

Table 61. CLICK_SRC_A description (continued)

| | |
|---|---|
| Z | Z CLICK-CLICK detection. Default value: 0<br>(0: no interrupt, 1: Z high event has occurred) |
| Y | Y CLICK-CLICK detection. Default value: 0<br>(0: no interrupt, 1: Y high event has occurred) |
| X | X CLICK-CLICK detection. Default value: 0<br>(0: no interrupt, 1: X high event has occurred) |

### 7.1.24 CLICK_THS_A (3Ah)

Table 62. CLICK_THS_A register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| -- | Ths6 | Ths5 | Ths4 | Ths3 | Ths2 | Ths1 | Ths0 |

Table 63. CLICK_SRC_A description

| | |
|---|---|
| Ths6-Ths0 | CLICK-CLICK threshold. Default value: 000 0000 |

1 LSB = full-scale / 128. THS6 through THS0 define the threshold which is used by the system to start the click detection procedure. The threshold value is expressed over 7 bits as an unsigned number.

### 7.1.25 TIME_LIMIT_A (3Bh)

Table 64. TIME_LIMIT_A register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| -- | TLI6 | TLI5 | TLI4 | TLI3 | TLI2 | TLI1 | TLI0 |

Table 65. TIME_LIMIT_A description

| | |
|---|---|
| TLI7-TLI0 | CLICK-CLICK time limit. Default value: 000 0000 |

1 LSB = 1/ODR. TLI7 through TLI0 define the maximum time interval that can elapse between the start of the click detection procedure (the acceleration on the selected channel exceeds the programmed threshold) and when the acceleration goes back below the threshold.

### 7.1.26 TIME_LATENCY_A (3Ch)

Table 66. TIME_LATENCY_A register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| TLA7 | TLA6 | TLA5 | TLA4 | TLA3 | TLA2 | TLA1 | TLA0 |

Table 67. TIME_LATENCY_A description

| | |
|---|---|
| TLA7-TLA0 | CLICK-CLICK time latency. Default value: 000 0000 |

1 LSB = 1/ODR. TLA7 through TLA0 define the time interval that starts after the first click detection where the click detection procedure is disabled, in cases where the device is configured for double click detection.

### 7.1.27 TIME WINDOW_A (3Dh)

**Table 68. TIME_WINDOW_A register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| TW7 | TW6 | TW5 | TW4 | TW3 | TW2 | TW1 | TW0 |

**Table 69. TIME_WINDOW_A description**

| | |
|---|---|
| TW7-TW0 | CLICK-CLICK time window |

1 LSB = 1/ODR. TW7 through TW0 define the maximum interval of time that can elapse after the end of the latency interval in which the click detection procedure can start, in cases where the device is configured for double click detection.

## 7.2 Magnetic field sensing register description

### 7.2.1 CRA_REG_M (00h)

**Table 70. CRA_REG_M register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| TEMP_EN | 0(1) | 0(1) | DO2 | DO1 | DO0 | 0(1) | 0(1) |

1. This bit must be set to '0' for correct working of the device

**Table 71. CRA_REG_M description**

| | |
|---|---|
| TEMP _EN | Temperature sensor enable.<br>0: temperature sensor disabled (default), 1: temperature sensor enabled |
| DO2 to DO0 | Data output rate bits. These bits set the rate at which data is written to all three data output registers (refer to *Table 72*). Default value: 100 |

**Table 72. Data rate configurations**

| DO2 | DO1 | DO0 | Minimum data output rate (Hz) |
|---|---|---|---|
| 0 | 0 | 0 | 0.75 |
| 0 | 0 | 1 | 1.5 |
| 0 | 1 | 0 | 3.0 |
| 0 | 1 | 1 | 7.5 |
| 1 | 0 | 0 | 15 |
| 1 | 0 | 1 | 30 |

Table 72. Data rate configurations (continued)

| DO2 | DO1 | DO0 | Minimum data output rate (Hz) |
|---|---|---|---|
| 1 | 1 | 0 | 75 |
| 1 | 1 | 1 | 220 |

### 7.2.2 CRB_REG_M (01h)

Table 73. CRA_REG register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| GN2 | GN1 | GN0 | 0(1) | 0(1) | 0(1) | 0(1) | 0(1) |

1. This bit must be set to '0' for correct working of the device.

Table 74. CRA_REG description

| | |
|---|---|
| GN1-0 | Gain configuration bits. The gain configuration is common for all channels (refer to *Table 75*) |

Table 75. Gain setting

| GN2 | GN1 | GN0 | Sensor input field range [Gauss] | Gain X, Y, and Z [LSB/Gauss] | Gain Z [LSB/Gauss] | Output range |
|---|---|---|---|---|---|---|
| 0 | 0 | 1 | ±1.3 | 1100 | 980 | 0xF800–0x07FF (-2048–2047) |
| 0 | 1 | 0 | ±1.9 | 855 | 760 | |
| 0 | 1 | 1 | ±2.5 | 670 | 600 | |
| 1 | 0 | 0 | ±4.0 | 450 | 400 | |
| 1 | 0 | 1 | ±4.7 | 400 | 355 | |
| 1 | 1 | 0 | ±5.6 | 330 | 295 | |
| 1 | 1 | 1 | ±8.1 | 230 | 205 | |

### 7.2.3 MR_REG_M (02h)

Table 76. MR_REG

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | 0(1) | 0(1) | 0(1) | 0(1) | MD1 | MD0 |

1. This bit must be set to '0' for correct working of the device.

Table 77. MR_REG description

| | |
|---|---|
| MD1-0 | Mode select bits. These bits select the operation mode of this device (refer to *Table 78*) |

Table 78. Magnetic sensor operating mode

| MD1 | MD0 | Mode |
|---|---|---|
| 0 | 0 | Continuous-conversion mode |
| 0 | 1 | Single-conversion mode |
| 1 | 0 | Sleep-mode. Device is placed in sleep-mode |
| 1 | 1 | Sleep-mode. Device is placed in sleep-mode |

### 7.2.4 OUT_X_H_M (03), OUT_X_LH_M (04h)

X-axis magnetic field data. The value is expressed as 2's complement.

### 7.2.5 OUT_Z_H_M (05), OUT_Z_L_M (06h)

Z-axis magnetic field data. The value is expressed as 2's complement.

### 7.2.6 OUT_Y_H_M (07), OUT_Y_L_M (08h)

Y-axis magnetic field data. The value is expressed as 2's complement.

### 7.2.7 SR_REG_M (09h)

Table 79. SR register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| -- | -- | -- | -- | -- | -- | LOCK | DRDY |

Table 80. SR register description

| | |
|---|---|
| LOCK | Data output register lock. Once a new set of measurements is available, this bit is set when the first magnetic file data register has been read. |
| DRDY | Data ready bit. This bit is when a new set of measurements are available. |

### 7.2.8 IR_REG_M (0Ah/0Bh/0Ch)

Table 81. IRA_REG_M

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |

Table 82. IRB_REG_M

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |

Table 83. IRC_REG_M

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |

### 7.2.9 TEMP_OUT_H_M (31h), TEMP_OUT_L_M (32h)

**Table 84. TEMP_OUT_H_M register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| TEMP11 | TEMP10 | TEMP9 | TEMP8 | TEMP7 | TEMP6 | TEMP5 | TEMP4 |

**Table 85. TEMP_OUT_L_M register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| TEMP3 | TEMP2 | TEMP1 | TEMP0 | -- | -- | -- | -- |

**Table 86. TEMP_OUT resolution**

| | |
|---|---|
| TEMP11-0 | Temperature data (8LSB/deg - 12-bit resolution). The value is expressed as 2's complement. |

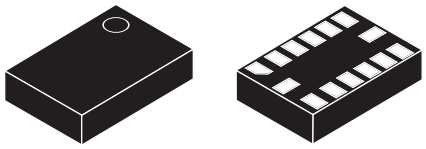
# 8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

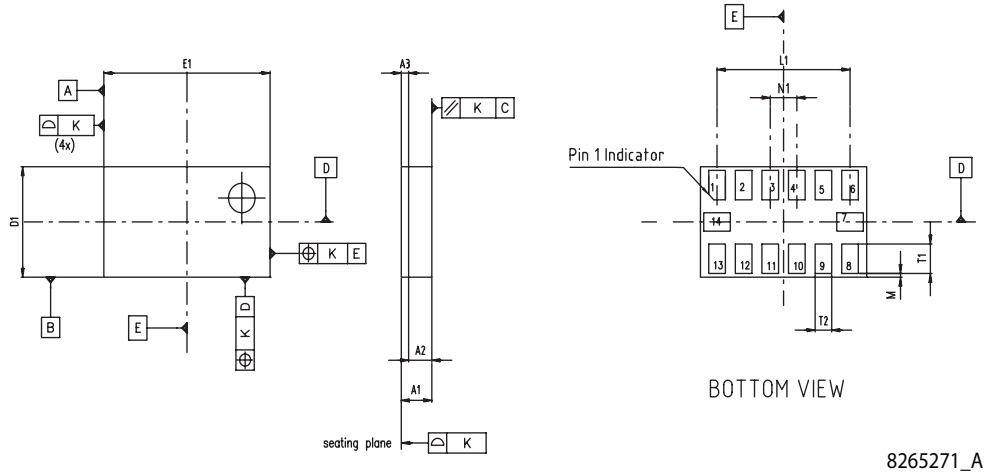
**Figure 5. LGA-14: mechanical data and package dimensions**

| Dimensions | | | |
|---|---|---|---|
| Ref. | mm | | |
| | Min. | Typ. | Max. |
| A1 | | | 1 |
| A2 | | 0.785 | |
| A3 | 0.16 | 0.2 | 0.24 |
| D1 | 2.85 | 3 | 3.15 |
| E1 | 4.85 | 5 | 5.15 |
| N1 | | 0.8 | |
| L1 | | 4 | |
| T1 | | 0.8 | |
| T2 | | 0.5 | |
| M | | 0.1 | |
| k | | 0.05 | |

Outline and mechanical data



**LGA 3x5x1 14L**
**Land Grid Array Package**



# 9 Revision history

Table 87. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 21-Apr-2011 | 1 | Initial release. |

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