OpenCPI HDL Device Workers Interface Specification

Authors:
Shepard Siegel, Atomic Rules LLC   (Shepard.Siegel@atomicrules.com)
Jim Kulp, Mercury Federal Systems, Inc. (jkulp@mercfed.com)

Revision History

Revision	Description of Change	By	Date
1.01	Creation	jkulp	2010-07-01
1.02	Added TimeGate documentation	Ssiegel	2010-08-16
1.03	Fixed omission of Tme Trigger in ADC and DAC	Ssiegel	2010-08-24

Table of Contents

1 References

This document depends on several others. Primarily, it depends on the “OpenCPI Generic Authoring Model Reference Manual”, which describes concepts and definitions common to all OpenCPI authoring models, and the “OpenCPI HDL Authoring Model Reference” which describes how HDL workers must be written.

Title	Published By	Link
OpenCPI Authoring Model Reference	OpenCPI	Public URL: http://www.opencpi.org/doc/amr.pdf
OpenCPI HDL Authoring Model Reference	OpenCPI	Public URL: http://www.opencpi.org/doc/hdlamr.pdf

2 Overview

This document describes OpenCPI HDL ***device workers***, which are IP blocks for FPGAs that on the "front" side present standard OpenCPI WIP-profile interfaces for use by applications, and on the "back" side attach to external devices via pins of the FPGA. They are essentially the "device drivers" for OpenCPI FPGA platforms. They are "optional" in the sense that, for a given FPGA platform, they are only required to be included in the bitstream design if the HDL application (the collection of interconnected application workers) actually needs them. This is in contrast to the core OpenCPI infrastructure IP that is required as a basis for all OpenCPI application bitstreams (described in a different document).

Thus one view of these device workers is they are "just workers", like application workers, in that they are controlled by WCI (as defined in [HDLAMR]), have configuration properties and control operations, and, when they act in the data plane, they have WIP data plane interfaces that consume or produce.

OpenCPI device workers support devices externally attached to FPGAs for reasons *other than* providing the core platform for all applications (like PCI Express and basic timekeeping).

Configuration properties shaded in yellow are meant only for debugging and can be "compiled out" when not desired, to save resources. Configuration property offsets for device workers may have an asterisk indicating that there is are gaps in the offsets.

As with all HDL workers, all device workers must follow the control pattern defined in the HDL Authoring Model Reference [HDLAMR]:

- First, workers are "taken out of reset", by deasserting the OCP MReset_n signal on its WCI OCP Slave interface. Per OCP, this reset signal may only be asserted for 16 clock cycles.
- Next, if explicitly supported by the worker (as indicated in the metadata), the ***Initialize*** control operation is performed. The worker *must not* complete the initialize operation (via the OCP response on the WCI), until it is ready to be started or has an initialization error.
- Finally, the ***Start*** control operation is performed to cause the worker to begin operating (enter the operational state).
- For its application interfaces (not WCI, but WSI, WMI, or WMemI) the device worker must tolerate a reset input assertion on that application interface without requiring re-initialization or re-start.
- Like all non-application workers, device workers are initialized and started before any attached application workers are taken out of reset, initialized and started.

Device Workers are instanced outside the OpenCPI application, and container, in what is known as FTop' (FTop-prime). This is the outer set of optionally instanced IP blocks in the OpenCPI HDL Architecture that are attached to external devices via pins of the FPGA. While Ftop (not prime) contains core functions required by all HDL applications, FTop' (Ftop-prime) contains optional device workers that are needed only by some applications. See Figure 1 below.

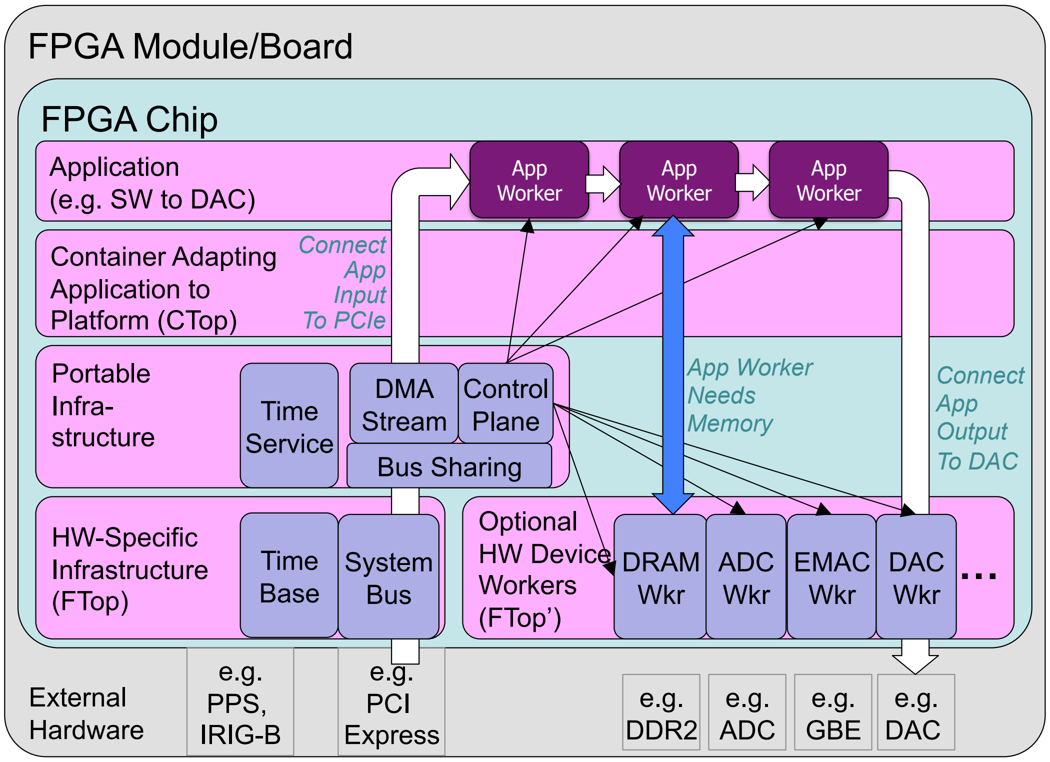

Figure 1: OpenCPI FPGA Architecture

3 DRAM Device Worker

3.1 *Function Performed*

This device worker provides access to external DDR2 SDRAM via a WMemI profile interface. It is based on the MIG memory controller from Xilinx, for both V5 and V6.

3.2 *Configuration Properties*

Property Offset	Property Name	Access	Description
+0x0000	dramStatus	RO	No user-useful status at this time
+0x0004	drmCtrl	RW	No user control at this time
+0x0008	dbg_calib_done	RO	
+0x000C	dbg_calib_err	RO	
+0x0010	dbg_calib_dq_tap_cnt	RO	
+0x0014	dbg_calib_dqs_tap_cnt	RO	
+0x0018	dbg_calib_gate_tap_cnt	RO	
+0x001C	dbg_calib_rd_data_sel	RO	
+0x0020	dbg_calib_ren_delay	RO	
+0x0024	dbg_calib_gate_delay	RO	
+0x0028	32'hCODE_BABE	RO	
+0x002C	wmemiWrReq	RO	
+0x0030	wmemiRdReq	RO	
+0x0034	wmemiRdResp	RO	
+0x0038	wmemi.status	RO	
+0x003C	Wmemi.ReadInFlight	RO	
+0x0048*	requestCount	RO	
+0x0050*	pReg	RW	
+0x0054	4B WRITE PIO	WO	
+0x0058	4B READ PIO	WO	
+0x005C	mReg	RW	
+0x0060	wdReg[0]	RO	
+0x0064	wdReg[1]	RO	
+0x0068	wdReg[2]	RO	
+0x006C	wdReg[3]	RO	
+0x0080	rdReg[0]	RO	
+0x0084	rdReg[1]	RO	
+0x0088	rdReg[2]	RO	
+0x008C	rdReg[3]	RO	

** Gaps in offsets exist before this property*

3.3 Using the DRAM Device Worker

The DRAM Device Worker provides a DRAM controller allowing a paged, flat-map on a WMemI slave port for use by application workers. Like all device workers, this device worker must be successfully initialized (it if implements the “initialize” control operation) and started before use. This allows the DRAM Device Worker to perform DRAM PHY training etc., which is a process that cannot be done under OCP reset.

This device worker provides memory to other workers. When a container is constructed for an HDL application that contains workers that require memory (and thus have a WMemI master interface), the container would provide the connection between the WMemI master interface of the HDL application and the application worker inside the application.   See the blue arrow in figure 1 above. The container would be responsible for any necessary adaptation between the WMemI master interface’s profile attributes (chosen by the implementer of the application worker needing memory), and the profile attributes of the DRAM device worker (chosen by the implementer of the DRAM device worker).

The WIP profile attributes of the WMemI interface of the DRAM device worker are:

Attribute Name	Attribute Value	Comments
DataWidth	128	
ByteWidth	8	Typical 8-bit byte-oriented write-enables
MemoryWords	4G	Supported memory is smaller than this
MaxBurstLengh	4K – 1	
PreciseBurst	true	No support for imprecise bursts
WriteDataFlowControl	true	Writes are flow controlled per word
ReadDataFlowControl	false	Using worker must accept whole read burst

4 OpenCPI A/D and D/A Device Worker Control (General Topic)

OpenCPI has generalized analog-to-digital (A/D) collection and digital-to-analog (D/A) emission capabilities that can be specialized for specific boards and devices. Control of these ADC and DAC device workers is performed with a first-class notion of actual time, as provided by the HDL time service. Both the ADC and DAC workers share a similar control paradigm for gating the ingress or egress of sample data to or from an asynchronous message domain (the OpenCPI "Data Plane"). Described below are the methods and properties for controlling ingress (collection) and egress (emission) across the sample/message (isochronous/asynchronous) boundary. The ***TimeGate*** module is a common capability used by both ADC and DAC device workers. It implements the time-based control and gating paradigm.

4.1 Time-based Control Scheme for the flow of ADC/DAC sample data

No samples shall cross the sample/message boundary, unless the ADC/DAC worker is in the "Operating" state, entered by the ***Start*** control operation, and exited by the ***Stop*** or ***Release*** control operation. In the "Operating" state, the movement of sample data is initiated by a ***Trigger Event***, which may be any combination of:

Start Control Operation: The completion of the "start" control operation may initiate sample data flow if other properties are setup with no other gating or conditions. In any case it is a precondition for sample data flow.

Software Trigger: A configuration property write to specifically enable sample data flow

Trigger Time Condition: An absolute time that specifies when the trigger should initially occur (as supplied from the HDL Time Service via an HDL Time Client).

External Trigger In: An external input event to the FPGA device used as a trigger

A ***Trigger Output*** signal (that can be external to the FPGA) is provided to synchronize other devices to the ***trigger event***.

The properties that may be set to further determine the flow of sample data are:

Dwell: specifies a time duration over which sample data will flow. It can be thought of as "how long" to be collecting or emitting active signal samples before pausing. A zero dwell duration is the default special case that describes infinite dwell: sample data flows until explicitly stopped.

Offset: specifies the time delay from the ***trigger event*** to the start of the sample data movement (to start of dwell).

Period: From the ***trigger event***, a non-zero periodic repeat duration as an interval that will pass before the repeat of the trigger/offset/dwell pattern (the time interval between ***trigger events*** after the initial one). A zero periodic repeat duration is the default special case that describes no repeat at all. The end of a non-zero periodic interval generates a new ***trigger event***.

To minimize latency, and latency-uncertainty (jitter), the effective sample/message boundary must be placed as close to the actual converter circuitry as possible.

The sample/message boundaries are strict, transactional barriers. Failure to successfully ingress a sample to message (“overrun” in an ADC Worker); or egress a message to sample (“underrun” in a DAC Worker), will be recorded and will raise a WCI attention. Conversely, status indication in these device workers records the messages and samples successfully processed.

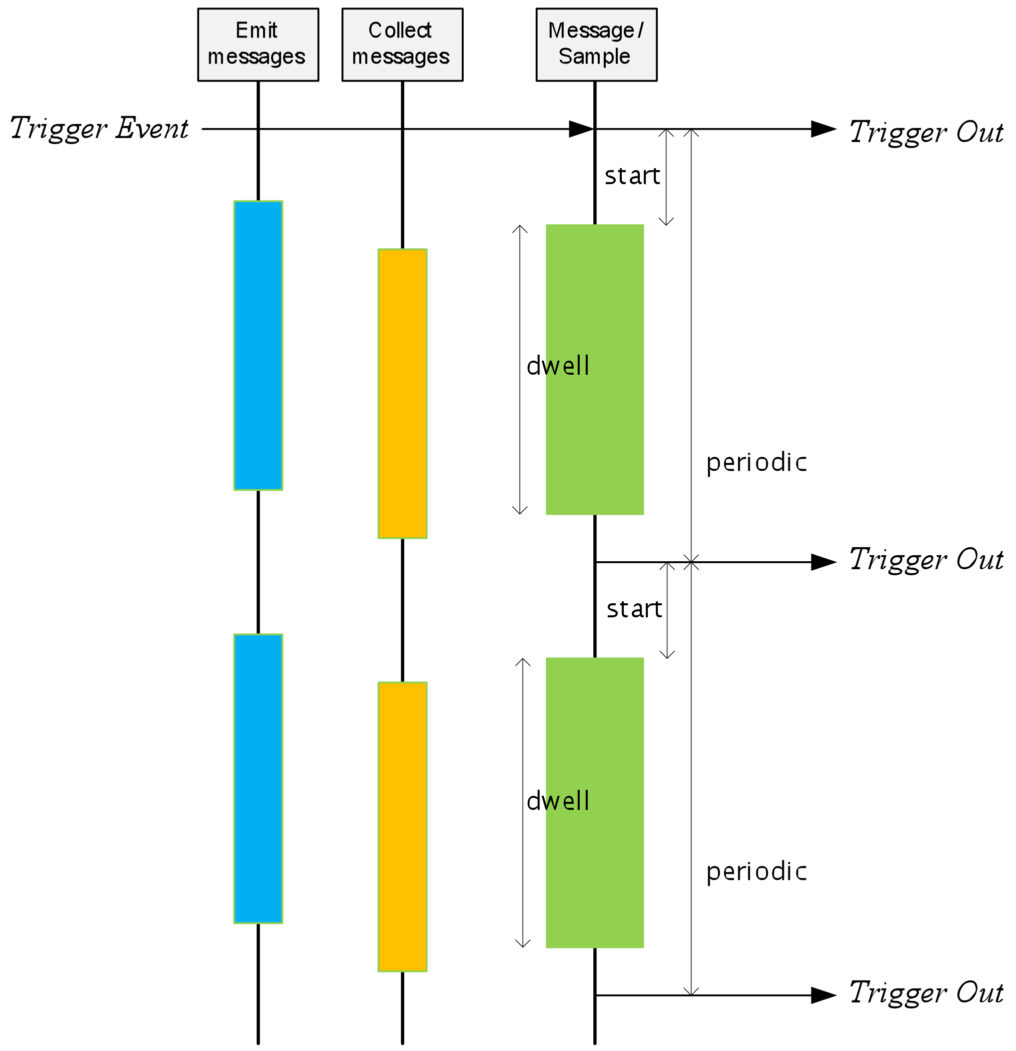

Figure 1 – Time Sequence Diagram of Message/Sample Boundary

The time sequence diagram above shows the following key relationships:

- *A trigger event causes a trigger output and establishes a start line*
- *A non-zero **period** creates an endless repetition of the start line*
- *An offset of **start offset** is inserted before data is allowed to cross the sample/message barrier*
- *Data crosses the sample/message boundary for the duration of **dwell** (Green)*
- *Messages arriving for emission need to arrive in time (Light Blue)*
- *Messages departing from collection leave as soon as possible (Orange)*

4.2 Programming the TimeGate module

Device workers such as the ADC Device Worker and DAC Device Worker containing an isochronous-to-asynchronous boundary employ a consistent method for programming either the single-shot or periodic dwell interval. Two “banks” of 4 properties, ‘A’ and ‘B’, allow one bank to be updated while the other is in operation. The selection of which bank is active is made in a separate control property. Thus changing which bank is being used atomically changes all 4 parameters. These properties are placed in the property space of any device worker that uses the TimeGate module.

Timegate Properties:

Property Sub-Offset	Property Name	Access	Description
+0x0_0000	tgCtrl_A	RW	Control (see below) – Bank A
+0x0_0004	tgStart_A	RW	Offset in sample clocks– Bank A
+0x0_0008	tgDwell_A	RW	Dwell in sample clocks – Bank A
+0x0_000C	tgPeriod_A	RW	Period in sample clocks – Bank A
+0x0_0010	tgCtrl_B	RW	Control (see below) – Bank B
+0x0_0014	tgStart_B	RW	Offset in sample clocks – Bank B
+0x0_0018	tgDwell_B	RW	Dwell in sample clocks – Bank B
+0x0_001C	tgPeriod_B	RW	Period in sample clocks – Bank B

Control register bit definitions:

Bits	Name	Access	Description
31:8		Reserved	0
7:3	syncEn	RW	Sync Enable. A ‘1’ enables a particular sync source[3:0]. Source 0 = ext 0 Source 1 = ext 1 Source 2 = Absolute Time Trigger Source 3 = Software Trigger
3:2		Reserved	
1	periodic	RW	0=Disables the tgPeriod specified periodic self-triggering 1= Enables the tgPeriod specified periodic self-triggering
0	gatedDwell	RW	0=Ungated, data moves when worker enabled 1=Gated Dwell, Dwell is generated from timegate logic

5 ADC Device Worker

5.1 Function performed

Like any other OpenCPI worker, the ADC device worker is controlled by its WCI interface (INITALIZE, START, etc); and its operation is configured by configuration properties. It accepts clock and data from an ADC (or ADCs); and produces a WSI-Master message stream output.

Following initialization and configuration, the ADC Device Worker produces several types of messages, identified by opcode. The types of messages produced, and how often they are emitted, are controlled by configuration properties. The amount of data produced by the WSI-Master is deterministic based on configuration property settings and the frequency of the ADC clock (which can be observed by reading a configuration property). A finite-sized FIFO buffers the short-term rate differences and clock domain crossing. This FIFO will overflow if the connected WSI-Slave cannot sustain consumption of the produced ADC device worker messages. When that overrun error condition occurs, it is recorded.

The ADC worker is a client of the HDL Time Service. As such the ADC worker may be programmed by configuration properties to optionally insert time information at the start of ADC sample data. Independently, the ADC Worker may be set to send discrete, periodic in-band “beacon” Time messages.

The ADC worker may be triggered, or re-triggered, by several means, including setting specific configuration properties, or the arrival of enabled synchronization (“sync”) signals (see TimeGate description above). Each time the ADC worker is triggered to acquire, it will produce a capture frame of data. A capture frame of data is comprised of **numMesgPerFrame** messages, each of **fixedMesgSize**. The product of these two configuration properties are the number of Bytes in the capture frame. This is directly related to the number of ADC samples, and to the so-called “dwell time” of continuous acquisition through the ADC sample clock. While the ADC device worker exposes the fixedMesgSize through every message sent, the count of numMesgPerFrame is not exported. It is used locally to simply count off how many messages to send in a frame of dwell.

Opcode	Message Type	Length	Description
0	Sample	Varies	On a 4B (32b) WSI link, two 16b ADC samples (N+1) and N are packed little-endian into a DWORD. Sample$_{N+1}$ is in bits [31:16], Sample$_N$ is in [15:0]. When the converter data is less than 16b, the data from the converter is MSB justified, with zeros in the LSBs. These are (typically) imprecise messages whose length will not exceed the configuration property “maxMesgLength”. Transmission of this message is enabled by default; it may be inhibited by setting the control bit disableSample.
1	Sync	0B	A Zero-Length message that is used to indicate a synchronization event. These events indicate sampling discontinuities, such as at the start of acquisition, or when acquisition is gated. Transmission of this message is disabled by default; it may be enabled by setting the control bit enableSync.

2	Timestamp	24B	A 24B message that conveys the timestamp and supporting information.
			
			`typedef struct {`
			`  Bit#(32) iSeconds;      // “now”: integer Seconds`
			`  Bit#(32) fSeconds;      // “now”: fractional Seconds`
			`  Bit#(32) dropCount;     // Rolling count of dropped samples`
			`  Bit#(32) sampCnt;       // Rolling count of captured samples`
			`  Bit#(32) dwellStarts;   // Rolling count of dwell starts`
			`  Bit#(32) dwellFails;    // Rolling count of dwell failures`
			`} SampMessage`
			
			Transmission of this message is disabled by default; it may be enabled by setting the control bit enableTimestamp.

5.2 Configuration Properties

This section describes the configuration properties of the ADC Device Worker.

Property Offset (B)	Property Name	Access	Description
+0x0_0000	wsiM Status	RO	WSI-M Port status in bits[7:0]
+0x0_0004	adcStatusLS	RO	See ADC Status Bits[31:0] Table TBD
+0x0_0008	maxMesgLength	RW	ADC Data maximum message length (in Bytes), multiples of 4B, $4 <= maxMesgLength <= 65532$
+0x0_000C	adcControl	RW	See ADC Control Bits
+0x0_0010		RO	rsvd
+0x0_0014	fcAdc	RO	Measured Frequency of ADC Sample Clock (in KHz, updated at 1KHz)
+0x0_0018	adcSampleEnq	RO	Rolling 32b count of ADC Samples ENQ in capture domain
+0x0_001C	sampleSpy0	RO	Last two samples from ADC0 (little endian) {second:first}
+0x0_0020	sampleSpy1	RO	Last two samples from ADC1 (little endian) {second:first}
+0x0_0024	spiClock	WO	Issue indirect-IO SPI command to Clock
+0x0_0028	spiAdc0	WO	Issue indirect-IO SPI command to ADC0
+0x0_002C	spiAdc1	WO	Issue indirect-IO SPI command to ADC1
+0x0_0030	spiResponse	RO	Last Response from an SPI Read Command
+0x0_0034	mesgCount	RO	Rolling 32b count of WSI messages sent (all opcodes)
+0x0_0038		RO	
+0x0_003C	Stats.dwellStarts	RO	Number of Dwell intervals Started
+0x0_0040	Stats.dwellFails	RO	Number of Dwell intervals Failed
+0x0_0044	lastOverflowMesg	RO	Value of mesgCount when buffer overflow last occurred
+0x0_0048	phaseCmdAdc0	WO	ADC0 Phase Shift (b1=ENA, b0=INC)
+0x0_004C	phaseCmdAdc1	WO	ADC1 Phase Shift (b1=ENA, b0=INC)
+0x0_0050	extStatus.pMesgCount	RO	Precise Messages Generated
+0x0_0054	extStatus.iMesgCount	RO	Imprecise Messages Generated
+0x0_0058	Stats.dropCount	RO	Samples Dropped
+0x0_005C	dwellFails	RO	Dwell intervals where samples were dropped
+0x0_0060 – 0x0_007C	TimeGate Control	RW	See TimeGate Control description
+0x0_0080 – 0x0_0084	triggerTime	RW	ADC Absolute Trigger Time in 32.32 format
+0x0_0088	softwareTrigger	WO	Write 0xC0DE_AAEE to trigger ADC (when enabled)

+0x0_0400 – 0x0_04FC	ADC0 SPI	RW	Memory Map of 1KB ADC0 device control space
+0x0_0800 – 0x0_08FC	ADC1 SPI	RW	Memory Map of 1KB ADC1 device control space
+0x0_0C00 – 0x0_0CFC	Clock SPI	RW	Memory Map of 1KB Clock device control space

5.2.1 adcControl (ADCWorker +0x0_000C)

This register controls the overall behavior of the ADC device worker. The initial value is zero.

Bits	Name	Access	Description
31:6		Reserved	0
5	timeGateBank	RW	0=Use TimeGate bank A 1=Use TimeGate bank B
4	average4	RW	0=Normal operation 1=The ADC outputs one averaged sample for every four digitized
3	inhibitOnDrop	RW	0=Continue acquire if samples dropped 1=Inhibit acquire if samples are dropped
2	enableTimestamp	RW	0=Inhibit Transmission of Timestamp messages 1=Allow Transmission of Timestamp messages (Opcode 2)
1	enableSync	RW	0=Inhibit Transmission of Sync messages 1=Allow Transmission of Sync messages (Opcode 1)
0	disableSample	RW	0=Allow Transmission of ADC data messages 1=Inhibit Transmission of ADC data messages (Opcode 0)

5.2.2 fcAdc (ADCWorker +0x0_0014)

The measured frequency (in KHz) of the ADC sample clock.

5.2.3 adcSampleCount (ADCWorker +0x0_0018)

A rolling 32b count of ADC Sample clocks observed.

5.3 Using the ADC Worker

With its default settings, the ADC worker will start producing data messages (Opcode 0) as soon as the Start control operation is performed. Other bits in the control property enable the two other opcodes: Sync (sample discontinuity) and Time (Time of following sample). Whether an overrun (samples dropped) stops the acquisition is another option.

6 DAC Device Worker

6.1 *Function Performed*

The DAC device worker accepts data from a WSI input and sends 16-bit data samples in the messages to the DAC. When the DAC device accepts fewer than 16 bits per sample, then the MSBs of the arriving 16 bits are presented to the DAC device.

6.2 *Configuration Properties*

This section describes the configuration properties of the DACWorker.

Property Offset (B)	Property Name	Access	Description
+0x0_0000	dacStatusMS	RO	See DAC Status Bits[63:32] [7:0] WSI-S port status
+0x0_0004	dacStatusLS	RO	See DAC Status Bits[31:0]
+0x0_0008		RO	
+0x0_000C	dacControl	RW	See DAC Control Bits
+0x0_0010	fcDac	RO	Measured Frequency of DAC Sample Clock (1/16 F_{DAC}) (in KHz, updated at 1KHz)
+0x0_0014	dacSampleDeq	RO	Rolling 32b count of Samples DEQ in emitter domain
+0x0_0018		RO	
+0x0_001C		RO	
+0x0_0020		RO	
+0x0_0024	firstUnderrunMesg	RO	mesgStart where underflowCount first became non-zero
+0x0_0028		RO	
+0x0_002C		RO	
+0x0_0030	syncCount	RO	Rolling 32b count of "Opcode 3" Sync Received
+0x0_0034	mesgStart	RO	Rolling 32b count WSI message Starts Received
+0x0_0038	underflowCount	RO	Rolling 32b count of underflows (16-samples per LSB)
+0x0_003C	stageCount	RO	Rolling 32b count of enqueues (16-samples per LSB)
+0x0_0040		RO	
+0x0_0044		RO	
+0x0_0048	pMesgCount	RO	WSI-S Precise Messages Received
+0x0_004C	iMesgCount	RO	WSI-S Imprecise Messages Received
+0x0_0050	tBusyCount	RO	WSI-S Rolling Count of SThreadBusy backpressure

+0x0_0060 - 0x0_007C	TimeGate Control	RW	See TimeGate Control description
+0x0_0080–0x0_0084	triggerTime	RW	DAC Absolute Trigger Time Register 32.32 format
+0x0_0088	softwareTrigger	WO	Write 0xC0DE_AAEE to trigger DAC (when enabled)

6.2.1 dacControl (DACWorker +0x0_000C)

This register controls the overall behavior of the DAC device worker.

Bits	Name	Access	Description
31:9		Reserved	0
8	timeGateBank	RW	0=Use TimeGate bank A 1=Use TimeGate bank B
7	toneEn	RW	0=Disable; 1= F_{DAC}/16 CW Tone (Write 0x88 to dacControl)
6	invertMSBs	RW	0=NOP; 1= Invert MSBs (dual-sample b31 and b15)
5	replicate16x	RW	0=replicate2x; 1=replicate16x
4	emitEnable	RW	0=emit Disabled; 1=emit Enabled
3	dacClkDiv	RW	0=Not Supported; 1=DAC outputs F_{SAMP}/8 (normal) (this bit always set)
2	dacDelay	RW	0 = Normal
1	dacRz	RW	0 = Normal
0	dacRf	RW	0 = Normal

Following START and emitEnable==1; the DACWorker will not begin emission until 128 4B words (256 samples) are received at the WSI-S port.

6.3 Using the DAC worker

After it is started, the DAC worker actually starts sending samples to the DAC upon receiving the first WSI message (actually 256 samples are available). After than it watches for an underrun condition where there is no incoming data to put on the isochronous output. By looking at the underrun indication (the first underrun message property), it is easy to determine how much data passed before underrun.