OpenCPI Reference Platform 2 COTS Components Specification

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Revision	Date	By	Notes
0.01	2009-11-16	ssiegel	Adopted from original
0.02	2009-12-09	ssiegel	ISE 11.4
0.03	2009-12-13	ssiegel	Included BIOS revision
0.04	2009-12-31	ssiegel	Red Hat Linux version clarified
0.05	2010-01-24	ssiegel	Checked Prices on www.newegg.com
0.06	2010-03-40	ssiegel	Processor and GPU refresh
0.07	2010-08-17	ssiegel	Updated and refresh

0.08	2010-11-02	mpepe	Added notes on assembly and setup
0.09	2010-11-18	mpepe	Added notes about FPGA setup.
0.10	2010-11-23	mpepe	Added notes about software dependencies.

Introduction

This document specifies the COTS components used for the OpenCPI FPGA Reference Platform 2 (ORP2). The parts and vendors specified herein have been selected for their ubiquity and low-cost. For most of the items listed, component substitutions may be made; however the burden of testing is then upon the user. Pricing is non-binding, quantity-one, guidance only. In addition to the parts list this document also provides some guidance on the assembly and configuration of the ORP2.

Components

It is possible to use one computer as both a development machine and a target. The ORP2 system contains both the development software required to design and implement an application and a mix of heterogeneous hardware on which to run the application.

Hardware

Table 1 below lists components central to the performance of the system.

Item	Quantity	Manufacturer	Part Number	Cost (estimate)	Description
1	1	www.evga.com	132-BL-E578-A1	$300	X85 Motherboard
2	1	www.intel.com	Corei7-980X	$1000	Gulftown 3.33 GHz 32nm Processor
3	1	www.corsair.com	DDR3 XMS3 12GB	$310	6x2GB (12GB) DDR3 1600 Memory
4	1	www.evga.com	012-P3-1470-AR	$330	NVIDIA GeForce GTX480 (Fermi) GPU
5	1	www.enermax.com	EMD625AWT	$160	625W MODU82+ Power Supply Unit
6	1	www.westerndigital.com	WD3000HLFS	$190	300GB 10K SATA Disk Drive
7	1	www.antec.com	P183	$120	ATX Mid Tower Computer Case
8	1	www.xilinx.com	EK-V6-ML605-G	$2000	Xilinx ML605 Virtex-6 Dev kit (includes software)

Notes:
1. Cost estimated, quantity one, as observed online Q3-2010.

2. The Xilinx ML605 includes a V6 LX240T device-locked copy of ISE Design Suite - Logic Edition.

All components in table 1, except for the Xilinx ML605, are available from computer component retails such as www.newegg.com. The rationale for the selection of line items 1 through 7 is to satisfy the requirement of identifying a high-performance and stable "X58-base Corei7 PC with 12GB RAM, strong GPU, and reliable 625W power supply". Deviating from these specific selections should not significantly alter system behavior. For example, replacing the GTX480 GPU (top of the line GPU in Q3-2010) with a different GPU should not change the behavior of an OpenCPI application not employing the GPU.

The Xilinx ML605 development kit is available from www.avnet.com and www.nuhorizons.com. Not included in the table above are components which may vary base on the user's specific requirements. These include, but may not be limited to, the CPU heat sink assembly, CD/DVD optical drive, keyboard, mouse, monitor, and peripheral hardware needed to complete the system.

An open-frame computer case may be used as an alternative to the enclosed case specified in line item 7 when frequent access to board hardware is desired; or where there may be mechanical interference from other PCIe add-in cards with taller profile. For example, PCIe cards with top-mounted FMC/VITA 57 connectors, such as the Xilinx ML605, will protrude in the vertical dimension such that the case side panel may not be fitted. One such open-frame case alternative offering is the "HSPC Tope DeckTech Stations (standard size)" from www.highspeeedpc.com at a cost of about $90.

Software

The ORP2 runs 64-bit Red Hat Enterprise Linux Desktop Workstation version 5.5 with automatic updates. The back-end FPGA development for the Xilinx FPGA requires ISE-LOGIC 12.3 or greater. A device-locked version of the ISE software is included with the ML605 development kit.

Item	Quantity	Manufacturer	Part Number	Cost (estimate)	Description
1	1	www.redhat.com	RHEL5-WS-64b	$179.00	Red Hat Enterprise Linux 5.5 64-bit Workstation
2	1	www.xilinx.com	EF-ISE-LOG-NL	Included in the price of the ML5605 development kit	Xilinx ISE Design Suite - Logic edition

Notes:

1. A V6-LX240T device-locked version of the Xilinx ISE Design Suite - Logic Edition is included with the purchase of the ML605.
2. When installing RHEL5 do not install the XEN virtualization software.
3. Recommend connecting RHEL5 to Red Hat Update, as our OpenCPI development systems receive OS updates in this manner.

4. The RHEL5 WS 64b is an annual subscription
5. The EVGA X58 Motherboard BIOS is version E758_74.

Optional

Depending on the intended use of the ORP2 the following optional components may be purchased and used with OpenCPI.

Hardware

Item	Quantity	Manufacturer	Part Number	Cost (estimate)	Description
1	1	www.u-blox.com	EVK-6T-0	$349.00	Precision timing evaluation kit (GPS)
2	1	www.4dsp.com	FMC150	$1995.00	Dual 250 MSPS @ 14-bit A/D and dual 16-bit 800 MSPS D/A FMC board
3	1	www.logitech.com	961419-0404	$79.99	Logitech Pro 5000 USB Webcam

Appendix I

Complete ORP2 BOM

Below is a bill of materials (BOM) for all of the hardware and software that was purchased to construct an instance of a ORP2 system. The hardware and software listed below was purchased and assembled in mid-October 2010.

Part Number	Unit Cost	Website	Description
N82E16813188039	$259.99	www.newegg.com	EVGA E758-A1 3-Way SLI (x16/x16/x8) LGA 1366 Intel X58 ATX Intel Motherboard
N82E16819115223	$999.99	www.newegg.com	Intel Core i7-980X Extreme Edition Gulftown 3.33GHz LGA 1366 130W Six-Core Desktop Processor BX80613I7980X
N82E16820145235	$259.99	www.newegg.com	CORSAIR XMS3 12GB (6 x 2GB) 240-Pin DDR3 SDRAM DDR3 1600 (PC3 12800) Desktop Memory Model
N82E16814130551	$489.99	www.newegg.com	EVGA 015-P3-1482-AR GeForce GTX 480 (Fermi) SuperClocked FTW 1536MB 384-bit GDDR5 PCI Express 2.0 x16 HDCP Ready SLI Support ...
N82E16817194067	$149.99	www.newegg.com	ENERMAX MODU82+ EMD625AWT_II 625W ATX12V v2.3 / EPS12V CrossFire Certified 80 PLUS BRONZE Certified Modular Active PFC Power
N82E16822136322	$179.99	www.newegg.com	Western Digital VelociRaptor WD3000HLFS 300GB 10000 RPM SATA 3.0Gb/s 3.5" Internal Hard Drive -Bare Drive
N82E16811129061	$154.99	www.newegg.com	Antec P183 Black Aluminum / Steel / Plastic ATX Mid Tower Computer Case
EK-V6-ML605-G	$1995.00	www.avnet.com	VIRTEX 6 FPGA ML605 Evaluation Kit and the Xilinx ISE Logic Edition Node Locked software
N82E16824236047	$289.99	www.newegg.com	ASUS VW266H Black 25.5" 2ms(GTG) HDMI Widescreen LCD Monitor
N82E16826193041	$6.99	www.newegg.com	Rosewill RK-100 Black USB Standard Keyboard
N82E16826193042	$5.99	www.newegg.com	Rosewill RM-C2U 3 Buttons 1x Wheel USB Optical Mouse
N82E16826992004	$4.99	www.newegg.com	DOLICA Midnight Edge Series ME-100 Mouse Pad
RHEL5-WS-64B	$179.00	www.redhat.com	Red Hat Enterprise Linux 5 64-bit workstation
961419-0404	$79.99	www.newegg.com	Logitech Pro 5000 USB Webcam

EVK-6T-0	$349.00	www.u-blox.com	Precision timing evaluation kit (GPS)
NP-05	$245.00	www.synaccess-net.com	5 Outlet Remote Power Management Strip
N82E16827135204	$18.99	www.newegg.com	ASUS Black 24X DVD+RW 32X CD-RW 2MB Cache SATA 24X DVD Burner

Appendix II

Notes on Hardware Assembly

The instructions below are non-normative. The instructions are based on one person's experience in assembling an ORP2. To avoid damage to the sensitive electronic components it is strongly recommended that one take precautions to eliminate the possibility of ESD.

1. Start with the motherboard assembly.
    a. CPU die installation
        i. Remove the fake plastic die from the CPU site on the motherboard.
        ii. Carefully, install the CPU die in the die site. Take note of the keying on the die and be sure to align it with the keying on the die site.
        iii. Secure the CPU die in the die site with the die holder. The die holder lever requires some pressure to latch.
    b. Heat sink installation
        i. Undo the for screws on the heat sinks legs to release the heat sink base.
        ii. Peal the cover off the stickers on the heat sink base and use the stickers to secure the heat sink base to the backside of the motherboard. Take care to align the four pilot holes on the motherboard with the screw holes on the heat sink base.
        iii. Apply the thermal compound to the top of the CPU. The thermal compound is pre-measured so use all of it.
        iv. Make sure to keep the power cord attached to the heat sink assembly accessible when you mate the fan assembly to the motherboard.
        v. Remove the sticker from the heat sink fan assembly and be careful not to get fingerprints on the part of the assembly that touches the top of the CPU.
        vi. Attach the heat sink fan assembly to the motherboard using the four screws removed earlier. Take care to align the screws with the holes in the heat sink base as each of the four screws must attach to the heat sink base that is on the backside of the motherboard.
        vii. Do not over-tighten the heat sink screws.
        viii. Attach the heat sink fan assembly power cord to the CPU fan site on the motherboard.
    c. Memory installation
        i. The 12GB of RAM come in six 2GB DIMMS.
        ii. Install one DIMM in each of the six DIMM slots on the motherboard. Take care to make sure that each DIMM is seated properly.
    d. Motherboard installation.
        i. The Antec P183 computer case comes with a large number of screws. Look for the plastic package with the word "motherboard" or the

letter "MB". There should be at least nine screws in the bag.
   ii. Remove the side panel from the Antec P183 case that is secured by two black screws.
   iii. Removed the stock peripheral faceplate. Pull the faceplate from the inside of the box to remove it.
   iv. Install the peripheral faceplate that comes with the EVGA X58 motherboard. Push the faceplate from the inside of the case until it snaps into place.
   v. Place the mother board into the case.
      1. Take care to align its peripheral interfaces with the peripheral faceplate.
      2. Take care to keep the wires for the fans free.
   vi. Use the nine motherboard screws to secure the board to the case.
2. Power supply installation
   a. Remove the second side panel from the Antec P183 case. This second side panel covers a cavity that is intended to be used to route power to the motherboard and the peripherals.
   b. Install the power supply unit and secure it to the back of the case with the provided screws.
   c. Route the two power cables from the power supply into the wire cavity side of the case.
      i. Plug the motherboard power cable into the mother board power site.
      ii. Plug the CPU power cable into the CPU power site on the motherboard.
   d. Route the power cords for the case fans into the backside of the CPU case. Plug the two fan connectors together in a daisy chain.
   e. Connect power cord to the power supply that has both a SATA and a 4-pin power connector. Route the cord to the back of the case.
      i. The SATA power connector will be for the CD/DVD drive.
      ii. Attach the 4-pin connector to the daisy chained fan power connectors.
   f. Connect a second SATA power connector to the power supply. This cable is for hard-drive. Leave this power connector in the base of the case.
   g. Connect a power cable that has a 4-pin connector to the power supply. This cable is for the Xilinx FPGA board. Leave this power connector in the base of the case.
   h. Connect the two 12 pin power cords to the power supply. These two cords are for the GPU. Leave them in the base of the case.
3. The Antec P183 case has some build-in wires for the SATA controller, USB ports, audio ports, and status lights. Route the bundle of built-in wires into the wire cavity side of the case. From the wire cavity you can reach the motherboard by passing the wires through the gap that exists between the motherboard and the peripheral bays.
   a. Connect the status light wires to the motherboard.
   b. Connect the USB cable to the site on the motherboard.
   c. Connect the SATA cable to the site on the motherboard.
   d. In our setup we did not attach the audio cable. You can if you want.

4. Install the CD/DVD drive
    a. Open the door on the front of the Antec P183 case.
    b. Remove the top-most bay cover. Push the levers on the side of the bay cover in to pop the bay cover off.
    c. Rotate the metal grill in a circle to weaken the it and then snap the metal grill off of the case.
    d. Attach one guide rail to each side of the drive. The metal tab on the guide rails should be facing toward the front of the drive.
    e. Slide the drive from the front of the case into the drive bay until it snaps into place.
    f. From inside of the case
        i. Attach the SATA power connector to the drive
        ii. Attach a SATA cable to the drive and to a SATA site on the motherboard.
5. Install the hard drive
    a. Remove t he bottom peripheral bay from the Antec P183 case.
    b. Using the four screws that have built-in washers provided with the Antec P183 case attach the drive to the peripheral bay. In our configuration the drive is perpendicular to the bottom of the bay.
    c. Slide the bay back into the case and secure it.
    d. From inside of the case
        i. Attach the SATA power connector to the drive
        ii. Attach a SATA cable to the drive and to a SATA site on the motherboard.
6. Install the Xilinx FPGA board.
    a. Set the S2 DIP switches for "Slave SelectMAP Platform Flash XL" mode and jumper J42 to PCIe present x4. See the appendix for more information on the ML605 setup.
    b. Remove the "legs" from the Xilinx FPGA board.
    c. Route the 4-pin power cable through hole in the center of the case and attach the 4-pin power connector to 4-pin power site that is at the center of the Xilinx FPGA board. The 6-pin power connector next to the USB site on the Xilinx FPGA board is not used when the Xilinx FPGA board is installed in a PCIe slot.
    d. Install the Xilinx FPGA board in the bottom 8x PCIe slot.
    e. Connect the USB cable to the USB site on the side of the Xilinx FPGA board and route the USB cable through the hole in the back of the computer case. At this time do not plug the USB cable into a USB slot.
7. Install the GPU
    a. Install the GPU in the top-most 16x PCIe slot. You may need to bend the metal tabs on the center peripheral bay to fit the GPU.
    b. Use both screws to attach the GPU to the case.
    c. Attach both power cords to the GPU. Route the cables through the hole in the center of the case.

8. Attach both side panels to the Antec P183 computer case.

Appendix III

Notes on Software Setup

BIOS

Our system is using EVGA BIOS version E758_74. Our EVGA X58 motherboard came with an older BIOS that did not recognize our hard drive. We used the directions on the EVGA website to upgrade the BIOS.

In the BIOS we also enable AHCI for the SATA controllers.

OS

Our installation of RHEL5 uses a single partition on the hard drive. We do not install the XEN virtualization software. Our ORP2 systems receive updates from the Red Hat Update Network.

Below are the configuration options that we used when installing RHEL5.

- Selected both "Office" and "Multimedia".
- Applications
  - Added "Engineering and Scientific"
- Development
  - Added "Development Libraries"
  - Added "Development Tools"
  - Added "X Software Development."
- Servers
  - Added "Web Server"
  - Added "Server Configuration Tools"
  - Added "Windows File Server"
- Base System
  - Added "System Tools"
- Disabled the firewall (we are on an internal network)
- Disabled SE Linux
- Enabled kernel dump

ISE

The install disk that comes with the Xilinx FPGA development kit may contain an old version of the ISE software. If this the case the latest ISE software can be downloaded from the Xilinx website.

GPU

Our ORP2 currently contains an NVIDIA GPU. The OpenCPI software for the GPU uses

OpenCL (http://www.khronos.org/opencl/) so we install the NVIDIA GPU driver required by the NVIDIA OpenCL package.

OpenCPI Software Dependencies

The installation of RHEL5 outlined above does not contain all of the packages that are required to build OpenCPI. Below is a list of packages and how to acquire them. All of the required package must be installed to build OpenCPI.

Please note the "Workstation Channel" for the RHEL5 subscription must be enabled for `yum` to have access to the workstation repositories. You can enable the "Workstation Channel" from the subscription management section of the RHEL5 website.

Required Packages

1. zlib - http://www.zlib.net/
   ```
   # yum install zlib-devel.x86_64
   ```
2. GNU g++ http://gcc.gnu.org/
   ```
   # yum install gcc-c++.x86_64
   ```
3. Python http://www.python.org/
   ```
   # yum install python.x86_64 python-devel.x86_64
   ```
4. Git - http://git-scm.com/download
   a. Download the source code.
   b. Unzip the source code.
      i. `$ bunzip2 git-1.7.3.2.tar.bz2`
      ii. `$ tar -xvf git-1.7.3.2.tar`
   c. Build Git and then install it.
      i. `$ cd git-1.7.3.2`
      ii. `$ ./configure`
      iii. `$ make`
      iv. `$ sudo make install`
5. Omni ORB http://omniorb.sourceforge.net/
   a. Download the source code.
   b. Unzip the source code.
      ```
      $ tar -zxvf omniORB-4.1.4.tar.gz
      ```
   c. Build Omni ORB and then install it.
      i. `$ cd omniORB-4.1.4.tar.gz`
      ii. `$ mkdir build`
      iii. `$ cd build`
      iv. `$ ../configure --prefix=/opt/opencpi/linux-x86_64/prerequisites/omniorb --without-openssl`
      v. `$ make`
      vi. `$ sudo mkdir -p /opt/opencpi/linux-x86_64/prerequisites/omniorb`
      vii. `$ sudo make install`

Optional Packages

These package are used by some of the examples.

- None at this time.

Appendix VI

Notes on FPGA Setup

ISE

We install ISE Design Suite - Logic Edition in its default location of /opt/Xilinx. When installing ISE make sure to check the "Install Cable Drivers" check box. This box is not checked by default.

JTAG USB Drivers

Please follow the directions in the Xilinx UG344 *USB Cable Installation Guide* to install the drivers required to support USB connection to the FPGA board.
This is a link to the UG344 document. You may need to repeat the `sudo chmod 666 /dev/windrvr6` step every time the ORP2 system is rebooted.

After performing the steps in UG344 download and install fxload.

1. Download the fxload source code from Source Forge.
2. Unpack the tar/gzip file.
3. If you do not have the Linux source files needed to build kernel modules installed on your RHEl5 system then:
   a. Open the file fxload file named `ezusb.c`
   b. Replace `#include <linux/usb/ch9.h>` with `#include </usr/include/linux/usb_ch9.h>`
4. Compile the files
   `$ make`
5. Install the files
   `$ sudo make install`

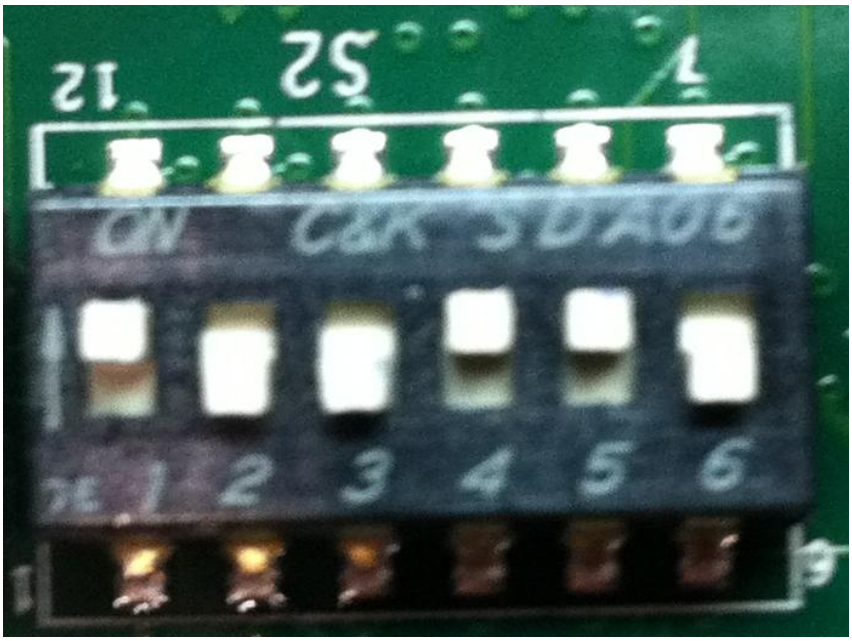
Make the windrvr6 device accesible by non-root users. This step is needed to allow Xilinx tools like iMPACT to connect to the FPGA board when run by non-root users.

```
# sudo chmod 666 /dev/windrvr6
```

Initial ML605 Setup

In the ORP2 system the ML605 is hosted in an 8x PCIe slot. The ML605 is connected to the systems PSU using the 4-pin 12V ATX (old-style hard drive) power connector. Before inserting the board into the system the S2 DIP switches must be configured for "Slave SelectMAP Platform Flash XL" and jumper J42 must be set to PCIe 4x present.

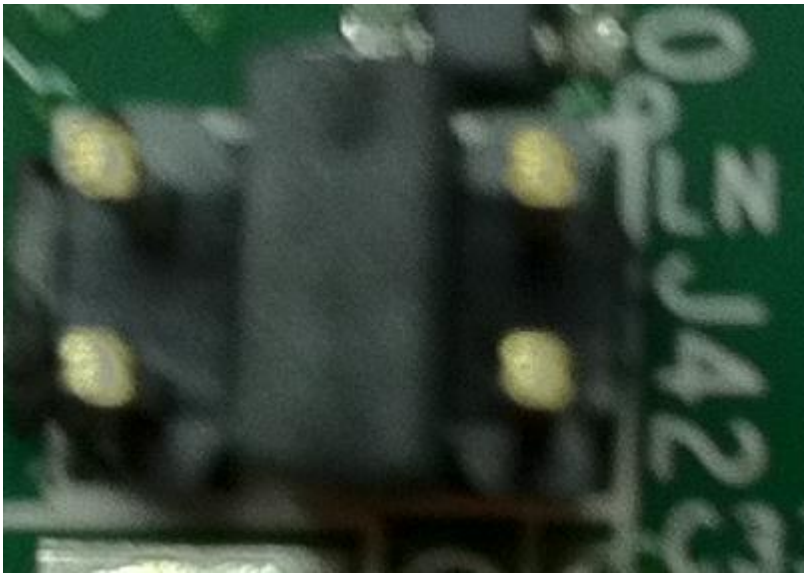
In version 1.4 (October 12, 2010) version of the Xilinx UG534 *ML605 Hardware User Guide* table 1-27 on page 57 contains the S2 DIP switch settings. Below is a picture of the S2 DIP switch with the expected settings.



The table below contains the expected S2 DIP switch settings.

S2.1	S2.2	S2.3	S2.4	S.5	S.6
on	off	off	on	on	don't care

In version 1.4 (October 12, 2010) version of the Xilinx UG534 *ML605 Hardware User Guide* figure 1-12 on page 32 contains the J42 jumper settings. Move the J42 jumper to PCIe present 4x. The picture below shows the proper setting for the jumper.



First OpenCPI Bitstream Load

OpenCPI allows you to load a bitstream while the Linux host is running. However, to achieve

this capabiltity, there is a one-time requirement of loading an OpenCPI bitstream into flash so that the BIOS sees and OpenCPI PCIe endpoint when Linux boots. Below are the one-time steps needed to load an OpenCPI bistream from flash into an ML605 with the Xilinx tools.

Once the S2 DIP switches and J42 jumper are set and the ML605 board is installed in the ORP2 system attach the USB cable (B-side) to the JTAG port on the back panel of the ML605 and the A-side to a free USB port on the ORP2.

Power on the ORP2 system. Make sure the power switch on the side of the ML605 board is in the "on" position. Build or get a copy of a known good ML605 OpenCPI bitstream. The first bitstream load must be done through flash. Therefore, the .bit bitstream file must be converted to a prom file using the Xilinx tool named `promgen`.

Before using the Xilinx tools the Xilinx environment script must be run. Use this command to run the Xilinx environment script.

```
$ . /opt/Xilinx/12.3/ISE_DS/settings64.sh
```

This is an example of the `promgen` command line needed to convert a ML605 .bit file into a prom file. In this example, `promgen` will output three files: `fpgaTop.cfi`, `fpgaTop.mcs`, and `fpgaTop.prm`.

```
$ promgen -w -p mcs -c ff -x xcf128x -u 00000000 ./fpgaTop.bit -data-width 16
# Where fpgaTop.bit is the name of the .bit file being converted
```

After generating the prom file launch the Xilinx iMPACT GUI program.

```
$ impact
```

When iMPACT starts:

1. Click "No" to the "Automatically create and save a project" question.
2. Click "Cancel" when prompted to "load" or "create" a new project.
3. In the upper left window named "iMPACT Flows" double-click on "Boundary Scan".
4. Right-click in the center window with the text "Right click to Add Device or Initialize JTAG chain".
5. Select "Initialize chain" from the menu. If this step succeeds a diagram of the detected devices will appear on the screen.
6. Click "No' when prompted to "Auto Assign Configuration Files".
7. Click "Cancel" when prompted to select "Device Programming Properties'.
8. Right-click on the icon of the xc6vlx240t and select "Add SPI/BPI Flash".
9. Navigate to and select the .mcs file produced by `promgen`. iMPACT only asks for the location of the .mcs file but it will want the .prm and .cfi files produced by `promgen` to be in the same directory as the .mcs file.
10. Select the "BPI PROM" and click "Ok".

11. Right-click on the "FLASH" icon attached to the xc6vlx240t and select "Program". The PROM programming may take several minutes to complete. When the flash is done being programmed the words "Program Succeeded" will appear on the screen.
12. Once the PROM is done being programmed exit iMPACT (do not save the project) and power off the ORP2 system. The system must be power off and not just rebooted. For completeness we recommend powering off the power supply to make sure that the motherboard is not providing any power at all to the FPGA board.
13. Power the ORP2 system on. During the power on the bitstream will be loaded from flash into the FPGA. To the right of the SFDP housing is a row of eight LEDs. If the PCIe training is successful one of the LEDs will illuminate.
14. Once the system is powered up you can use the program `ocfrp_check` as a sanity test to see if the OpenCPI bitstream actually got loaded in the FPGA.

```
$ sudo ./bin/ocfrp_check

# If successful, the output will look something like:
Found OpenCPI FPGA reference platform "0000:03:00.0" with bitstream
birthday: Sat Oct 30 16:11:29 2010
```

15. After following the one-time (first-time) instructions to load an OpenCPI bitstream subsequent OpenCPI bitstreams can be loaded into the ML605 FPGA using the `loadBitStreamML605` script. The Xilinx iMPACT tool will fail to run if `/dev/windrver6` has the wrong permissions. Use `sudo chmod 666 /dev/windrvr6` to make the file accessible by non-root users.

```
$ cd scripts
$ ./loadBitStreamML605 <Path to bitstream .bit file> <PCIe address> <JTAG
USB>
# Example
$ ./loadBitStreamML605 ./fpgaTop.bit 0000:03:00.0 usb21
```

Reserve Memory for User-mode DMA

The OpenCPI bitstream can perform user-mode DMA without a kernel-mode drives. Use the following steps to set aside memory for OpenCPI user-mode DMA.

1. At this time the OpenCPI gateway requires that the user-mode DMA memory pool be in a 32-bit memory range. The first step is to find a "usable" contiguous memory range. We do this by `grep`'ing the `/var/log/messages` file for the unused memory regions. In the example below we find three usable memory ranges. The first range is small and the third range is outside of the 32-bit address range. Fortunately the second address space is in the 32-bit address range and it is large enough for us to reserve several hundred megabytes of memory.

```
$ sudo grep BIOS /var/log/messages | grep usable

 $ sudo grep BIOS /var/log/messages  | grep usable
Nov  2 14:17:14 ocrp1-mfs kernel:  BIOS-e820: 0000000000010000 -
 000000000009e000 (usable)
Nov  2 14:17:14 ocrp1-mfs kernel:  BIOS-e820: 0000000000100000 -
```

```
 000000009f790000 (usable)
Nov  2 14:17:14 ocrp1-mfs kernel:  BIOS-e820: 0000000100000000 -
 0000000360000000 (usable)
```

2. Modify grub.conf to reserve memory for user-mode DMA. In this example, we are going to reserve 512MB of memory starting 512MB below the top of the second unused memory range show in the example above.

```
# Add the memmap variable to the bootline in grub.conf. The memmap
# variable includes the size of the reserved memory region and
# the starting address of the memory region. Continuing with
# our example we are reserving 512MB at 0x7F790000.
# Our bootline looks like:

$ sudo vi /boot/grub/grub.conf
kernel /vmlinuz-2.6.18-164.11.1.el5 ro root=/dev/vg00/lv01
memmap=512M$0x7f790000 panic=5 crashkernel=128M@16M initrd /initrd-2.6.18-
164.11.1.el5.img
```

3. Now reboot the system.
4. The user-mode DMA memory pool is provided to the OpenCPI software by way of an environment variable name `OCPI_DMA_MEMORY`.

```
$ export OCPI_DMA_MEMORY=<size in Megabytes>M$<Starting address in hex>
# For our example we would use:
$ export OCPI_DMA_MEMORY="512M\$0x7F790000"
```