3C7 Digital Systems Design

Lab Session D

Aim:

The purpose of this session is familiarise yourself with the Implementation flow in the Xilinx Vivado environment to allow you to begin to target designs on the BASYS 3 development board (Part 1). You will target some existing designs to the BASYS 3 development board (Part 2).

Learning Outcomes:

On completing this lab session you will be able to:

- Use the tools provided to synthesize and implement your design, and generate a BIT file for your design
- Program the BASYS 3 board
- Use the Hardware Manager within the Xilinx Vivado environment.

PART 1 – Vivado Tutorial

In the LabD folder you will find a pdf document called LabD_tutorial.pdf. This is an implementation tutorial for the Vivado environment. You will implement a Pulse Width Modulator (PWM) design. Note that I have added some comments into the pdf where I found the tutorial unclear or where things did not happen quite as described. Wherever you see this symbol, click on the note to see the message.

Figure 1: Note symbol in the pdf

Note any tasks as you go along, e.g. where you are asked to save a copy of a waveform and include this in your write-up.

Instructions:

1. Make a new folder called LabD for this exercise. (remember to use a local location like C:/temp/studentID/LabD – particularly for students using remote access)

2. This tutorial is targeting the ZedBoard device. We will eventually be using a BASYS 3 device but follow the instructions as per the tutorial for now.

3. The required design files are supplied in tutorial code.zip. Read about what is involved in synthesizing the design.

4. When you have your completed utilization report (Fig 1.25), pause and explore the contents of the report. Does it make sense? What can you observe form it? Record your observations for your lab report.

5. **Note** that a few stages in this tutorial do not need to be completed. These are clearly marked. You simply need to read the steps without undertaking them.

PART 2 – Implement on BASYS 3 board

The implementation tutorial provided in the file *LabD_tutorial.pdf* is aimed at a different board (Zedboard) and hence won't download to our BASYS 3 board. You will be taken through the flow in detail with an existing design and will then try to target another design onto the board. You need to complete Part 1 before attempting this section. You will use the supplied USB cable to download the design.

Instructions:

LEDs – BASYS 3

The BASYS 3 board has sixteen individual surface-mount LEDs located above the slide switches as shown below. The LEDs are labelled LD15 through LD0. LD15 is the left-most LED, LD0 the right-most LED.

LEDs on the BASYS 3 board

These can function as an indicator within an embedded application. The module bargraph.v utilises 8 of the available LEDs and provides a graph display useful for peak amplitude measurements in audio and communications signal processing applications. This simple module makes the LEDs output a pattern typical for a volume indicator.

1. Start the Vivado tool, closing any project left open from your last exercise.

2. Copy the directories in the LabD folder into a new folder on your machine. You will need the files contained in "bargraphtest code basys.zip"

3. In Vivado, open a new project. Select RTL Project and make sure the "Do not specify sources at this time" box is unchecked. Click Add Files and add *bargaphtest.v*, *bargraph.v* and *clock.v* to the project (some of these may be located in the Peripherals folder). Select both target language and simulator language to Verilog. Click Next.

4. In the Add Constraints window, click Add Files and add *bargraphtest.xdc* to the project. Click Next.

5. Select the board BASYS 3 under the Boards tab. Click Finish.

6. Ensure that USB is selected on jumper JP2 (beside the ON/OFF button). Turn the power ON – you should see a red light indicating that the board is on.

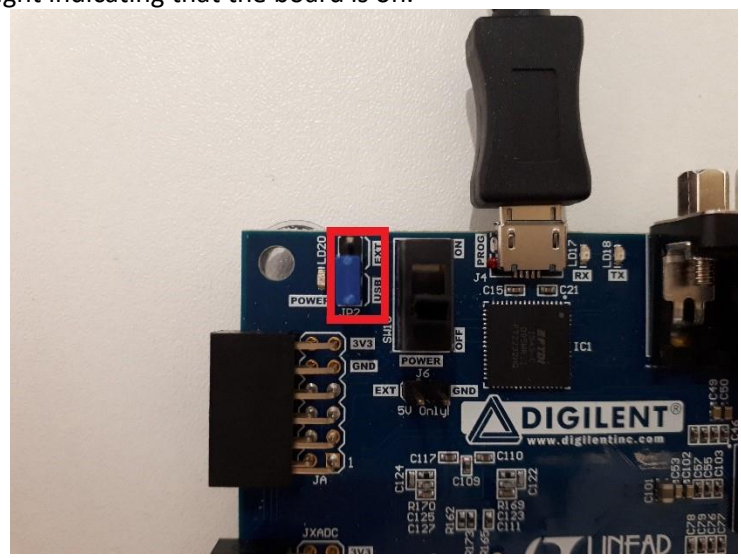
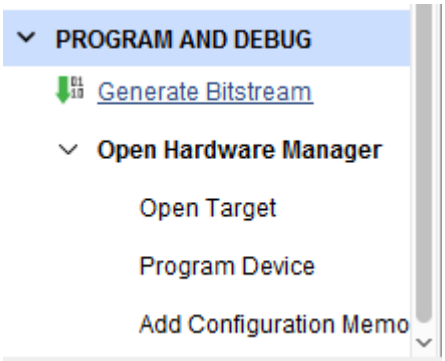
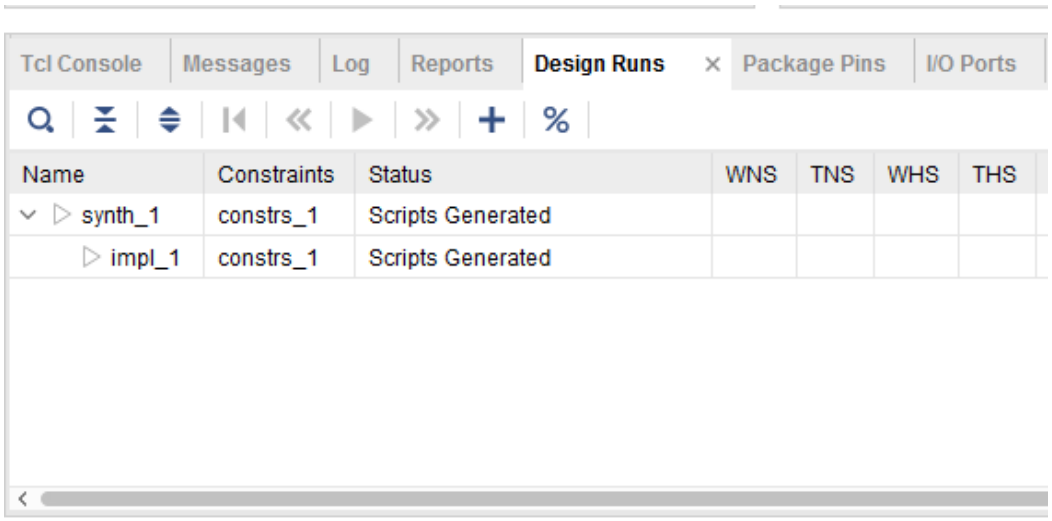


Figure 1: Jumper JP2 on the BASYS 3, with USB selected

7. Ensure the *bargraphtest.v* module is highlighted in the hierarchy window. Double click "Generate Bitstream" in the Flow Navigator window, under "PROGRAM AND DEBUG". This should launch two processes, Synthesis and Implementation. Click "Yes" and "OK" in any dialog boxes which pop up to run these processes with default settings. The progress of these runs can be tracked in the Design Runs window (Window -> Design Runs).

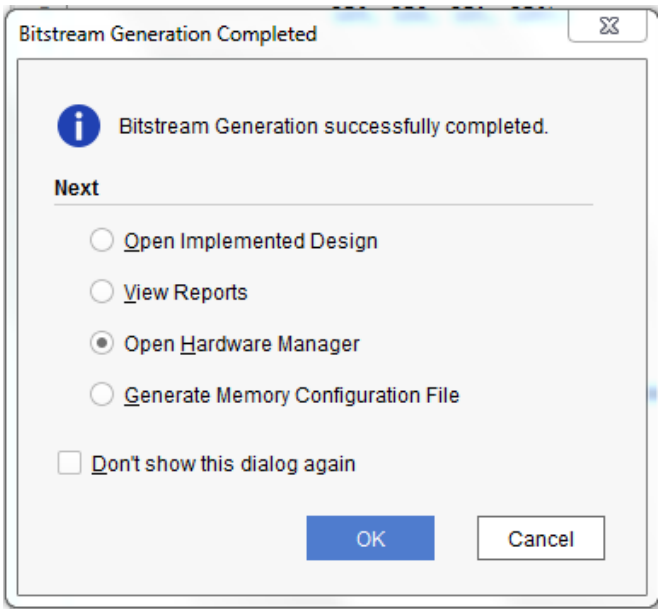


Generate Bitstream button



Design Runs window

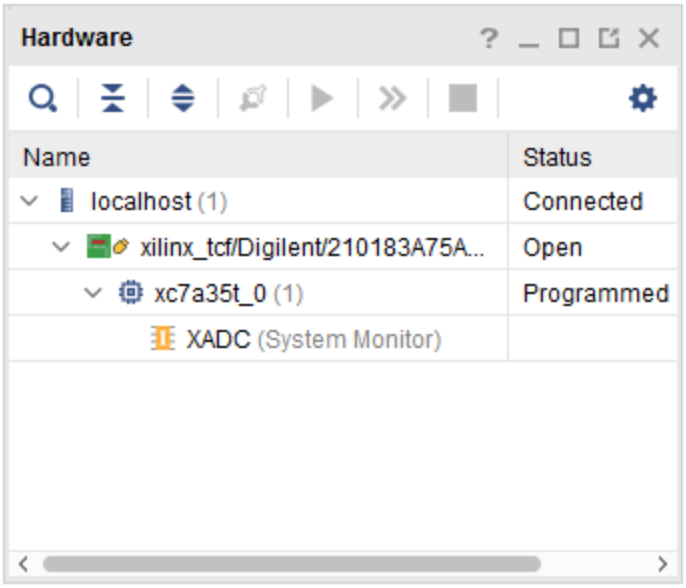
8. After the design has been successfully synthesised and implemented, the following dialog box shows. Select “Open Hardware Manager”.



Bitstream Generation Completed dialog box

9. Click “Open Target -> Auto Connect” to start the hw_server which scans for devices. Right-click on the Xilinx device which appears underneath localhost and click “Open Target” to show the connected FPGA.

10. Right-click the FPGA device and select Program Device. Direct programming to the FPGA takes a few seconds to less than a minute, depending on the speed of the PC’s USB port.



Hardware window

11. Have a look at your board – the LEDs should be flashing! Well done - You have downloaded your first design to the board. Can you estimate how quickly they are changing, and what is the sequence they are displaying?

12. Go back to your design and observe the synthesis report and implementation report. Observe the resource utilisation and record them for the report.

13. Set the binary equivalent of your board number as the input switches and capture a photo of the design working on your board. Include this in your report.

14. Open the source files (including .xdc) that you have added for this section; based on the contents covered in the lectures so far, describe (in a few lines) what you infer about the contents of each file.

Submission:

You must submit the following parts, contained in a single PDF, via Blackboard:

- Short write-up on what you did in the lab and your key takeaways.
- Observations and resource consumption details captured for Vivado's tutorial code.
- Observations and resource consumption details captured for Basys-3 implementation.
- Additional inclusions as described in parts of this lab sheet.

Name the file LabD_surnameinitial.pdf, e.g. LabD_shankers.pdf.

Deadline:

Group A (Tuesday labs): Tuesday 28th February 2023.
Group B (Friday labs): Friday 03rd March 2023.
All submissions are via blackboard. This report is worth 10% of your CA.

Plagiarism

Plagiarism is interpreted by the University as the act of presenting the work of others as one's own work, without acknowledgement. Plagiarism is considered as academically fraudulent, and an offence against University discipline. The University considers plagiarism to be a major offence, and subject to the disciplinary procedures of the University.
Visit http://tcd-ie.libguides.com/plagiarism

All students must complete the TCD Ready Steady Write plagiarism tutorial and sign a declaration when submitting course work, whether in hard or soft copy or via Blackboard, confirming that you understand what plagiarism is and have completed the tutorial. If you read the information on plagiarism, complete the tutorial and still have difficulty understanding what plagiarism is and how to avoid it, please seek advice from your College tutor, your Course Director, your supervisor, or from Student Learning Development.

e.g. having exactly the **same testvectors or module** as another person **is plagiarism**.

Plagiarism will result in loss of **ALL** marks for this assignment.