Laboratory #4: Multiplexer Design (Part 1)

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35219 Lab Group 5
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Pre-lab work:

1. In order to prepare for this lab, it is helpful to look over the Quartus software, and to review notes on Mux's and decoders.
2. Prepare a working 2:1 Multiplexer with a select input which corresponds to:
    a. S(0) → M = X
    b. S(1) → M = Y
3. Using multiple 2:1 Multiplexers, design a 5:1 Mux
4. Find truth tables for each Mux design

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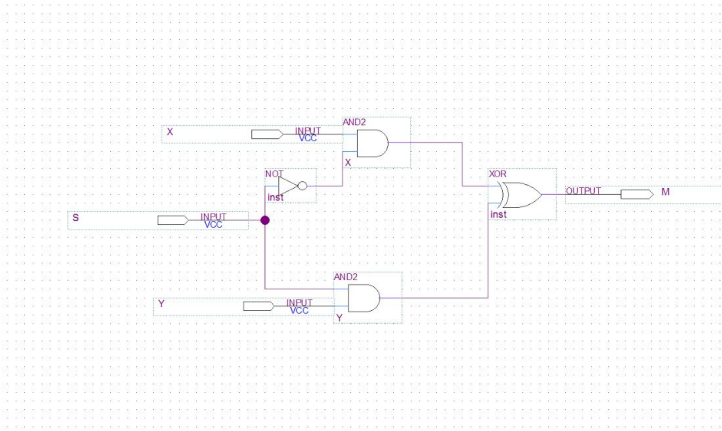
PreLab 4
4/23/16
Grade: 9/10

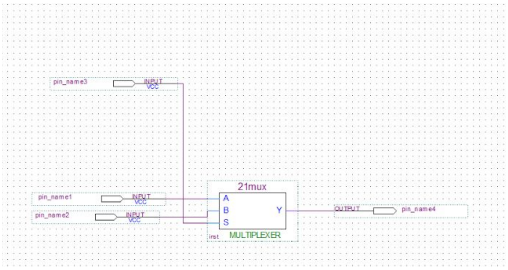
I began by reviewing the lesson on MUX and looking over the PDFs on Quartus software. I then started out by drawing the general schematic for a 2:1 MUX.

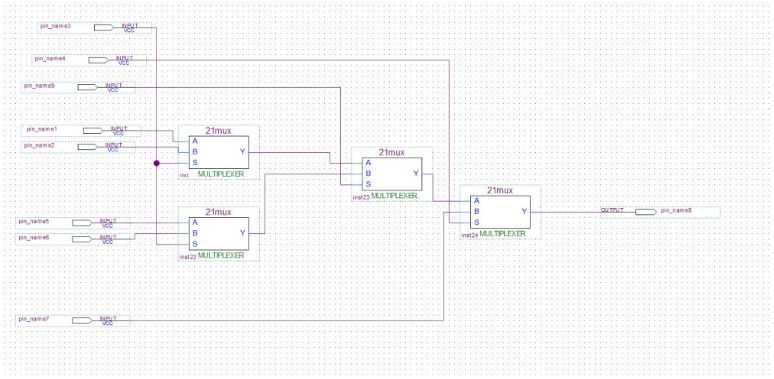


M = X(S)' or Y(S)

X	Y	S	M
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	1	1

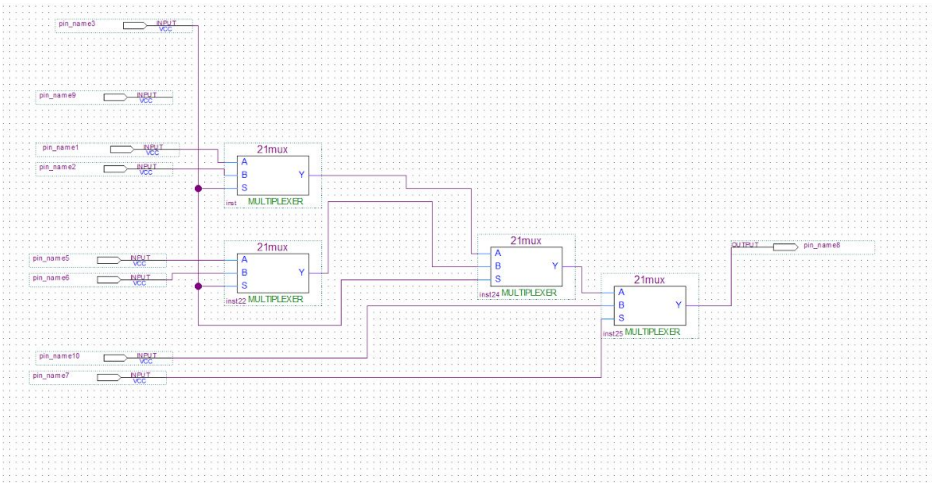
I found in the Quartus library a useful 2:1 mux function .
This Mux function should have the same functionality as the circuit above.





Designing the 5:1 MUX took some thought. Pushing the output values of the 2 first level MUX through a 2:1 mux, will give the “correct” output from the first level. Then taking the output value of the second level MUX, and pushing it through with the third input, will give us the final result out.

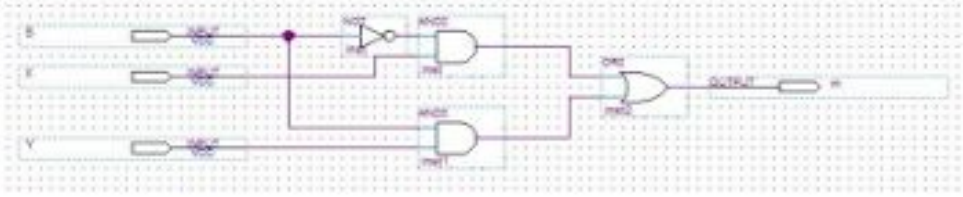
I created an 8:1 MUX by using the same method as the 5:1



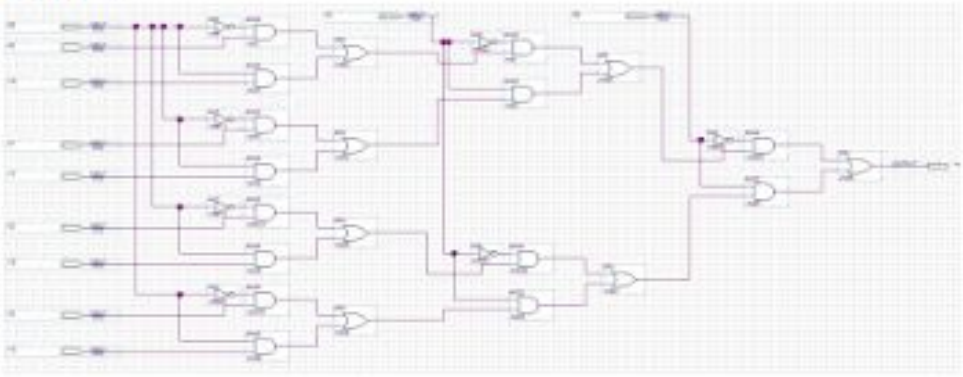
Simran Judge

Lab 4 Prelab

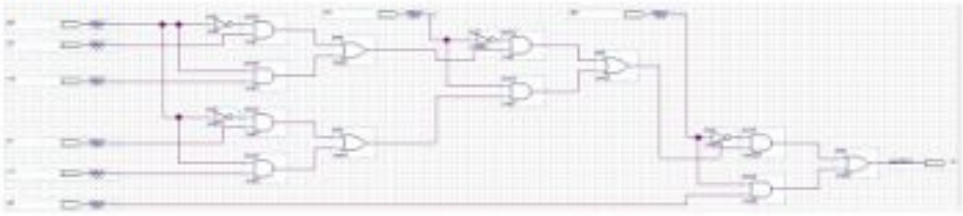
s	x	y	m
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1



8-to-1 MUX



5-to-1 MUX



I. Objectives

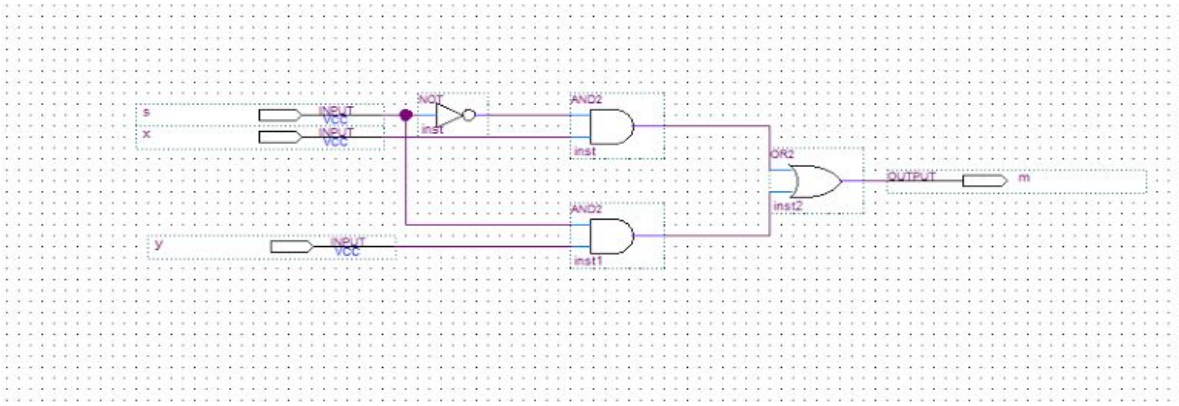
Our objective was to design the schematics for different multiplexers on Altera Quartus II. The main objective was to design a three-bit wide 5-to-1 multiplexer and to explore how multiplexers could be built hierarchically. The purpose of this laboratory is to learn how to connect simple input and output devices to an FPGA chip and implement a circuit that uses these devices. We used the switches SW17−0 on the Altera DE2-series board as inputs to the circuit. We used light emitting diodes (LEDs) and 7-segment displays as output devices.

II. Introduction

In this lab, we were responsible for creating a working 8 bit wide 2:1 multiplexer. Our challenge began with the implementation of a simple 2:1 multiplexer. Using Altera Quartus II Software, we designed the schematic for the 2:1 MUX, which matched the schematic in our prelabs. From this, we built an 8:1 MUX, and finally a 5:1 MUX. By using only 2:1 MUXs, we create a hierarchical structure of MUXs to combine into a large input or output multiplexer. We were able to implement this logic using Altera Quartus II. We were able to test our design using waveforms and an Altera FPGA.

III. Procedure

1. **2-to-1 MUX** Schematic



2. Once we came up with our working 2-to-1 mux, we wanted to make sure that all of our switches and output LED's were functioning as they should. We tested each light, and switch, and found that everything was as expected.
3. We then designed our own "symbol" from the 2:1 Mux we designed above and called it "selectorM"
4. From our new symbol, we could easily create an 8:1 hierarchically designed multiplexer

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Schematic
8:1 MUX

"selectorM" is
our 2-to-1 MUX

We need another selector input for each level of logic (i.e 3 selectors for 3 levels)

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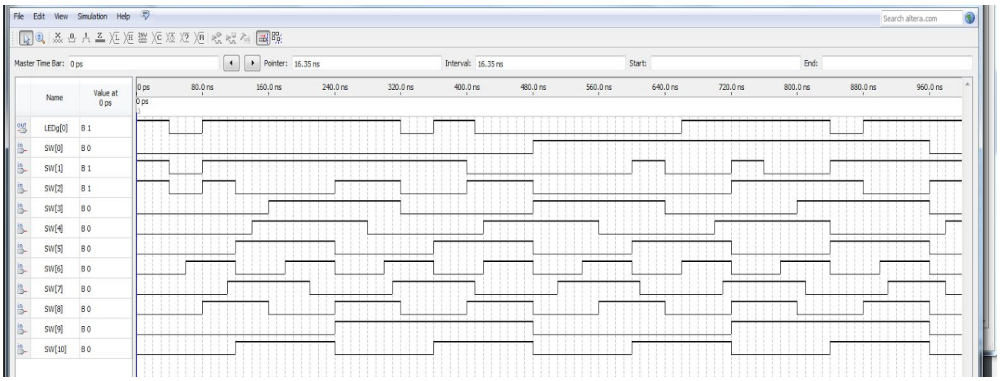
5. We had to test that our schematic functioned as expected, so we ran it through our simulator.

Simulation

8:1 MUX



To ensure that our logic and schematic were correct our group had to analyze the different values.

For a few inputs and check the corresponding outputs. For us, the easiest way was to see that everywhere where our selectors (SW[0], SW[9], and SW[10]) were0, since our LED should then correspond to whichever state SW[1] was in.

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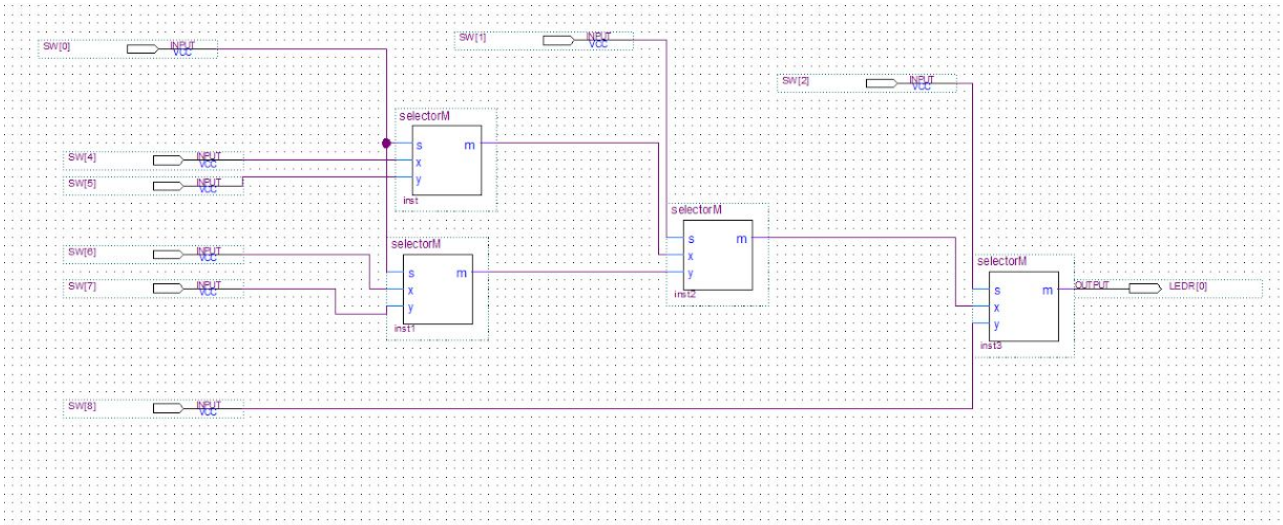
6. Next we used our working 2:1 Mux to build a **5:1 MUX**. Since there are an odd number of inputs, we will need to have an additional input line for the last 2:1 mux.

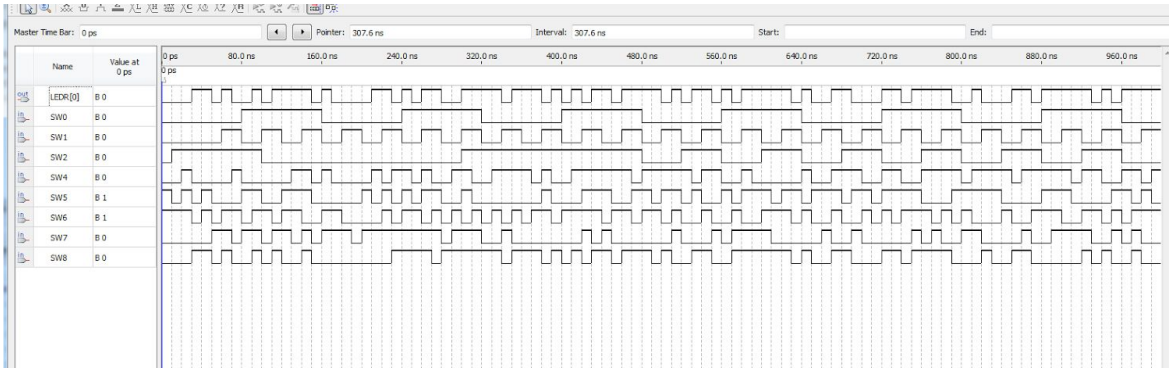
Schematic for 5:1 MUX



We found that using the first three switches (SW[0], SW[1], and SW[2]) as select lines made it easier to track the outputs. The 5:1 Mux uses a total of 4, 2:1 Multiplexers. The first 3

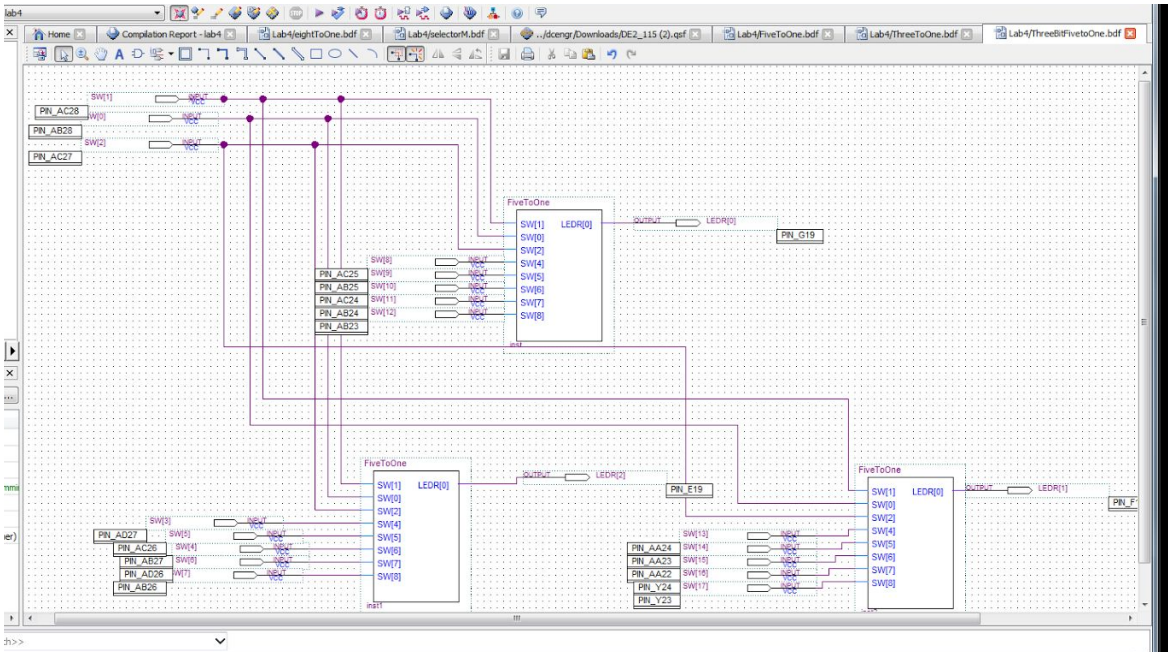
Multiplexers take in 4 inputs, which outputs the “choice” from those inputs. Then the last 2:1 MUX decides the final “choice” between the 5th input and result from the first 4 inputs result. We use an additional 2:1 mux to choose from the final output. This results in a complete design of a 5:1 Mux.

Simulation of 5:1 Mux

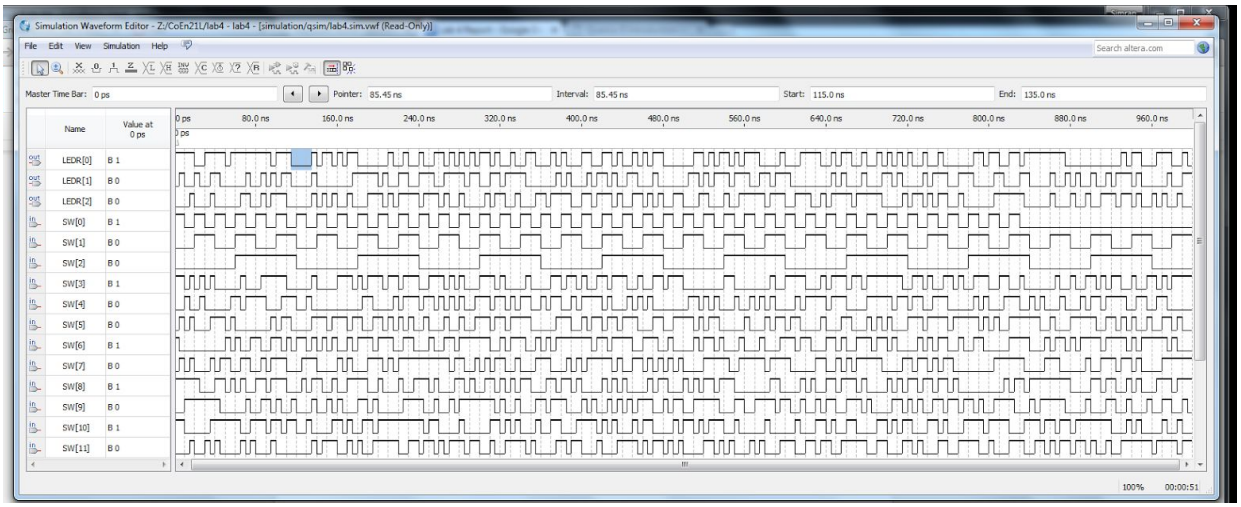


7. Once we had made sure that our 5:1 Mux worked correctly from our simulation, we moved on to building the schematic for a 3 bit wide, 5:1 MUX.
In order to test this MUX, we had to output the result of each bit to an LED light, and ensure that functionality was as expected.

Schematic for our 3 bit wide, 5:1 MUX



Simulation for our 3 bit wide, 5:1 MUX



IV. Results

The results of the lab directly matched the logic design and schematics from the pre lab. The FPGA had no unintended effects and was easy to use. We tested different combinations for the select switches and the FPGA behaved as expected and displayed the appropriate LEDs.For each MUX (2:1, 5:1, 8:1), we tested the waveform simulations (shown above) and got our expected results.

V. Conclusion

The lab went smoothly. The schematics from the pre-lab helped us to create our final schematic in the Quartus II program. Initially, we had trouble getting the correct LEDs on the FPGA to light up according to the truth table but after fixing errors in the schematic, the circuit ran correctly. We practiced how to use Altera Quartus II to implement logic design. We gained experience with running the circuit and analyzing the waveforms in order to determine whether our circuit design was implemented correctly. Using the Altera tutorial, we did pin assignments to use the on-board switches for inputs and the LEDs as outputs. Finally, we ran our circuit on the FPGA with success. In this lab, we learned how to use multiplexers hierarchically and also implement the basic logic design of multiplexers. This lab also helped us in understanding how to: construct logic design, implement the logic using a schematic, and test the circuit using Altera Quartus II and the FPGA.

VI. References

- Ogunfumi, T. *Laboratory #4: Multiplexer Design (Part 1).* 2016. Print.
- Quartus II Tutorial
    - ftp://ftp.altera.com/up/pub/Altera_Material/12.1/Tutorials/Schematic/Quartus_II_Introduction.pdf
- Waveform Simulator Tutorial
    - ftp://ftp.altera.com/up/pub/Altera_Material/13.1/Tutorials/Verilog/Quartus_II_Simulation.pdf

- Pin Assignment Chart
    - ftp://ftp.altera.com/up/pub/Altera_Material/12.1/Boards/DE2-115/DE2_115_User_Manual.pdf