LABORATORIO DE DISEÑO DE SISTEMAS DIGITALES
PRÁCTICA 6

Ángeles Cruz Israel Aarón

PROBLEMA:

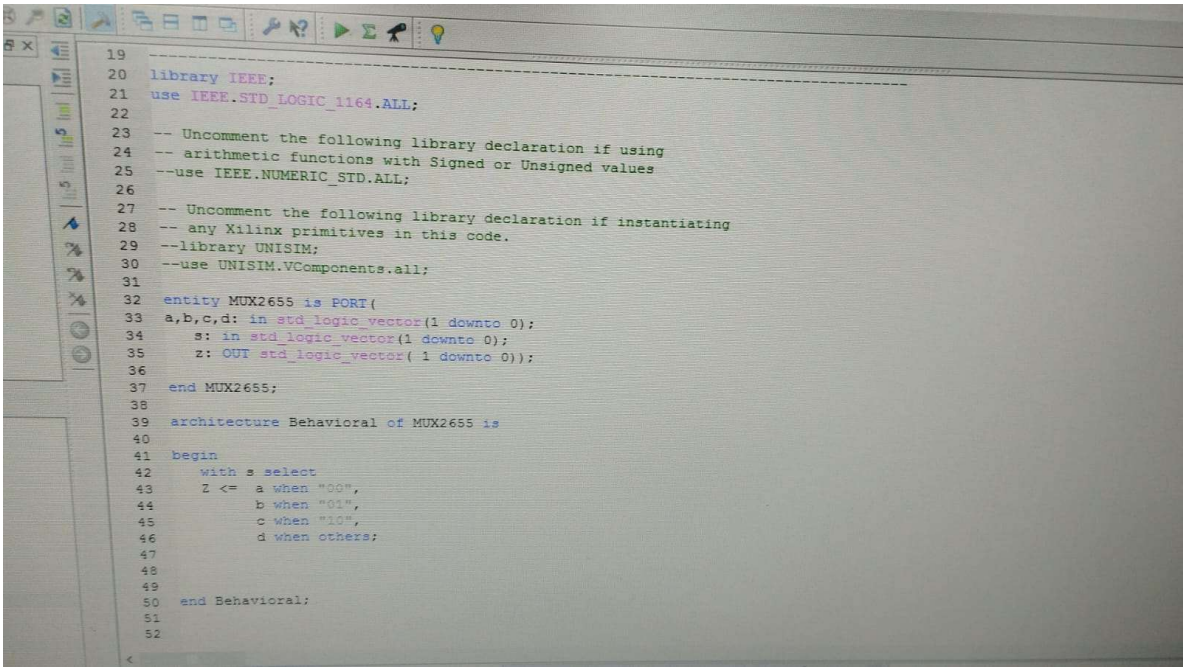
Diseñe un multiplexor con un selector de dos entradas, es decir la combinación de 00 hasta 11, con cuatro entradas de a - d y una salida z de 00 - 11.

Solución:

```
Library IEEE;
Use IEEE.STD_LOGIC_1164.ALL;

entity MUX is PORT(
a,b,c,d: in std_logic_vector(1 downto 0);
      s: in std_logic_vector(1 downto 0);
      z: OUT std_logic_vector(1 downto 0));
end MUX;

architecture Behavioral of MUX is
begin
  with s select
  z <=  a when "00";
        b when "01",
        c when "10",
        d when others;
end Behavioral;
```



```
19  ----------------------------------------------------------------------------------
20  library IEEE;
21  use IEEE.STD_LOGIC_1164.ALL;
22
23  -- Uncomment the following library declaration if using
24  -- arithmetic functions with Signed or Unsigned values
25  --use IEEE.NUMERIC_STD.ALL;
26
27  -- Uncomment the following library declaration if instantiating
28  -- any Xilinx primitives in this code.
29  --library UNISIM;
30  --use UNISIM.VComponents.all;
31
32  entity MUX2655 is PORT(
33  a,b,c,d: in std_logic_vector(1 downto 0);
34     s: in std_logic_vector(1 downto 0);
35     z: OUT std_logic_vector( 1 downto 0));
36
37  end MUX2655;
38
39  architecture Behavioral of MUX2655 is
40
41  begin
42     with s select
43     Z <=  a when "00",
44           b when "01",
45           c when "10",
46           d when others;
47
48
49
50  end Behavioral;
51
52
```