

LABORATORIO DE DISEÑO DE SISTEMAS DIGITALES  
PRÁCTICA 5

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PROBLEMA:

Diseñar un buffer con una entrada y una salida, además con un enable que habilite o deshabilite la salida.

Este problema se soluciona así:

```
library IEEE;  
use IEEE.STD_LOGIC_1164.ALL;
```

```
entity BUFFER is  
  port(  
    enable: in std_logic;  
    salida: out std_logic);  
end BUFFER
```

```
architecture Behavioral of BUFFER is  
begin
```

```
  process (enable, entrada) begin  
    if enable = '0' then  
      salida <= 'Z';  
    else  
      salida <= entrada;  
    end if;  
  end process;
```

```
end Behavioral;
```

```
BUFER.vhd]
Layout Help

18 --
19
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22
23 -- Uncomment the following library declaration if using
24 -- arithmetic functions with Signed or Unsigned values
25 --use IEEE.NUMERIC_STD.ALL;
26
27 -- Uncomment the following library declaration if instantiating
28 -- any Xilinx primitives in this code.
29 --library UNISIM;
30 --use UNISIM.VComponents.all;
31
32 entity BUFER is PORT(
33     enable, entrada: in std_logic;
34     salida: out std_logic);
35
36 end BUFER;
37
38 architecture Behavioral of BUFER is
39
40 begin
41     process (enable, entrada) begin
42         if enable = '0' then
43             salida <= 'Z';
44         else
45             salida <= entrada;
46         end if;
47     end process;
48
49 end Behavioral;
50
51
```

BUFER.vhd Design Summary (Programming File Generated)