Course Code : CST 215 **KOLP/RW – 19 / 9035**

Third Semester B. E. (Computer Science and Engineering) Examination

COMPUTER ARCHITECTURE AND ORGANIZATION

Time : 3 Hours] [Max. Marks : 60

Instructions to Candidates :—

(1) All questions carry marks as indicated against them.
(2) Assume suitable data and illustrate answers with neat sketches wherever necessary.
(3) Q. **One** is compulsory.

1. (a) How do you differentiate between computer architecture and Organisation ? Can you place a real world example to define same. What are Addressing modes and why are they required ? 5 (CO 1)

(b) Apply your knowledge to Identify different addressing modes for the following :—

(i) EA = [Ri]
EA = [LOC]

(ii) EA = [Ri] + [Rj] + X

(iii) EA = [PC] + X

Also Write a program to explain Auto – increment addressing mode using LOOP ? 5 (CO 1)

2. (a) What do you understand by expanding Opcode ? Is it possible to design an expanding Opcode to allow the following to be encoded in a 12 bit instruction ? Assume a register operand requires 3 bits and this instruction set does not allow memory addresses to be directly used in an instruction :

(i) 4 instruction with 3 registers.

(ii) 255 instruction with 0 register.

(ii) 16 instruction with 0 register. 5 (CO 3)

(b) Illustrate three bus organization connecting the various parts of the CPU and Also demonstrate with example. 5 (CO 3)

3. (a) Design the flow model of Booth's algorithm for two compliment multiplication and evaluate the result of $14^{*} -5$? 6 (CO 4)

(b) Sketch the flowchart for restoring and non – restoring division method. 4 (CO 4)

OR

(c) Differentiate Hardwired and micro program control unit. 4 (CO 3)

4. (a) How many methods are available for controlling interrupts for a single device ? Can you name them ? Illustrate techniques used to handle multiple devices in brief. 4 (CO 1, CO 2)

OR

(b) Describe various Components of Virtual Memory. At what point of time the contents of Virtual memory are referred. 4 (CO 1, CO 2)

(c) Define Cache memory. What techniques are available to map the cache with main memory ? Discuss Direct and set Associative mapping and solve respectively.

A computer system uses 16 – bit memory addresses. It has a 2 K – byte cache organized in a specified manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte. Calculate the number of bits in each of the Tag, Block, and Word fields of the memory address. Solve the above problem by considering Direct Mapping and Set associative mapping independently. 6 (CO 1, CO 2)

5. (a) Why do we need to interface DMA controller ? How does data transfer takes place between device controller to DMA and CPU to DMA ? Consider the scenario and Solve the Following :

Consider the disk drive with the following specification – 12 surfaces, 512 tracks / surface, 512 sector / track, 1 kB / sector, rotation speed 3000 rpm. Assuming operation of a disk in cycle stealing mode such that whenever one byte

word is ready, it is sent to memory, similarly, for writing and the disk interface reads a 2 byte word from the memory in each DMA cycle. Considering Memory cycle time as 40 nsec. Discover the maximum percentage of time that the CPU gets blocked during DMA operation. 5 (CO 2)

(b) Illustrate techniques used to handle multiple devices in brief. 5 (CO 2)

6. (a) Differentiate between synchronous and asynchronous bus transfer. 5 (CO 1)

(b) What functions are to be performed by a typical I/O interface ? Explain the interrupt driven mode of data transfer and the DMA driven data transfer elaborating on how they are accomplished and their relative merits and demerits. 5 (CO 1)