Course Code : CST 251 **KOLP/RW – 19 / 9037**

Third Semester B. E. (Computer Science and Engineering) Examination

FUNDAMENTALS OF DIGITAL LOGIC AND COMPUTER ARCHITECTURE

Time : 3 Hours] [Max. Marks : 60

Instructions to Candidates :—

(1) All questions carry marks as indicated against them.

(2) Assume suitable data and illustrate answers with neat sketches wherever necessary.

1. (a) Design a combinational circuit which takes 3 bit input and produces the square of input number. 5(CO1,2)

(b) Prove the following Boolean expression using Boolean algebraic rules :

(i) AB+AC'+BC=AB+AC'

(ii) (A'B'+C)(A+B)(B'+AC)'=A'BC 5(CO1)

OR

(c) Simplify the following equations using K–map;

$F = \Sigma m(0, 5, 6, 8, 9, 10, 11, 16, 20, 24, 25, 26, 27, 29, 31)$ 5(CO1)

2. (a) Find the solution for following BCD operations :

(i) 436.62–745.81

(ii) 206.7+149.9 5(CO1)

(b) Design and explain Lookahead carry adder with the help of diagram and equations. 5(CO2)

OR

(c) Explain the concept of multiplexor with the help of truth table and implement 3 input Exnor operation using 4:1 multiplexor. 5(CO2)

3. Solve any **Two** :

(a) Differentiate between Latch and Flipflop. Explain J–K–Flipflop in detail with the help of truth table and diagram. 5(CO2)

(b) Design the state diagram for the following sequential circuit :

Ja = B, Ka = BX', Jb = X', Kb = A⊕X, Y = ABX' 5(CO2)

(c) Design 3 bit UP/Down synchronous counter using D flipflop. 5(CO2)

4. (a) Explain different types of addressing modes with the help of example. 6(CO3)

OR

(b) Assuming Single bus architecture, 32 bit processor and 32 bit word length write the control signal for the following instruction

ADD(R1)+, R2 6(CO3)

(c) Convert the following numbers to IEEE single precision and double precision:

(i) 6.25×10^{-2}

(ii) 1/15 4(CO3)

5. Solve any **Two** :

(a) Distinguish between static memory and dynamic memory. Design 8M x 32 using 1M x 16 static memory chips. 5(CO4)

(b) For a block associative mapping cache with 4 blocks per set, find the main memory address format. Assume 128K word of main memory, 4K words of cache and cache block consists of 16 words. Also explain how TAG bit is used to find appropriate block in memory. 5(CO4)

(c) A two level memory system has eight different virtual pages on a disk to be mapped into four page frames in the main memory. A certain program generated the following page trace : 1, 0, 2, 2, 1, 7, 6, 7, 0,1, 2, 0, 3, 0, 4, 5, 1, 5, 2, 4, 5, 6, 7, 6, 7, 2, 4, 2, 7, 3, 3, 2, 3.

Compare hit ratio for FIFO and LRU. 5(CO4)

6. Solve any **Two** :

(a) Explain the following terms :

(i) Interrupt control in I/O

(ii) Locality of reference. 5(CO3)

(b) What are the handshaking singals and what are the sequences of events during an input operation using handshake scheme ? 5(CO3)

(c) What are the three types of hazards that cause performance degradation in pipelined processors ? Explain them in detail. 5(CO3)