Course Code : CST 251 **MQNR/MW – 19 / 9537**

Third Semester B. E. (Computer Science and Engineering) Examination

FUNDAMENTALS OF DIGITAL LOGIC AND COMPUTER ARCHITECTURE

Time : 3 Hours] [Max. Marks : 60

Instructions to Candidates :—

(1) All questions carry marks as indicated against them.

(2) Assume suitable data and illustrate answers with neat sketches wherever necessary.

1. (a) Design a combinational circuit for BCD to Gray Code convertor. 5(CO1,2)

(b) Implement the following Boolean expression using only NAND gates without reducing the equation. F = (BC + A') (B' + C'D). 5(CO1)

OR

(c) Simplify the following equations using K-map :

(i) $F = \pi M(0, 4, 8, 9, 10, 11, 12, 14)$

(ii) $F = \Sigma(4, 5, 6, 7, 12, 13, 14) + d(1, 9, 11, 15)$

5(CO1)

2. Solve any **Two** :—

(a) Design and explain BCD adder with the help of diagram and example. 5(CO2)

(b) Explain the concept of demultiplexor. Draw the demultiplexor tree for implementing 1:16 demux using 1:2 demux. 5(CO2)

(c) Design priority encoder for the following priorities : D1>D0>D2>D3. 5(CO2)

3. Solve any **Two** :—

(a) Differentiate between different types of Flip flops. Convert JK-flip flop to D-Flip-flop. 5(CO2)

(b) Design overlapping sequence detector for detecting the sequence of "1101" using T flip-flop. 5(CO2)

(c) Distinguish between synchronous and asynchronous sequential circuits. Design asynchronous mod5 counter using JK flip flop. 5(CO2)

4. (a) What is a Stack ? State some uses of the same. Show how a Stack can be implemented using auto increment and auto decrement addressing modes. Write an assembly language program using the assembly language you are familiar with to add a sequence of n numbers. Give appropriate comments. 7(CO3)

(b) Why is the wait - for - memory - function - completed step needed when reading form or writing to the main memory ? 3(CO3)

OR

(c) Differentiate between guard bits and sticky bits with example. 3(CO3)

5. (a) Distinguish between the write - through and write - back policies pointing out their relative merits and demerits. 3(CO4)

OR

(b) How many 128 x 8 RAM chips are needed to provide a memory capacity of 2048 bytes and also find how many lines of the address bus must be used to access 2048 bytes of memory ? 3(CO4)

(c) Discuss the relative advantages and disadvantages of the three mapping techniques used in cache memories. Consider a main memory of size 128 MB and a cache of size 64 KB. If the block size is 64 bytes and the cache uses 4 - way set - associative mapping, give the main memory address format and explain. 7(CO4)

6. (a) What is DMA Transfer ? How does it take place ? Write short note on the functionalities carried out by an I/O processor. 5(CO3)

OR

(b) Consider a computer in which several devices are connected to a common interrupt request line. Explain how you would arrange for interrupts from device j to be accepted before the execution of the interrupt service routine for device i is completed. Comment in particular on the times at which interrupts must be enabled and disabled at various points in the system. 5(CO3)

(c) Discuss the concept of pipelining. What is ideal speedup in a pipelined organization ? Discuss the various factors that might reduce the speedup and suggest ways of overcoming or minimizing them. 5(CO3)