Course Code : CST 204 / CST 215 **ITSJ/RW – 17 / 1019**

Third Semester B. E. (Computer Science and Engineering) Examination

COMPUTER ARCHITECTURE AND ORGANIZATION

Time : 3 Hours] [Max. Marks : 60

Instructions to Candidates :—

(1) Due credit will be given to neatness.

(2) Illustrate your answers wherever necessary with the help of neat sketches.

1. (A) Summarize the basic operational concept of a processor with neat labeled diagram. 4 (CO 1)

(B) Suppose a datapath has three operand busses (two source, one destination), 45 instruction types and 32 registers where each register is 16 bits wide. Immediate operands can be in the range of −128 K to +128 K.

(1) Design an instruction format for instruction that have one operation, one destination register and two source register. Label the fields and minimum number of bits need for each field.

(2) Design an instruction format for instruction that have one operation, one destination register and one source register, and an immediate value. Label the fields and minimum number of bits need for each field. 4 (CO 1)

(C) Describe what happens when the instruction :

ADD R1, (R2)+

is executed. Assume that the instruction is stored at main memory location 2050. [R2] = 950 and memory location 950 contains 3000. 2 (CO 1)

OR

(D) Give an example of zero–address, one–address, two–address and three–address instructions. 2 (CO 1, CO 2)

2. (A) Consider a computer system in which a memory read or write operation takes the same amount of time as any internal operation in the CPU. Is the WMFC signal needed in this case ? Why ? 2 (CO 3)

(B) Consider the following instruction :

ADD (R0)+, R1, R2

Where the first two are source operands and the third is the destination operand ? Show the control sequence to execute this instruction for a single bus organization assuming the instruction itself is only a one word. 5 (CO 3)

(C) Discuss the principle of operation of a micro programmed control unit. 3 (CO 3)

OR

(D) Point out the advantages and disadvantages of hardwired control over micro programmed control. 3 (CO 3)

3. (A) Give the booth's recoding and bit – pair recoding multiplier of the number 1000111101000101. 2 (CO 4)

(B) Discuss the Booth's multiplication algorithm. Simulate the same for 25 * (–16). 6 (CO 4)

(C) Differentiate between single and double precision IEEE standard for floating point representation. 2 (CO 4)

4. (A) Design 4 M x 32 memory using 512 K x 8 static memory chips. 6 (CO 2)

OR

(B) Write a short note on how data is read and written into disk. 6 (CO 2)

(C) Draw possible configuration for a 16 MB (4 M x 4) asynchronous DRAM. Use cell array. 4 (CO 2)

5. (A) Explain the term locality of reference with its type. 3 (CO 1, CO 2)

OR

(B) Can memory interleaving increase the speed of execution ? If yes, how and if no, why ? 3 (CO 1, CO 2)

(C) Discuss the different types of Cache mapping techniques. A 2–way set associative cache memory uses blocks of 4 words. The cache can accommodate a total of 2048 words from main memory. The main memory size is 128 K x 32. What is the size of the cache memory ? Show how the cache is organized ? 7 (CO 1, CO 2)

6. Solve any **Two** :—

(A) Three devices A, B and C are connected to the bus of a computer. I/O transfer for all three device use interrupt control. Interrupt nesting for devices A and B is not allowed but interrupt requests from C may be accepted while either A or B is being serviced. Suggest different ways in which this can be accomplished in each of the following cases :

(a) The computer has one interrupt – request line and no vectored – interrupt capability.

(b) Two interrupt – request line INTR1 and INTR2 are available, with INTR1 having higher priority.

Specify when and how interrupt are enabled and disabled in each case. 5 (CO 1)

(B) Write short note on distribute bus arbitration. 5 (CO 1)

(C) What is DMA ? Describe how DMA is used to transfer data from peripherals. 5 (CO 1)

(D) What is interrupt service routine ? Explain vector interrupt mechanism available for handling interrupts. 5 (CO 1)