Course Code : CST 215 **EVFU/MW – 18 / 6020**

Third Semester B. E. (Computer Science and Engineering) Examination

COMPUTER ARCHITECTURE AND ORGANIZATION

Time : 3 Hours] [Max. Marks : 60

Instructions to Candidates :—

(1) All questions carry marks as indicated against them.
(2) Assume suitable data and illustrate answers with neat sketches wherever necessary.
(3) **Q.1** is compulsory.

1. (a) The memory unit of a computer has 256 K words of 32 bits each. The computer has an instruction format with 4 fields: an operation code field, a mode field to specify one of the seven addressing modes, a register address field to specify one of 60 processor registers, and a memory address. Specify the instruction format and the number of bits in each field if the instruction is in one memory word. 3(CO 2)

   (b) Consider the possibility for saving the return address of a subroutine. Can a processor register be used if subroutine nesting has to be supported? Justify the answer and provide the solution for implementing subroutine nesting. 2(CO 1)

   (c) Write assembly language program for following task using two address instruction.

   $$Z = a_n x^n + a_{n-1} x^{n-1} + ... + a_1 x + a_0$$ 5(CO 1)

2. (a) Draw the 20 bits micro instruction code format. 2(CO 3)

   (b) Give a typical single bus organization connecting the various parts of the CPU and show how an instruction like SUB R0, R1, (R2) gets executed here. Assume that the instruction is a one word instruction and R0, R1 are source operands where (R2) is the destination operand. 6(CO3)

OR

Consider the following instruction :

ADD (R0)+, R1, R2

Where the first two are source operands and the third is the destination operand. Show the control sequence to execute this instruction for a single bus organization assuming the instruction itself is only a one word instruction. 6(CO 3)

(c) What are the control signals associated with each register ? 2(CO 3)

3. (a) Consider a 16 bit, floating point number with a 6 bit exponent and a 9 bit fractional mantissa where the base is 2 and the exponent is represented in excess–31 format. Add the numbers a, b formatted as follows

A = 0100001 111111110

B = 0011111 001010101.

Give the answer in the normalized form. Use rounding to get the 9 bit mantissa. 6(CO 4)

OR

Discuss the concept of bit pair recoding. Multiply the following pair of signed 2's complement numbers using bit pair recoded multiplier. Multiplicand=110011 and Multiplier = 101100. Give the Booth multiplier recoding table. 6(CO 4)

(b) Draw flowchart for restoring and non–restoring division method. 4(CO 4)

4. (a) Discuss the concept of pipelining. What is ideal speedup in a pipelined organization ? Discuss the various factors that might reduce the speedup and suggest ways of overcoming or minimizing them. 4(CO 1,CO 2)

OR

(a) Discuss advantages and disadvantages of virtual memory. 4(CO 1,CO 2)

(b) Discuss the different types of Cache mapping techniques. A 2–way set associative cache memory uses blocks of 4 words. The cache can accommodate a total of 2048 words from main memory. The main memory size is 128 K X 32. What is the size of the cache memory ? Show how the cache is organized ? 6(CO 1,CO 2)

5. (a) For a memory of a capacity 512 KB, how many 16 K X I RAM chips will be needed ? 2(CO 2)

(b) Write short note on ROM memories and its types. 4(CO 2)

OR

A disk system has 18 recording surfaces with 1024 tracks/surface. There are 16 Sectors/track, each sector contains 1024 bytes. The inner and out diameter of a disk is 5 and 9 inch respectively.

(i) What is the total disk capacity ?

(ii) What is the track density ?

(iii) What is the maximum bit density ?

What is the data transfer rate if rotational speed is 7200 rpm? 4(CO 2)

(c) Show the organization of 16–megabit Dynamic–RAM chip,configured as 2M x 8. The cells must be organized using 4K x 4K array. 4(CO 2)

6. (a) What are the functions to be performed by a typical I/O interface ? Explain the interrupt driven mode of data transfer and the DMA driven data transfer elaborating on how they are accomplished and their relative merits and demerits. 6(CO 1)

(b) Differentiate between synchronous and asynchronous bus transfer. 4(CO 1)

OR

Explain how data may be transferred from a hard disk to memory using DMA including arbitration for the bus. Assume a synchronous bus, and draw a timing diagram showing the data transfer. 4(CO 1)