Course Code : CST 215 **CXDW/RW – 18 / 5020**

Third Semester B. E. (Computer Science and Engineering) Examination

COMPUTER ARCHITECTURE AND ORGANIZATION

Time : 3 Hours] [Max. Marks : 60

Instructions to Candidates :—

(1) Attempt all questions compulsory.
(2) All questions carry marks as indicated against them.
(3) Due credit will be given to neatness and adequate dimensions.
(4) Assume suitable data and illustrate answers with neat sketches wherever necessary.

1. Solve any **One** from (b) and (c) :

(a) What are Addressing modes and why are they required ? Propose an addressing mode suitable for implementing stacks. Give the implementation of stack in assembly using the above mentioned addressing mode. 6(CO1)

(b) (i) Write a program to evaluate the expression :

A X B + C X D

In a single accumulator processor assume that the processor has load, store, Multiply and add instructions and that all the values fit in the accumulator. 2(CO1)

(ii) Suppose a data path has three operand busses (Two sources and one destination), 45 instruction type and 32 registers where each register is 16 bits wide. Immediate operands can be in the range of ±128k. Design an instruction format for instruction that have one operation, one destination register and two source register. Label the fields and minimum number of bits need for each field. 2(CO1)

(c) Given 8 bit instruction, is it possible to use expanding Opcode to allow the following to be encoded ? If so show the encoding of :

(i) 3 instruction with two 3-bit operand

(ii) 2 instructions with one 4-bit operand.

(iii) 4 instructions with one 3-bit operand. 4(CO1)

2. Solve any **Two** :

(a) Apply single bus organization of the data path of a CPU to represent control sequence for execution of the instruction ADD (R3), R1. 5(CO3)

(b) Compare and contrast between Hardwired and Micro programmed control unit ? 5(CO3)

(c) Compare RISC and CISC ? 5(CO3)

3. Solve any **Two** :

(a) How do we represent Floating point numbers ? Design the format structure if the range of exponent in single precision format is –126 to +127. 5(CO4)

(b) Design the flow model of Booth's algorithm for multiplication of signed two's complement numbers, explain in brief. Present its Design issues. 5(CO4)

(c) Write an algorithm for restoring division method. Also perform 15/8. 5(CO4)

4. Solve any **Two** :

(a) Design the internal organization of Synchronous DRAM. Also provide a necessary sketch of control time relationship diagram with burst read of length 4 in an SDRAM. 5(CO2)

(b) Give an overview of organization of data on optical disk and magnetic Tape ? 5(CO2)

(c) Criticize the following statement, "using a faster processor chip results in a corresponding increase in performance of a computer even if the main memory speed remains the same". 5(CO2)

5. Solve any **Two** :

(a) What are Hit Rate and Miss Penalty ? Consider the following analogy for the concept of caching. A serviceman comes to a house to repair the heating system. He carries a toolbox that contains the number of tools that he has used recently in similar jobs. He uses these tools repeatedly, until he reaches a point where other tools are needed. It is likely that he has the required tool in his truck outside the house. But, if needed tools are not in the truck, he must go to his shop to get them. Suppose we argue that the toolbox, the truck and the shop correspond to the L1 and L2 cache, and the main memory of a computer. How good is this analogy ? Discuss its correct and incorrect features ? (CO1,CO2)

(b) How do we proceed with address translation method by using associative mapped TLB in virtual memory organization ? Show all necessary views in it with neat sketch. 5(CO1,CO2)

(c) An instruction pipeline has five stages where each stage takes 2 nano seconds and all instructions use all five stages. Branch instruction are not overlapped, i.e the instruction after the branch is not fetched till the branch instruction is completed under ideal conditions :

(i) Calculate the average instruction execution time assuming that 20% of all instruction executed are branch instruction. Ignore the fact that some branch instructions may be conditional.

(ii) If a branch instruction is conditional, the branch need not be taken; if the branch is not taken, the following instructions can be overlapped. When 80% of all branch instructions are conditional Branch instruction and 50% of conditional Branch Instruction are such that the branch is taken. Calculate the average instruction execution time. 5(CO1,CO2)

6. (a) List three methods of controlling interrupts for a single device. Explore the techniques used to handle multiple devices in brief ? 5(CO1)

(b) Consider the disk drive with the following specification 16 surfaces, 512 tracks/surface, 512 sector/tracks, 1kB/sector, rotation speed 3000 rpm. The disk is operated in cycle stealling mode whereby whenever one byte word is ready, it is sent to memory, similarly, for writing, and the disk interface reads a 4 byte word from the memory in each DMA cycle. Memory cycle time is 40 nsec. Find out the maximum percentage of time that the CPU gets blocked during DMA operation. 5(CO1,CO2)