Course Code : CST 214/202 **JSRK/MW – 17 / 2018**

Third Semester B. E. (Computer Science and Engineering) Examination

DIGITAL CIRCUITS AND FUNDAMENTAL OF MICROPROCESSORS

Time : 3 Hours] [Max. Marks : 60

Instructions to Candidates :—

(1) All questions carry marks as indicated against them.
(2) Due credit will be given to neatness and adequate dimensions.
(3) Assume suitable data and illustrate answers with neat sketches wherever necessary.

1. (a) Reduce the following expression to the simplest possible POS and SOP forms

$f = \Sigma m(6, 9, 13, 18, 19, 25, 27, 29, 31) + d(2, 3, 11, 15, 17, 24, 28)$

6 (CO 1)

(b) (i) Perform BCD addition- 679.6 + 536.8

(ii) Convert the following- 11011.101_2 to decimal

(iii) Convert the following- $B9F.AE1_6$ to octal

2+1+1 (CO 1)

OR

(c) Reduce the expression: $A[B + C'(AB + AC)']$ using Boolean algebra.

4 (CO 1)

2. Solve any **Two** :—

(a) What do you mean by combinational circuit ? Design a combinational logic circuit by finding its minimal expressions in both SOP and POS forms where logic circuit will have 4 inputs A, B, C, D that will produce output '1' only whenever two adjacent input variables are 1's. A and D are also to be treated as adjacent. Implement it using any one universal logic gates.

5 (CO 2)

(b) Design and explain a combinational circuit for 4 bit Look Ahead Carry Adder. 5 (CO 2)

(c) Illustrate an implementation of BCD subtractor using 10's complement method with design. 5 (CO 2)

3. A clocked sequential mealy circuit is provided with a single input x and a single output z, whenever the input produces a string of pulses 111 or 000 and at the end of the sequence it produces an output z = 1 using D-FF and overlapping is also allowed.

(i) Obtain the state diagram.

(ii) Obtain the state table.

(iii) Design the sequence detector circuit. 10 (CO 3)

OR

4. (a) Explain excitation table. Convert SR slip-flop to JK flip-flop. 5 (CO 3)

(b) A sequential circuit with two JK flip-flops A and B, one input X and output Z is verified by the following input equations :

$J_1 = X'Q_0$

$K_1 = X + Q_0$

$J_0 = K + Q_1$

$K_0 = X'$

(a) Draw excitation table

(b) Draw state diagram

(c) Draw sequential circuit. 5 (CO 3)

5. Solve any **Two** :—

(a) Explain how synchronous and asynchronous counters differ from each other. Design a Mod-10 asynchronous counter using T-FF. 5 (CO 3,4)

(b) Design the self start counter that goes from state 0, 1, 2, 4 and back to 0. The undesired states must always go to zero (0000) on the next clock pulse. (use D flip-flop). 5 (CO 3,4)

(c) Explain shift registers. Give the design for a 4-bit serial in serial out register which will shift its content towards right serially after the application of clock input. Initially register is in reset state. Mention how many clock pulses are required to store the 4-bit information in the register and to shift the information from this register using truth table. Consider the bit string "1101" to in and out from the register. 5 (CO 3, 4)

6. (a) Describe PLA ? Design PLA circuit to implement BCD to excess-3 code conversion. 6 (CO 2, 4)

OR

(b) Implement the following functions using PAL --- :—

$w(A, B, C, D) = \Sigma m(2, 12, 13)$

$x(A, B, C, D) = \Sigma m(7, 8, 9, 10, 11, 12, 13, 14, 15)$

$y(A, B, C, D) = \Sigma m(0, 2, 3, 4, 5, 6, 7, 8, 10, 11, 15)$

$z(A, B, C, D) = \Sigma m(1, 2, 8, 12, 13)$ 6 (CO 2, 4)

(c) Design the memory system for 256 K X 8 RAM using 64 K x 8 RAM. 4 (CO 2, 4)

7. Solve any **Two** :—

(a) Write an assembly language program that will add 10 data bytes stored at memory address 2000 H and onwards and store their 8-bit sum at 2050 H. 5 (CO 4)

(b) Explain flag register of 8085 microprocessor. 5 (CO 4)

(c) Explain the action of PUSH and POP instruction in 8085 microprocessor on stack pointer and program counter. 5 (CO 4)