Course Code : CST 215 **MQNR/MW – 19 / 9535**

Third Semester B. E. (Computer Science and Engineering) Examination

COMPUTER ARCHITECTURE AND ORGANIZATION

Time : 3 Hours] [Max. Marks : 60

Instructions to Candidates :—

(1) All questions carry marks as indicated against them.
(3) Q. **Six** is compulsory.

1. Solve any **Two** :

(a) Suppose a datapath has three operand busses (two source, one destination), 45 instruction types and 32 registers where each register is 16 bits wide. Immediate opearands can be in the range of -128K to +128K.

(1) Design an instruction format for instruction that have one operation, one destination register and two source register. Lable the fields and minimum number of bits need for each field.

(2) Design an instruction format for instruction that have one operation, one destination register and one source register, and an immediate value. Lable the fields and minimum number of bits need for each field. 5(CO1)

(b) Explain in detail the different types of instrutions that are supported in a typical processor. Registers R1 and R2 of a computer contain the decimal values 1200 and 2400 respectively. What is the effective address of the memory operand in each of the following instructions ?

(a) Load 20 (R1), R5

(b) Add–(R2), R5

(c) Move # 3000, R5

(d) Sub (R1) +, R5. 5(CO1)

(c) With the help of a block diagram, explain the basic functional units of a computer. 5(CO1)

2. (a) Give a typical single bus organization connecting the various parts of the CPU and show how an instruction like ADD R1, (R2), R3 gets executed. Assume that the instruction is a one word instrution and R1, (R2) are source operands where R3 is the destination operand. 6(CO3)

(b) Consider a computer system in which a memory read or write operation takes the same amount of time as any internal operation in the CPU. Is the WMFC signal needed in this case ? Why ? Justify with example. 4(CO3)

OR

(c) Differentiate between hardwired and microprogrammed control unit design. 4(CO3)

3. (a) Discuss a multiplier that multiplies two 4- bit numbers. Describe the algorithm for integer division with suitable example. 7(CO4)

(b) Write IEEE standared for a double precision floating point format and explain the various fields. 3(CO4)

OR

(c) Give examples for worst case, ordinary and good multipliers under the booth multiplication scheme. 3(CO4)

4. Solve any **Two** :—.

(a) For the memory capacity of 256 KB, how many 32 k x 1 RAM will be needed ? Draw and explain. 5(CO2)

(b) Describe dynamic RAM with significance of capacitor. 5(CO2)

(c) A disk system has 18 recording surfaces with 1024 tracks/ surface. There are 16 Sectors/ track, each sector contains 1024 bytes. The inner and out diameter of a disk is 5 and 9 inch respectively.

(i) What is the total disk capacity ?

(ii) What is the track density ?

(iii) What is the maximum bit density ?

(iv) What is the data transfer rate if rotational speed is 7200 rpm? 5(CO2)

5. (a) Illustrate how speed-up achieved through pipelining. Draw the pipelining diagram for the following cases having four instructions in total :

(a) Data hazard in second instruction.

(b) Instruction hazard in second instruction.

(c) Structural hazard in second instruction. 6(CO2)

OR

(b) How do we proceed with address translation method by using associative mapped TLB in virtual memory organization ? Show all necessary views in it with neat sketch. 6(CO2)

(c) Define cache memory. Also describe mapping function of cache memory. 4(CO2)

6. (a) Explain the working of Daisy chain and priority based daisy chain interrupt handling mechanism. 5(CO1)

(b) Explain the Centralized and distributed Bus arbitration. 5(CO1)