

Course Code : CST 204/CST 215

JSRK/MW – 17 / 2019

**Third Semester B. E. (Computer Science and Engineering)
Examination**

COMPUTER ARCHITECTURE AND ORGANIZATION

Time : 3 Hours]

[Max. Marks : 60

Instructions to Candidates :—

- (1) Due credit will be given to neatness and adequate dimensions.
- (2) Illustrate your answers wherever necessary with the help of neat sketches.

1. (A) Why data bus is bidirectional and address bus is unidirectional in most of the microprocessors ? 2 (CO 1)
- (B) State use of the stack for subroutine handling. Show how a Stack can be implemented using auto increment and auto decrement addressing modes. 4 (CO 1)

OR

- (C) Write an assembly language program to add a sequence of n numbers. Give appropriate comments. 4 (CO 1)
 - (D) Write assembly language program for following task.
$$C = \sum_{i=1}^n A_i * B_i$$
 4 (CO 1, CO 2)
2. (A) Give a typical single bus organization connecting the various parts of the CPU and show how an instruction like SUB R0, R1, (R2) gets executed. Assume that the instruction is a one word instruction and R0, R1 are source operands where (R2) is the destination operand. 6 (CO 3)

OR

- (B) Give the organization of a typical hardwired control unit and explain the functions performed by the various blocks. Discuss the dataflow for a sample instruction. 6 (CO 3)

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Contd.

- (C) What is the purpose of multiplexer in giving input to ALU ? 2 (CO 3)
- (D) Draw the 20 bits micro instruction code format. 2 (CO 3)
3. (A) How many addition/subtraction done for the multiplier value 01110110 in Booths algorithm ? Justify. 2 (CO 4)
- (B) Give examples for worst case, ordinary and good multipliers under the Booth multiplication scheme. 3 (CO 4)
- OR**
- (C) What is the mantissa part of a floating point number ? How would you calculate the exponent part of a floating point number ? 3 (CO 4)
- (D) Discuss the restoring division algorithm and give a possible implementation for it. Simulate the same for 24/9. 5 (CO 4)
4. (A) Which memories are faster: Dynamic or static ? Why ? 2 (CO 2)
- OR**
- (B) For a memory of a capacity 256 KB, how many 32 K X 1 RAM chips will be needed ? 2 (CO 2)
- (C) Consider a disk pack with a seek time of 4 ms and rotational speed of 10000 RPM. It has 600 sector/track and each sector can store 512 bytes of data. Consider a file stored in the disk. The file contains 2000 sector. Assume that every sector access necessitates a seek and the average rotational latency for accessing each sector is half of time for one complete rotation. How much total time is needed to read entire file ? 6 (CO 2)
- (D) Explain Flash memory in detail. 2 (CO 2)
- OR**
- (E) Write about function of memory organization. 2 (CO 2)

5. (A) Distinguish between the write – through and write – back policies pointing out their relative merits and demerits. 3 (CO 2)
- (B) Derive the expression for the average memory access time for a system with three levels of caches with hit ratios h_1 , h_2 and h_3 and access times t_{c1} , t_{c2} , t_{c3} and main memory access time t_m . Explain the same. 3 (CO 2)
- (C) An eight-way set-associative cache consists of a total of 256 blocks. The main memory contains 8192 blocks, each consisting of 128 words.
- (a) How many bits are there in the main memory address ?
- (b) How many bits are there in the TAG, SET and WORD fields? 1 + 3 (CO 2)

OR

- (D) What is meant by virtual memory ? Explain how virtual address is mapped to physical address using paging technique. 4 (CO 2)
6. Solve any **Two** :—
- (A) What are the functions to be performed by a typical I/O interface ? Explain the interrupt driven mode of data transfer and the DMA driven mode of data transfer elaborating on how they are accomplished and their relative merits and demerits. 5 (CO 1)
- (B) Write in detail about memory mapped I/O and I/O mapped I/O. 5 (CO 1)
- (C) Explain daisy chain mechanism of handling interrupts. Can daisy chain method handle priority groups ? Explain. 5 (CO 1)