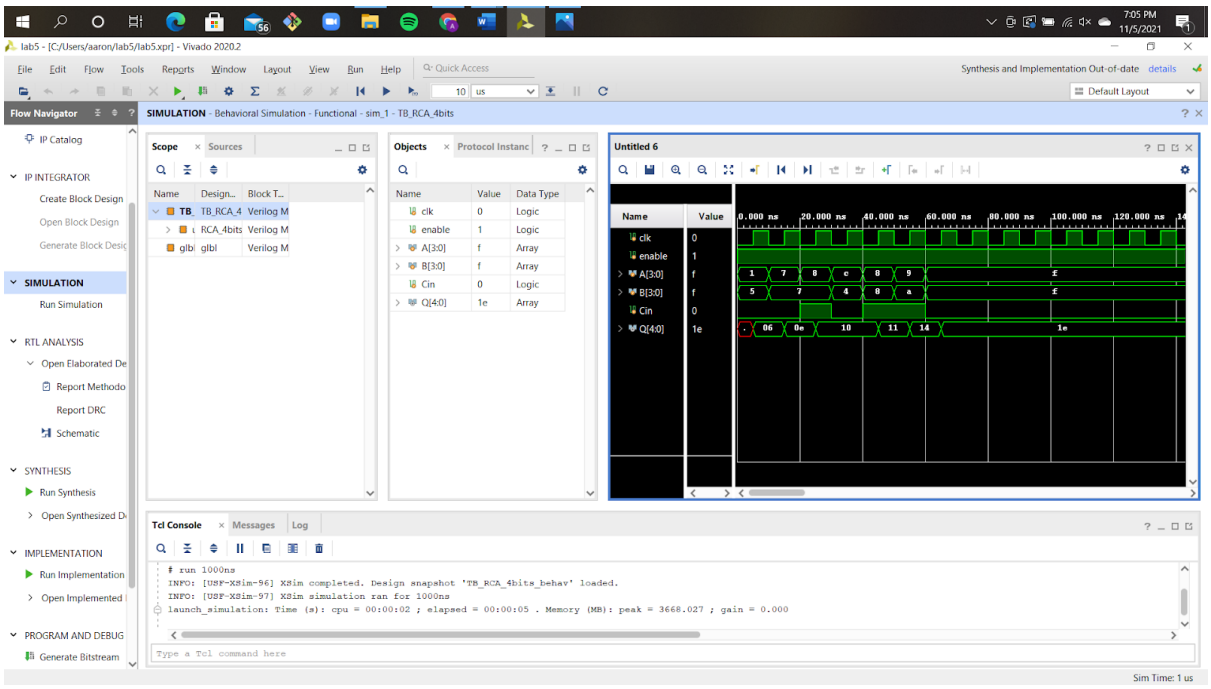
i. Complete Table 1 from the simulation(Ripple adder)

A[3:0]	B[3:0]	Cin	Sum[3:0]	Cout
0001	0101	0	0110	0
0111	0111	0	1110	0
1000	0111	1	0000	1
1100	0100	0	0000	1
1000	1000	1	0001	1
1001	1010	1	0100	1
1111	1111	0	1110	1

i. Simulation waveform for the above test-cases

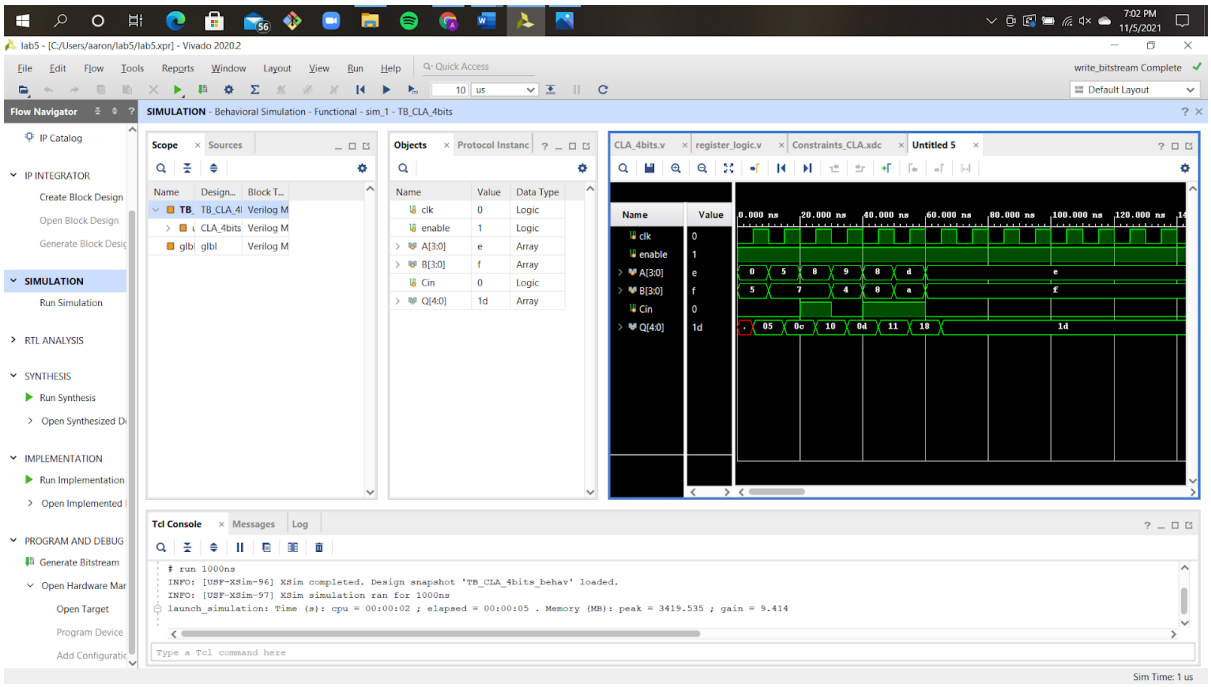


i. Complete Table 2 from the simulation(Carry lookahead adder)

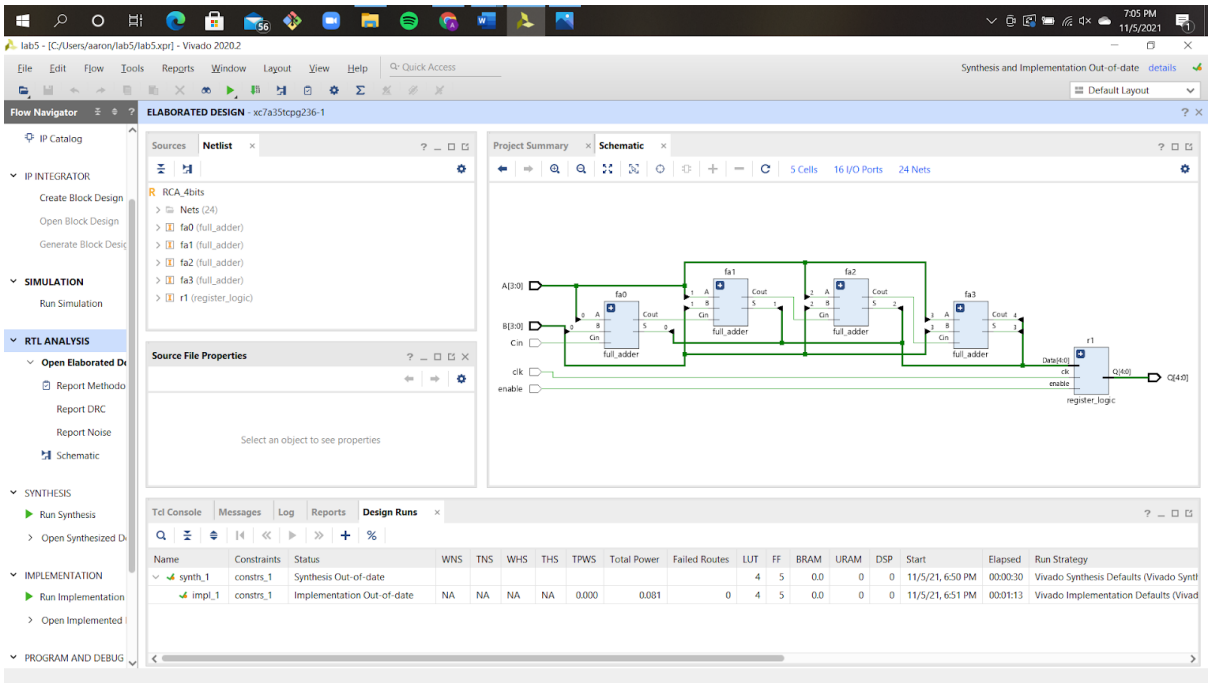
A[3:0]	B[3:0]	Cin	Sum[3:0]	Cout
0000	0101	0	0101	0
0101	0111	0	1100	0
1000	0111	1	0000	1
1001	0100	0	1101	0
1000	1000	1	0001	1
1101	1010	1	1000	1
1110	1111	0	1101	1

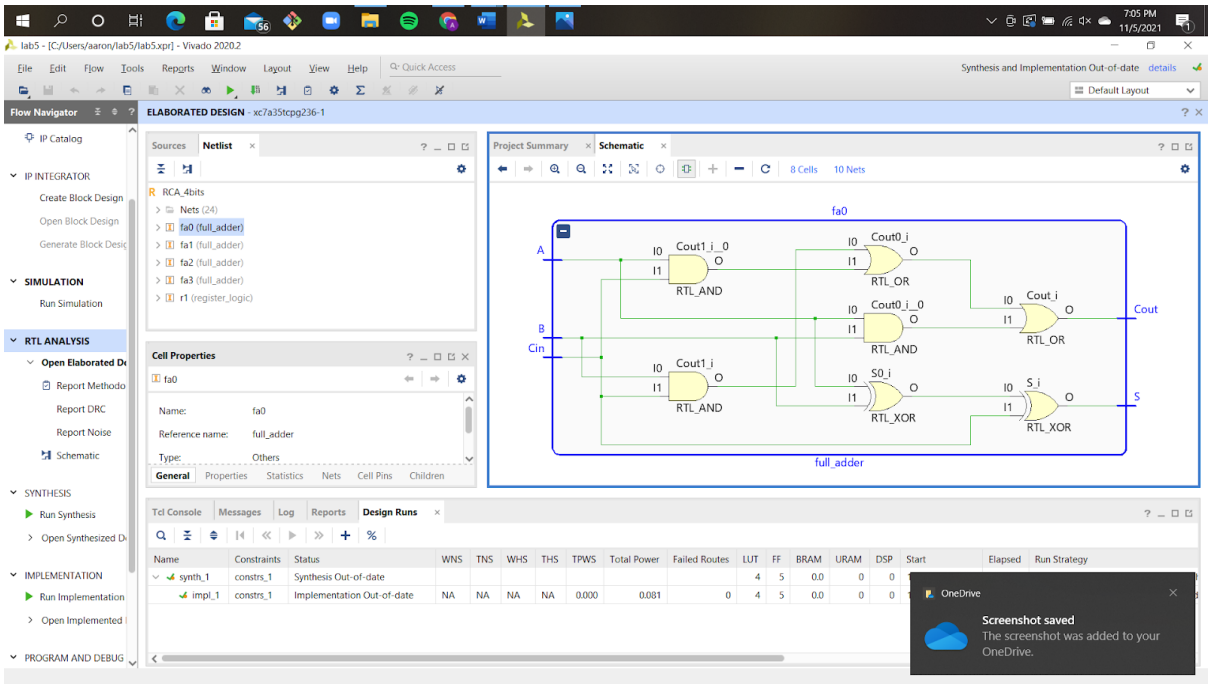
Table 2. Testcases for Carry Lookahead Adder Verification

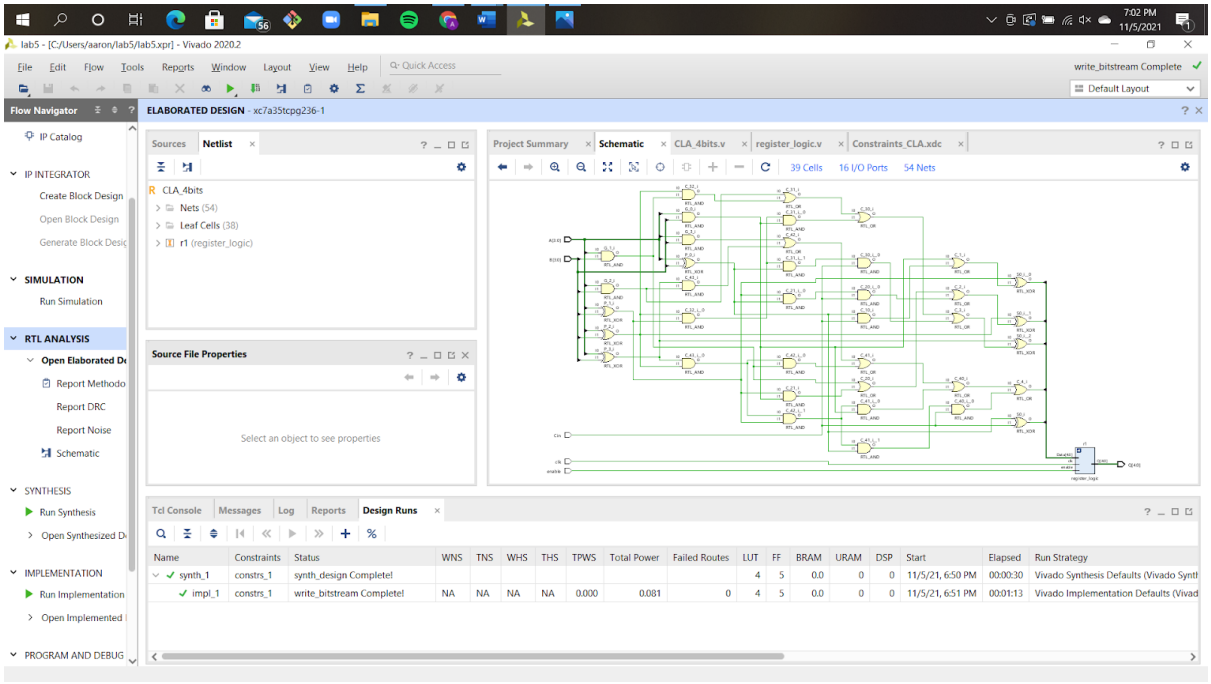
i. Simulation waveform for the above test-cases



i. Screenshots of the gate-level schematics for both the adder techniques






7:02 PM
11/5/2021
lab5 - [C:/Users/aaron/lab5/lab5.xpr] - Vivado 2020.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
write_bitstream Complete
Default Layout
Flow Navigator
ELABORATED DESIGN - xc7a35tcpg236-1
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Desig
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated D
Report Methodo
Report DRC
Report Noise
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized D
IMPLEMENTATION
Run Implementation
Open Implemented
PROGRAM AND DEBUG
Sources
Netlist
CLA_4bits
Nets (54)
Leaf Cells (38)
r1 (register_logic)
Source File Properties
Select an object to see properties
Project Summary
Schematic
CLA_4bits.v
register_logic.v
Constraints_CLA.xdc
39 Cells
16 I/O Ports
54 Nets
Tcl Console
Messages
Log
Reports
Design Runs
Name
Constraints
Status
WNS
TNS
WHS
THS
TPWS
Total Power
Failed Routes
LUT
FF
BRAM
URAM
DSP
Start
Elapsed
Run Strategy
synth_1
constrs_1
synth_design Complete!
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Vivado Synthesis Defaults (Vivado Synth
impl_1
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write_bitstream Complete!
NA
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Vivado Implementation Defaults (Vivad