# CS 278 Study Guide #4: Computer Architecture

Due 3/10

## NAME: Aaron Borjas

**GRADE:**

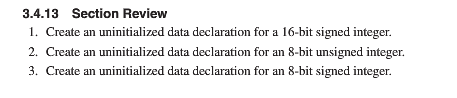
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| --- | --- | --- |
| **CATEGORY** | **POINTS** |  |
| EX04\_01 |  | 10 |
| EX04\_02 |  | 15 |
| EX04\_03 |  | 25 |
| EX04\_04 |  | 25 |
| EX04\_05 |  | 25 |
| **TOTAL** |  | 100 |

## EXERCISES:

**Answer the following written questions (EX04\_01, EX04\_02) in this Word Document. Please show your work where appropriate. For EX04\_03 - EX04\_05, place each problem in a assembler folder of the same name as the problem. Submit all folders and the word document using Whitgit.**

**EX04\_01 –** Answer ALL the review question on pages 3 & 4 of this document.

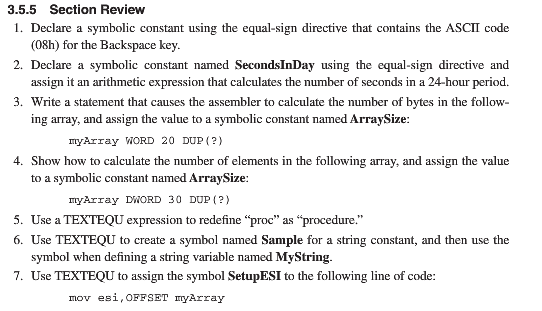
**EX04\_02 –** Answer ALL the section review questions below.





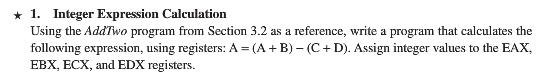
1. temp1 SWORD ?
2. temp2 BYTE ?
3. temp3 SBYTE ?
4. temp4 QWORD ?
5. A DWORD (double word) can hold a 32-bit signed integer

**EX04\_03 –** Answer ALL the section review questions for 3.5.5 on page 88



1. backspace\_key = 08h
2. SecondsInDay = 24\*60\*60
3. ArraySize = ($ - myArray)/2
4. ArraySize = ($ - myArray)/4
5. procedure TEXTEQU <proc>
6. Sample TEXTEQU <“HELLO WORLD”>
7. SetupESI TEXTEQU <move esi, OFFSET myArray>

**EX04\_04 –** Do programming problem on page 1 on page 100



**EX04\_05 –** Do programming problem on page 4 on page 100

# CS278 Study Guide 4: Data Representation

## Reading Assignment for Next Class Period

* Read Chapter 3.1 to 3.3 of Irvine

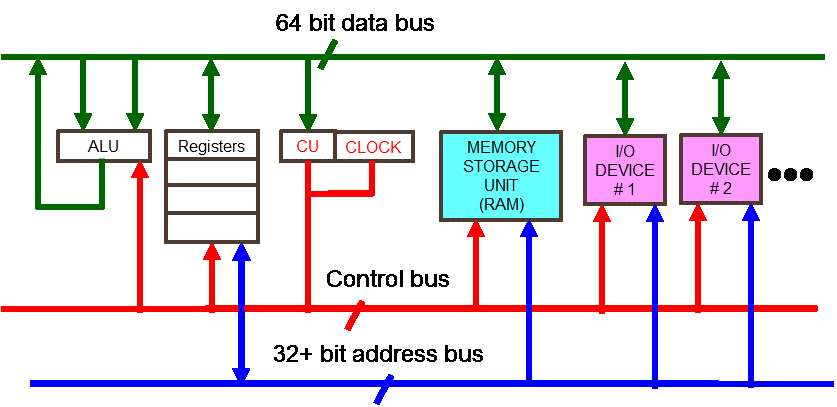
## Background Material for this Session

* Chapter 2.1-2.5 of Irvine

## Learning Goals for this Study Guide

* Understand Data Representation

## Understanding Computer Architecture

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**Write out your answers to these questions and turn them in with the other written questions.**

**Question 1:** What is the Fetch, Decode, Execute Cycle, and what happens in each phase of the cycle?

Fetch goes out to an area in memory called the instruction queue and increments the instruction pointer after doing so. Decode is when the CPU looks at the binary bit pattern to see if the instruction has operands. Execute is when the CPU executes the instruction decoded in the previous step.

**Question 2:** The Intel Extreme 2 Dual Core Processor has a clock frequency of 2.67 Giga Hertz. Approximate how many machine instructions it perform in 1 second:

5.34 billion operations per second (1,000,000,000 hertz (operations per second) per gigahert)

**Question 3:** What is the performance bottleneck in modern computers?

The way the computer accesses memory. The further out it goes from the CPU the worse the performance gets and the longer it takes to perform actions. This is the “fetch” part.

**Question 4:** What is the purpose of cache and branch prediction?

Cache is where the most recently used instructions are stored. The reason these instructions are stored here is because the cache is super high-speed memory, so instructions can be accessed rapidly. Branch prediction is when the computer guesses which option an if-else statement will go to. The reason this is important is because it tries not to waste any time by trying to guess which option will most likely be predicted

**Question 5**: A CPU contains registers and what other elements?

Clock, control unit (CU), arithmetic logic unit (ALU)

**Question 6**: What busses connect the CPU to the rest of the computer system?

Data bus, I/O bus, control bus, address bus

**Question 7**: In this class we will focus on Protected Mode operation of the x86 processors. What are the features of protected mode?

Every feature and instruction are available to use. Segments, separate memory areas, are given to programs. Processor prevents programs from getting memory outside of their assigned segment.