Birla Institute of Technology & Science, Pilani
Hyderabad Campus

INSTRUCTION DIVISION
SECOND SEMESTER 2021 - 2022
Course Handout Part II

03-01-20221

In addition to part-I (General Handout for all courses appended to the time table) this portion gives further specific details regarding the course.

Course No.	:	EEE F348
Course Title	:	FPGA Based System Design Laboratory
Instructor-in-Charge	:	Amit Kumar Panda
Instructors	:	Samala Jagadheesh, Aditi Sood, Venkatarao Selamneni

Scope and Objective of the Course:

HDL (hardware description language) and FPGA (field-programmable gate array) devices allow designers to quickly develop and simulate a sophisticated digital circuit, realize it on a prototyping device, and verify operation of the physical implementation. It combines together the flexibility of a microprocessor and high performance of an Application Specific Integrated Circuit (ASIC). The ease of programming and debugging with FPGAs, as compared to ASICs, decreases the overall non-recurring-engineering (NRE) costs and time-to-market of FPGA-based products. In this lab-oriented course, students will develop their skills by working on more challenging digital system design using Verilog hardware description language (HDL) in an industry-standard design environment. Students will also implement real-world designs in field programmable gate arrays (FPGAs) as well as test and optimize the FPGA-implemented systems.

Textbooks :

1. Wolf Wayne, FPGA Based System Design, Pearson Edu, 2004.
2. Verilog HDL: A Guide to Digital Design and Synthesis Book by Samir Palnitkar.
3. FPGA prototyping by Verilog examples By Pong P. Chu., Wiley, 2008
4. FPGA tutorial by Xilinx (http://www.xilinx.com/training/fpga-tutorials.htm#ISE)

Course Plan:

The practices are intended to provide hands-on experience on the simple Verilog code writing to implement on fpga. Then the real life examples will be taken and will be implemented. Then some interface examples will be experimented. Finally, some complex problem will be taken and will be worked by students in project mode.

PTO.

List of Experiments

Introduction to FPGA based system design
Introduction to Verilog, Modelling Styles (Lecture)
Basics of Verilog HDL (Lecture)
Simple Programs in Verilog (Exercise)
Demonstration of Design, Synthesis and Implementation of digital block on FPGA (Demo + Exercise)
Deign of Combinational Circuits on FPGA (Demo + Exercise)
Deign of Counter on FPGA (Demo + Exercise)
Deign of Shift Resgister/ LFSR on FPGA (Demo + Exercise)
FSM Design using Verilog (Lecture + Exercise)
VIO (Virtual Input/output) IP for Debugging (Lecture + Demo)
Implementation of ALU using VIO (Exercise)
Integrated Logic Analyzer IP (Demo)
System Generator (Demo)
Projects and Assignments

Evaluation Scheme:

Evaluation Component	Weightage (%)	Date & Time	Nature of Component
Laboratory Practical Regular class work	30%	Regular Lab and Performance	Open Book
Project/Assignments	20%	To be announced	Open Book
Lab Quiz	10%	To be announced	To be announced
Lab Exam	40%	To be announced	To be announced

Chamber Consultation Hour: Chamber consultation hours of Instructors will be announced separately.

Notices: All notices of this course will be displayed in CMS/ Google Classroom

Make-up Policy: Make-up will be given on **genuine** grounds only. Prior application should be made for seeking the make- up examination.

INSTRUCTOR-IN-CHARGE