Birla Institute of Technology & Science, Pilani
Hyderabad Campus

FIRST SEMESTER 2022-2023

Course Handout Part II

Date: 29-08-2022

In addition to part-I (General Handout for all courses appended to the time table) this portion gives further specific details regarding the course.

Course No.	:	EEE F348
Course Title	:	FPGA Based System Design Laboratory
Instructor-in-Charge	:	Dr. Subhendu Kumar Sahoo
Instructor	:	Amit Kumar Panda, Soumi Saha, Himanshi Awasthi

Scope and Objective of the Course:

HDL (hardware description language) and FPGA (field-programmable gate array) devices allow designers to quickly develop and simulate a sophisticated digital circuit, realize it on a prototyping device, and verify operation of the physical implementation. It combines together the flexibility of a microprocessor and high performance of an Application Specific Integrated Circuit (ASIC). The ease of programming and debugging with FPGAs, as compared to ASICs, decreases the overall non-recurring-engineering (NRE) costs and time-to-market of FPGA-based products. In this lab-oriented course, students will develop their skills by working on more challenging digital system design using Verilog hardware description language (HDL) in an industry-standard design environment. Students will also implement real-world designs in field programmable gate arrays (FPGAs) as well as test and optimize the FPGA-implemented systems.

Textbooks :

1. FPGA prototyping by Verilog examples By Pong P. Chu., Wiley, 2008
2. FPGA tutorial by Xilinx (http://www.xilinx.com/training/fpga-tutorials.htm#ISE)
3. Wolf Wayne, FPGA Based System Design, Pearson Edu, 2004.
4. Verilog HDL: A Guide to Digital Design and Synthesis Book by Samir Palnitkar

Course Plan:

The practices are intended to provide hands-on experience on the simple Verilog code writing to implement on fpga. Then the real life examples will be taken and will be implemented. Then some interface examples will be experimented. Finally, some complex problem will be taken and will be worked by students in project mode.

PTO.

List of Experiments

LAB 1: Verilog modeling style and synthesis results
LAB 2: Implementation of simple combinational design in Xilinx ZED Board
LAB 3: Design of A Counter Using the On Board Clock
LAB 4: Design and implement a traffic light control circuit
LAB 5 & 6 (Assignment -1): Design and implement a Parking lot occupancy counter
LAB 7 : Using IP Integrator
LAB 8: FPGA System design Using IPI
LAB 9 : Hardware Debugging using VIO
LAB 10 :Design of an alu and hardware debugging using VIO
LAB 11: Integrated logic analyzer (ILA) core for hardware debugging
LAB 12: Creating a MAC Using the Xilinx System Generator and Implementation on Hardware
LAB 13 : FIR Filter design Using the Xilinx System Generator and writing verilog code – Analysis of resourse utilization.
LAB 14: Black Box Using the Xilinx System Generator: Importing a Verilog Module
LAB 15: Designing FIR filter using theVivado System Generator's FIR and FDATool blocks
LAB 16 :To Implement the image processing algorithms using FPGA.
Final Project

Evaluation Scheme:

Component	Duration	Weightage (%)	Date & Time	Nature of Component
Laboratory Practical Regular class work	4 hours/ week	35%	Regular lab Performance	Open book
Project/Assignment		20%	Will be announced	Open book
Lab Quiz		20%	Will be announced	Closed book
Lab Exam		25%	Will be announced	To be announced

Chamber Consultation Hour: Chamber consultation hours of Instructors will be announced separately.

Notices: All notices of this course will be displayed in CMS

Make-up Policy: Only One Lab Make-up will be granted for genuine reason with prior-permission from Instructor-in-charge.
Academic Honesty and Integrity Policy: Academic honesty and integrity are to be maintained by all the students throughout the semester and no type of academic dishonesty is acceptable.

INSTRUCTOR-IN-CHARGE