BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI - HYDERABAD CAMPUS
ACADEMIC-GRADUATE STUDIES AND RESEARCH DIVISION
FIRST SEMESTER 2022-2023
COURSE HANDOUT (PART-II)

Date: 27/07 /2023

In addition to Part I (General Handout for all courses appended to the timetable) this portion gives further specific details regarding the course.

Course No : EEE G626
Course Title : Hardware and Software Co-design
Instructor-in-charge : Dr. Amit Kumar Panda

1. Scope and Objective:

FPGA and ASIC based design, Low-Power Techniques in RT Embedded Systems On-chip networking. Hardware Software partitioning and scheduling, Co-simulation, synthesis and verifications, Architecture mapping, HW-SW Interfaces and Re-configurable computing.

This course deals with the system-level design of embedded systems comprised of both hardware and software; investigate topics ranging from system modeling to hardware-software implementation; explore analysis and optimization processes in support of algorithmic and architectural design decisions; and gain design experience with case studies using contemporary high-level methods and tools. The course emphasizes a top-down design methodology driven by bottom-up constraints. The topics covered will include Co-design of hardware and software. Concurrency, real-time control, hardware/software interfaces, and error handling.

2. Text Book:

(T1) Daniel D Gajski, Frank Vahid, Sanjay Narayan, Jie Gong,*Specification and Design of Embedded Systems*, Prentice Hall, 1994.
(T2) Jorgen Staunstrup, Wayne Wolf,*Hardware / Software Co-Design: Principles and Practice*, Kluwer Academic, 1997
(T3) Patrick R. Schaumont, A Practical Introduction to Hardware/Software Codesign, Springer, 2010

3. Reference Books:

1. G. DeMicheli, R. Ernst and W. Wolf, Readings in Hw/Sw Co-design, M. Kaufmann, 2002,
2. Ahmed A. Jerraya and Jean Mermet eds.: System Level Synthesis, Kluwer 1999.
3. Hardware/Software Codesign. G. DeMicheli and M. Sami (eds.), NATO ASI Series E, Vol. 310, 1996.
4. Sanjaya Kumar, James H. Aylor, Barry W. Johnson, and Wm. A. Wulf. The Codesign of Embedded Systems. Kluwer, 1995

4. Course Plan:

Lecture No.	Topics to be covered	Reference to T1
01-03	Hardware Software Co-Design Overview: Brief introduction to Embedded System Design and Challenges	T1/T2/T3/ class notes
04-05	Hardware Software Co-Design Overview: Motivation and driving factors of HSCD, Co-design problems	T1/T2/T3/ class notes
06-07	Hw-Sw Co-design Flow, process steps, requirements	T1/T2/T3/ class notes
08	Cross-fertilization Between Hardware and Software Design	T1/T2/T3/ class notes
09	System Design: Specification, Synthesis, Simulation, Estimation	T1/T2/T3/ class notes
10, 11	Introduction to Specification and Model	T1/T2/T3/ class notes
12-21	Different type of Hw-Sw System Models: State-, Activity-, Structure-, Data –Oriented Models and Heterogeneous Models	T1/T2/T3/ class notes
22-24	Architectural Models: Top-Down and Bottom-Up approach, Different types Architectures	T1/T2/T3/ class notes
25-28	Introduction to Specification Languages	T1/T2/T3/ class notes
29-31	System Synthesis: Partitioning and Mapping, HW/SW Co-synthesis and Synthesis Flow	T1/T2/T3/ class notes
33-33	System Partition: Hw/Sw Partition, Partitioning issues, Partitioning approaches: Structural and Functional	T1/T2/T3/ class notes
34-39	Partitioning Metrics, Cost functions, Partitioning algorithm classes Basic partition methods	T1/T2/T3/ class notes
40-42	Design Estimation: Quality metrics, Performance estimation methods, clock cycle estimation	T1/T2/T3/ class notes

5. Evaluation Scheme:

EC No.	Evaluation Component	Type	Duration	Weight	Date
1	Mid Examination	Close Book	90 Min	20% (40 M)	**14/10 4.00 - 5.30PM**
2	Lab Demonstration/ Experiments/ Seminar	Open Book	-	10% (20 M)	To be announced
3	Research Assignment/ Open Challenge / Design Contest	Open Book	-	15% (30 M)	To be announced
4	Quizes	Close Book	20 Min	5% (10 M)	To be announced
5	Live Project (FPGA prototype)	Open Book	-	20% (40 M)	To be announced
6	Comprehensive Exam	Close Book	180 Min	30% (60 M)	21/12 AN

6. Chamber Consultation Hour: To be announced in Class

7.Notices: All notices regarding the course will be put up in CMS and Google Classroom.

8.Make-up Policy: No make-up will be allowed unless the student is hospitalized for serious medical issue.

9.Academic Honesty and Integrity Policy: Academic honesty and integrity are to be maintained by all the students throughout the semester and no type of academic dishonesty is acceptable.

Instructor - in - charge
EEE G626