FIRST SEMESTER 2019-2020
(COURSE HANDOUT PART II)

Date: 01.08.2019

In addition to Part I (General Handout for all courses appended to the timetable) this portion gives further specific details regarding the course.

Course No : CS G553
Course Title : Reconfigurable Computing
Instructors/in-charge : CHETAN KUMAR V

1. Scope and Objective

Reconfigurable (adaptive) computing is a novel yet important research field investigating the capability of hardware to adapt to changing computational requirements such as emerging standards, late design changes, and even to changing processing requirements arising at run-time. Reconfigurable computing thus benefits from a) the programmability of software similar to the Von Neumann computer and b) the speed and efficiency of parallel hardware execution. The purpose of the course reconfigurable computing is to instruct students about the possibilities and rapidly growing interest in adaptive hardware and corresponding design techniques by providing them the necessary knowledge for understanding and designing reconfigurable hardware systems and studying applications benefiting from dynamic hardware reconfiguration.

2. Contents

The course covers the following subjects:

- Reconfigurable computing systems (Fine and coarse grained architectures and technology)
- Design and implementation (Algorithms and steps to implement algorithms to FPGAs)
- Temporal partitioning (Techniques to reconfigure systems over time)
- Temporal placement (Techniques and algorithms to exploit the possibility of partial and dynamic hardware reconfiguration)
- On-line communication (State-of-the-art techniques about how modules can communicate data at run-time)
- Applications (applications benefiting from dynamic hardware reconfiguration and verification using Xilinx System Design tools and Boards).

3. Background

Background for the course is a basic knowledge in the following areas: digital design, optimization algorithms, and computer architecture.

4. Text Book

1. Wolf Wayne, *FPGA Based System Design*, Pearson Edu, 2004.

5. Reference Book

1. Scott Hauck, André DeHon, Reconfigurable Computing - The Theory and Practice of FPGA Based Computation, The Morgan Kaufmann Series in Systems on Silicon, 2007.
2. C Bobda, Introduction to Reconfigurable Computing: Architectures, Algorithms, and Applications, Springer, 2007.
3. R Vaidyanathan, Trahan Jerry, Dynamic Reconfiguration: Architectures and Algorithms, L, Kluwer Academic, 2003.
4. Uwe Meyer-Baese, DSP with FPGAs, Springer-Verlag, 2003.
5. Journal papers and Conference publications (will be uploaded in the course website)

6. Course Plan

Lecture No.	Learning Objectives	Topics to be covered
01, 02	Introduction	Introduction application and comparison • General Purpose Computing • Domain Specific Computing • Application Specific Computing • Reconfigurable Computing
03, 04,05	VLSI Technology	Wires, Registers and RAM • Wires and vias • Gate delay vs. wire delay • Registers and RAM
06, 07	Reconfigurable Computing Hardware	Programmable logic, an overview of • PLA, PAL, SPLD and CPLD
08,09	Hardware Description Languages	Modeling with HDLs • Verilog/VHDL Combinational Network Delay, Power and Energy Optimization
10,11, 12, 13	Reconfigurable Computing Device	FPGA Architecture, FPGA Fabrics Configuration • SRAM Based-FPGAs • Permanently Programmed FPGAs Programmable I/O, Circuit Design of FPGA Fabrics, Architecture of FPGA Fabrics, Case Studies (Xilinx, Altera, Actel etc).
14,15	Reconfigurable Computing Architecture	Fine - Grained and Course - Grained Reconfigurable Architecture, Case Studies.
16, 17,18	Programming Reconfigurable Systems	Logic Design Process • Design • Integration • FPGA Design Flow Implementation Approaches • Run Time Reconfiguration (RTR) • Partial Reconfiguration (PR)
19, 20, 21, 22	Mapping Designs to Reconfigurable Platform	Logic Implementation for FPGAs, Syntax-Directed Translation Logic Synthesis • Two-Level Logic Synthesis • Multi-Level Logic Synthesis LUT-Based Technology Mapping
23, 24, 25, 26, 27, 28	High-Level Synthesis for Reconfigurable Devices (Behavioral Design)	Modeling • DFG, CFG Introduction to Binding, Scheduling and Allocation, Temporal Partitioning Temporal Partitioning Algorithms • ASAP • ALAP
29, 30, 31, 32,33	Temporal Placement and Routing	Offline and Online Temporal Placement Routing Cost, Routing-Conscious Placement
34,	Online	Communication at run-time between modules on the

7. Evaluation Scheme

EC No.	Evaluation Component	Duration (min)	Marks (Weightage %)	Date & Time	Nature of Component
1.	Mid-Sem Exam	90	40 (20%)	1/10, 11:00 - 12.30 PM	Closed Book
3.	Regular Labs+ Assignments+ Project+ Presentations	-----	80 (40%)	To be announced	Open Book
4.	Comprehensive	180	80 (40%)	06/12 AN	Closed Book

8. Lab

This course has lab components using Xilinx Vivado, Xilinx System Generator, and Xilinx partial reconfiguration tools. For better understanding of concepts, this course has a lab oriented project. Final design should be implemented in Xilinx FPGAs.

9. Chamber Consultation Hours

Will be announced in the class

10. Notices

Notices regarding the course will be put up on the course web site

11. Makeup

Make-up will be given on **genuine** grounds only. Prior application should be made for seeking the make- up examination.

Instructor - in - charge
CS G553