BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI - HYDERABAD CAMPUS
FIRSTSEMESTER 2022-2023
COURSE HANDOUT (PART-II)

Date: 15/08 /2022

In addition to Part I (General Handout for all courses appended to the timetable) this portion gives further specific details regarding the course.

Course No : EEE G626
Course Title : Hardware and Software Co-design
Instructor-in-charge : Dr. Amit Kumar Panda

1. Scope and Objective:

FPGA and ASIC based design, Low-Power Techniques in RT Embedded Systems On-chipnetworking. Hardware Software partitioning and scheduling, Co-simulation, synthesis andverifications, Architecture mapping, HW-SW Interfaces and Re-configurable computing.

This course deals with the system-level design of embedded systems comprised of both hardware and software; investigate topics ranging from system modeling to hardware-software implementation; explore analysis and optimization processes in support of algorithmic and architectural design decisions; and gain design experience with case studies using contemporary high-level methods and tools. The course emphasizes a top-down design methodology driven by bottom-up constraints. The topics covered will include Co-design of hardware and software. Concurrency, real-time control, hardware/software interfaces, and error handling.

2. Text Book:

(T1) Daniel D Gajski, Frank Vahid, Sanjay Narayan, JieGong,*Specification and Design of Embedded Systems*, Prentice Hall, 1994.
(T2) Jorgen Staunstrup, Wayne Wolf,*Hardware / Software Co-Design: Principles and Practice*, Kluwer Academic, 1997

3. Reference Books:

1. G. DeMicheli, R. Ernst and W. Wolf, Readings in Hw/Sw Co-design, M. Kaufmann, 2002,
2. Ahmed A. Jerraya and Jean Mermet eds.: System Level Synthesis, Kluwer 1999.
3. Hardware/Software Codesign. G. DeMicheli and M. Sami (eds.), NATO ASI Series E, Vol. 310, 1996.
4. Sanjaya Kumar, James H. Aylor, Barry W. Johnson, and Wm. A. Wulf. The Codesign of Embedded Systems. Kluwer, 1995
5. Proceedings of IEEE.
6. IEEE Transactions.
7. ACM Transactions

4. Course Plan:

Lecture No.	Topics to be covered	Reference to T1
01, 02	Introduction to Embedded System Design and Challenges	T1: Ch 1, class notes
03, 04, 05	Introduction to Hardware Software Co-design and motivation	T1: Ch 1, class notes
06, 07	Specification, Model, Architecture and Languages	T1: Ch 2-3, class notes
08, 09,10, 11, 12, 13, 14	Models taxonomy, State-Oriented & Activity Oriented Models, Structure & Data –Oriented Models	T1: Ch 2.1-2.7, class notes
15, 16, 17	Architectural Models	T1: Ch 2.8-2.12 / class notes
18, 19, 20	Introduction to Specification Languages	T1: Ch 3.1-3.4 / class notes
21, 22	System-C	----
23, 24	Specification Example: Telephone Answering Machine	T1: Ch 4 / class notes
25, 26	System Synthesis: Partitioning and Mapping, HW/SW Co-synthesis	T2: Ch 2 / class notes
27, 28	System Partitioning issues, Partitioning approaches: Structural and Functional	T1: Ch 6.1-6.3 / class notes
29, 30, 31, 32, 33	Partitioning Metrics, Partitioning algorithms	T1: Ch 6.4-6.9 / class notes
34, 35, 36, 37	Design Quality Estimation	T1: Ch 7 / class notes
38, 39, 40	Recent Trends	-----

5. Evaluation Scheme:

EC No.	Evaluation Component	Type	Duration	Weight	Date
1	Mid Examination	Close Book	90 Min	20%(40 M)	31/10 3.30 - 5.00PM
2	Regular Lab	Open Book	-	20% (40 M)	Regular
3	Quizes	Close Book	-	10% (20 M)	To be announced
4	Project + Presentations	Open Book	-	20% (40 M)	To be announced
5	Comprehensive Exam	Close Book	180 Min	30% (60 M)	19/12 AN

6. Chamber Consultation Hour: To be announced in Class

Notices: All notices regarding the course will be put up in CMS and Google Classroom.

Make-up Policy: No make-up without prior permission.

Academic Honesty and Integrity Policy: Academic honesty and integrity are to be maintained by all the students throughout the semester and no type of academic dishonesty is acceptable.

Instructor - in - charge
EEE G626