

BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI
FIRST SEMESTER 2022 - 2023
COURSE HANDOUT (PART II)

Date: 19/ 08 / 2022

In addition to Part I (General Handout for all courses appended to the timetable) this portion gives further specific details regarding the course.

Course No : **MEL G624**
Course Title : **Advanced VLSI Architecture**
Instructor-in-charge : Subhendu Kumar Sahoo
Instructors :G Sahith

Course Description : Instruction set design and architecture of programmable DSP architectures; dedicated DSP architectures for filters and FFTs; DSP transformation and their use in DSP architecture design; Application Specific Instruction set Processor; superscalar and VLIW architectures

1. Scope and Objective:

Study of advanced processor architectures and their implementation techniques that leverage data-level parallelism and task level parallelism. This includes study of Vector, SIMD and GPU architectures and implementations; study of architectures and implementations that exploit thread-level parallelism and task level parallelism via multi-processing; study of memory hierarchy design for all the above processors, and application domain specific processor architectures and their implementations.

2. Expected Learning Outcomes:

Gaining understanding of how (beyond instruction-level parallelism) data-level parallelism, thread-level parallelism and task level parallelism can be exploited to architect and implement:

- a. Vector Processors
- b. SIMD processors and Multi-media processors
- c. Graphical Processing Units (GPU) and General Purpose Graphical Processing Units (GPGPU)
- d. Multi-core processors
- e. Domain Specific Instruction Set Processor architectures
- f. Memory hierarchy organization for the above processors

3. Text Book:

T1. *Computer Architecture: A Quantitative Approach*, by J.L. Hennessy & D.A. Patterson, Morgan Kaufmann., 6th, 2019.

4. Reference Books:

- R1. Modern Processor Design: Fundamentals of Superscalar Processors, John Paul Shen & Mikko.H.Lipasti , Tata McGraw Hill,2011.

- R2. DSP Processor Fundamentals, Phil Lapesly , Jeff Bier, Amit Shoham, Edward.A.Lee, Wiley India Edition,2011.
- R3 Journals & Conference Proceedings

4. Course Plan:

| Lect No. | Learning Objective | Topics to be covered | Reference |
|----------|--|--|-------------------------|
| 01-03 | Classification of computers from architectural point of view, Quantitative principles performance measurement. | Fundamentals of Quantitative Design and Analysis | T1- Ch-1 & Appendix-A |
| 04-10 | Memory hierarchy design for high performance. | Memory Hierarchy Design | T1- Ch-2 and Appendix-B |
| 11-13 | Review of pipelining concepts. | Pipeline architectures | T1- Appendix-C |
| 14-15 | Basics of super scalar architecture. | Superscalar Architectures | Ch-3 - Appendix-C |
| 16-17 | Different DSP architectures | Different DSP architectures and their units | Class Notes |
| 18-19 | Basics of VLIW architecture | Introduction to VLIW architectures | Chapter-3 |
| 20-23 | Instruction-level parallelism in high performance processors | Introduction to Parallel Processing, ILP | Chapter-3 |
| 24-30 | Vector architectures and implementations. Multimedia architectures and implementations.. | Data-Level Parallelism in Vector, SIMD | Chapter-4 |
| 31-36 | Graphical Processing Unit Architectures | GPU Architectures | Chapter-4 |
| 37 | Processing of single set of code by several processors. | Multithreading | Chapter-3 |
| 38-39 | Small multicore processors | Small multiprocessors | Ch-5 |
| 40 | Interconnection network to connect multiple processors | Multiprocessor interconnects | Class Notes |
| 41-42 | Large multicore processors | Large multiprocessors | Ch-5 |

The material in the text will be supplemented with papers from Journals. Class Notes will include journal papers, e-material

5. Evaluation Scheme:

| EC No. | Evaluation Component | Duration (min) | Marks (Weightage %) | Date and Time | Nature of Component |
|--------|------------------------------|----------------|---------------------|---------------------|-----------------------|
| 1 | Mid-Semester Exam | 90 Min | 25% | 01/11 3.30 - 5.00PM | Open Book |
| 2 | Assignments, Design Problems | NA | 40% | To be announced | Open Book |
| 3 | Comprehensive Exam | 180 Min | 35% | 21/12 AN | Open Book/Closed Book |

* Details of the assignments will be announced later.

6. Chamber Consultation Hours: *To be Announced*

7. Make-up Policy:

Make Up for any component will be given only in genuine cases. In all cases prior intimation must be given to IC.

9. Notices: Notices regarding the course will be displayed on Google classroom/CMS.

Academic Honesty and Integrity Policy: Academic honesty and integrity are to be maintained by all the students throughout the semester and no type of academic dishonesty is acceptable

Instructor - in - charge