Birla Institute of Technology & Science, Pilani
Hyderabad Campus

INSTRUCTION DIVISION
FIRST SEMESTER 2019 - 2020
Course Handout Part II

09-06-2020

This is a modified hand-out for graduating students enrolled in the course.

Course No.	:	EEE F348
Course Title	:	FPGA Based System Design Laboratory
Instructor-in-Charge	:	Dr. Sayan Kanungo
Instructor	:	

Scope and Objective of the Course:

HDL (hardware description language) and FPGA (field-programmable gate array) devices allow designers to quickly develop and simulate a sophisticated digital circuit, realize it on a prototyping device, and verify operation of the physical implementation. It combines together the flexibility of a microprocessor and high performance of an Application Specific Integrated Circuit (ASIC). The ease of programming and debugging with FPGAs, as compared to ASICs, decreases the overall non-recurring-engineering (NRE) costs and time-to-market of FPGA-based products. In this lab-oriented course, students will develop their skills by working on more challenging digital system design using Verilog hardware description language (HDL) in an industry-standard design environment. Students will also implement real-world designs in field programmable gate arrays (FPGAs) as well as test and optimize the FPGA-implemented systems.

Textbooks :

1. FPGA prototyping by Verilog examples By Pong P. Chu., Wiley, 2008
2. FPGA tutorial by Xilinx (http://www.xilinx.com/training/fpga-tutorials.htm#ISE)
3. Wolf Wayne, FPGA Based System Design, Pearson Edu, 2004.
4. Verilog HDL: A Guide to Digital Design and Synthesis Book by Samir Palnitkar

Course Plan:

The practices are intended to provide hands-on experience on the simple Verilog code writing to implement on fpga. Then the real life examples will be taken and will be implemented. Then some interface examples will be experimented. Finally, some complex problem will be taken and will be worked by students in project mode.

PTO.

List of Experiments

LAB 1: Verilog modeling style and synthesis results
LAB 2: Implementation of simple combinational design in Xilinx ZED Board
LAB 3: Design of A Counter Using the On Board Clock
LAB 4: Design and implemention of FSM
LAB 5 & 6: Assignment -1 using FSM
LAB 7 : Demonstration of IP Integrator
LAB 8: Hardware Debugging using VIO
LAB 9 : Design of an alu and hardware debugging using VIO
LAB 10 : Using ILA (Integrated Logic Analyzer) IP for debugging
LAB 11-12: Creating a MAC Using the Xilinx System Generator and Implementation on Hardware
LAB 13: Designing FIR filter using theVivado System Generator's FIR and FDATool blocks

Final Project

Revised Evaluation Scheme:

Component	Comments	Weightage (%)	Date & Time	Nature of Component
Laboratory Practical Regular class work	Attendance and Asignments (upscaled)	40%	Regular lab Performance	Open Book
Project/Assignment	Evaluation on Proposal (downscaled)	10%	Completed	Open Book
Lab Quiz	First Quiz will be considered (downscaled)	10%	Completed	Closed Book
Lab Exam	Mid-Sem 20M Comprehensive Assignment 60M (upscaled)	40%	Will be announced	To be announced

Chamber Consultation Hour: Chamber consultation hours of Instructors will be announced separately.

Notices: All the study materials required to prepare for the comprehensive is uploded in CMS.

Make-up Policy: Only One Lab Make-up will be granted for genuine reason with prior-permission from Instructor-in-charge.

Dr. Sayan Kanungo

INSTRUCTOR-IN-CHARGE