BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, Pilani
Hyderabad Campus

ACADEMIC-GRADUATE STUDIES AND RESEARCH DIVISION

FIRST SEMESTER 2023-2024
COURSE HANDOUT

Date: 03.08.2023

In addition to part I (General Handout for all courses appended to the Time table) this portion gives further specific details regarding the course.

Course No : MEL G624

Course Title : Advanced VLSI Architectures

Instructor-in- Charge: Prof. Subhendu Kumar Sahoo

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1. Course Description:

The course explores advanced VLSI processor architectures, their implementation strategies (microarchitectures) and associated memory hierarchies and their microarchitectures for high performance system design. It also covers the various techniques utilized to leverage parallelism at hardware, application and compiler levels. Students will gain an understanding of how (beyond instruction-level parallelism) data-level parallelism, thread-level parallelism and task level parallelism can be exploited to architect and implement different processing cores e.g.: Vector Processors, SIMD processors and Multimedia processors, Graphical Processing Units (GPU) and General Purpose Graphical Processing Units (GPGPU), Multi-core processors, Domain Specific Processors and Memory hierarchy organizations for the above processors. The course also explores the emerging research directions in VLSI processor design and system architectures.

2. Scope and Objective:

The objective of the course is to understand and gain an in-depth view of Advanced VLSI Architectures: specifically to study various processor architectures, associated microarchitectures and memory organizations that have evolved to exploit different types of parallelisms to increase processor performance. The scope of the course covers the following in detail:

(a) Study of advanced processor architectures and associated implementation techniques (microarchitectures) and memory organization techniques

(b) This includes study of Vector, SIMD and GPU and Domain Specific architectures and implementations

(c) Study of architectures and implementations that exploit thread-level parallelism and task level parallelism via multi-processing (includes multicore processors)

(d) Study of memory hierarchy design for CPUs, vector processors, GPUs and application domain specific processors

3. Text Book:

a).(T1) Computer Architecture: A Quantitative Approach, by John L. Hennessy and David A. Patterson, Morgan Kaufmann, sixth edition, 2019.

4. Reference Books:

a).(R1) Research articles and reports: Details to be provided in the class

5. Course Plan :

Module	Lect Session	Topics to be covered	Reference to Text	Learning Outcome
1	1-7	Introduction of the course and its positioning in the professional domain. Classification of computers (from application point of view) and their design goals. Classification of computers from an architectural point of view. Review of technology and factors contributing to delay and power consumption in computing / information processing. Speed and power implications of computing / information processing architectures and implementations. Power-delay trade-offs and low power techniques. Reliability, Availability, Dependability issues Performance Metrics of processors/computers **(06 Lectures)**	Chapter-1 (T2)	**Learn**: Classification of processors and computers from application point of view and architecture point of view. Also, speed and power implications of their VLSI implementations
2	8-14	Memory hierarchy design for high performance CPUs. **(06 Lectures)**	2.2(T1), 3.1, 3.2, 3.3(T2), Ref	**Learn:** Complete memory hierarchy
3	15-22	Leveraging data-level parallelism: Vector architectures and implementations; Multimedia architectures and implementations. **(08 Lectures)**	2.1, 2.3(T1);3.4(T2), Ref	**Learn :** DLP & vector architectures
4	23-31	Graphical Processing Unit (GPU) and General Purpose GPU Architectures **(08 Lectures)**	2.4; 2.6; 2.10 (T1), Chapter 4 (T2), Chapter 5 (R1), Ref	**Learn:** GPUs
5	32-39	Thread-level Parallelism and Multiprocessors: centralized Shared memory architecture; distributed shared-memory architecture; coherence, consistency and synchronization issues and protocols. **(08 Lectures**)	4.6;4,7(T1) Chapter 6 (T2), Ref	**Learn:** TLP & multicores
6	40-44	Dedicated hardware architectures and their FPGA implementations. Application / Domain Specific Processor design and implementation. Recent (and research) architectures and their implementations for machine learning, machine vision, cognitive computing and real-time big-data analytics. Seminars. **(05 Lectures)**	Chapter 3 (T1), Ref	**Learn:** ASIP, H/W accelerators, Domain specific architectures and research trends

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6. Lab Plan :

SL. No	Assignments	No of Cycles:3 (2hr/cycle)
1	Design Assignment Using Verilog	Continuous
2	ASIC/FPGA implementation	Continuous
3	ASIC/FPGA implementation	Continuous

7. Evaluation Scheme :

SL. No	Component & Nature	Weightage	Duration	Date	Nature
1.	Assignment-1	15 (15%)	Continuous	Weekly	OB
2.	Mid-Semester Exam	30 (30%)	90 min	10/10 4.00 - 5.30PM	CB
3.	Assignment-2 Paper/Report Writing)	15 (15%)	Continuous	As per Time Table	OB
4.	Comprehensive Exam	40 (40%)	180 min	09/12 AN	CB (30%) OB(10%)

Note: Evaluation Scheme will be updated, in case any new institutional guidelines for evaluation are issued during the semester

8. Chamber Consultation Hour: Thursday: 5pm to 6pm (Link will be shared in class). **9.**

Make-up Policy: No make up for Lab & Assignments.

10. Course Notice: Will be displayed on the Nalanda Notice board.

Note: A student who scores less than 20% marks will be awarded NC.

11. Academic Honesty and Integrity Policy: Academic honesty and integrity are to be maintained by all the students throughout the semester and no type of academic dishonesty is acceptable.

Instructor-in-Charge
MEL G 624