BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI,
HYDERABAD CAMPUS
FIRST SEMESTER 2019-20
COURSE HANDOUT (PART-II)

01-08-2019

In addition to Part I (General Handout for all the courses appended to the time table), this portion gives further specific details regarding the course.

Course No.	**CS / EEE / ECE / INSTR F215**
Course Title	**Digital Design**
Instructor-in-charge	**Syed Ershad Ahmed**
Team of Instructors	
Lecture	Syed Ershad Ahmed
Tutorial	Syed Ershad Ahmed, Ponnalagu, , Rajesh Kumar, S K Chatterjee, Saroj Mondal, Ramakant
Practical	Syed Ershad Ahmed, Parikshit Parshuram, Ponnalagu , Rajesh Kumar, Runa Kumari, S K Chatterjee, Saroj Mondal, Souvik Kundu, Surya Shankar
Course Description	This course covers the topics on logic circuits and minimization, Combinational and sequential logic circuits, Programmable Logic devices, State table and state diagrams, Digital ICs, Arithmetic operations and algorithms, Introduction to Computer organization, Algorithmic State Machines
Scope and Objective	The objective of the course is to impart knowledge of the basic tools for the design of digital circuits and to provide methods and procedures suitable for a variety of digital design applications. The course also introduces fundamental concepts of computer organization. The course also provides laboratory practice using MSI devices.

Text Books:

T1: M.Moris Mano and Michael D. Ciletti " Digital Design", PHI, 5th Edition, 2013
T2: G Raghurama, TSB Sudharshan "Introduction to Computer Organization". EDD notes 2007
T3: Laboratory Manual for Digital Electronics and Computer Organization.

Reference Books:

R1: Donald D. Givonne, "Digital Principles and Design" TMH, 2003.
R2: Samir Palnitkar, "Verilog HDL", Prentice Hall; 2 edition, 2003

Course Plan

Lect. No.	Learning Objectives	Topics to be covered	Chapter in the Text Book
1	Introduction to Digital Systems and Characteristics of Digital ICs.	Digital Systems, Digital ICs	1.1, 1.9, 2.3, 10.1 & 10.2
2-3	Boolean algebra and logic gates, Codes number systems	Boolean functions, Canonical forms, number systems and codes	1.2 - 1.7, 2.4-2.9
4 - 5	Simplification of Boolean functions	K-Maps (4,5 variables)	3.1- 3.8
Lab	Simulation and synthesis basics	Hardware Description Language	3.11 (To be discussed in Lab)
6-7	Simplification of Boolean functions	QM Method	3.10
8-10	Combinational Logic, Arithmetic circuits	Adders, Subtractors, Multipliers	4.1 – 4.7
11-12	MSI Components	Comparators, Decoders, Encoders, MUXs, DEMUXs	4.8 - 4.11
Lab	Simulation of Combinational Logic Functions.	HDL for Combinational Logic	4.12 (To be discussed in Lab)
13-15	Sequential Logic	Flip-Flops & Characteristic tables, Latches	5.1 - 5.4
16-18	Clocked Sequential Circuits	Analysis of clocked sequential circuits, state diagram and reduction	5.5, 5.7 & 5.8
19-21	Registers & Counters	Shift registers, Synchronous & Asynchronous counters	6.1 - 6.5
Lab	Simulation of Sequential Logic Functions.	HDL for Sequential Logic	5.6 (To be discussed in Lab)
22-23	Analysis of arithmetic units	Multiplication & Division algorithms	T2: Appendix A & Class Notes
24-27	Modular approach for CPU Design	RTL, HDL description	8.1 & 8.2, 8.4 - 8.8
28-30	Design of Digital Systems	Algorithmic State Machines	R1. Chapter 8
31-33	Design of Asynchronous Circuits.	Asynchronous Sequential Logic	9.1 – 9.4
34-36	Memory and PLDs	RAM, ROM, PLA, PAL	7.2, 7.5 - 7.7
37-39	Memory Organization	Memory Hierarchy & different types of memories	T2: Ch 6 & Class Notes
40-42	Digital Integrated Circuits	TTL, MOS Logic families and their characteristics	10.3, 10.5, 10.7 - 10.10

Evaluation Scheme:

Component	Duration	Weightage (%) and Marks	Date & Time	Nature of Component
Mid Semester Test	1 ½ Hour	25% (75)	1/10, 9.00 -- 10.30 AM	Closed Book
Surprise Quizzes	----	15% (45)		Open Book
LAB Component	Day to Day Evaluation	10% (30)		Demo/Practicals/ (Open Book)
	LAB Exam	10% (30)		Closed Book
Comprehensive Exam	3 Hours	40% (120)	6/12 FN	Closed Book
TOTAL		100% (300)		

General Instructions for Lab:

1. There will be an observation book of 100 pages (white)
2. After every lab, observation book must be signed by Faculty/Research Scholar
3. Lab carries 20% weightage.
   (i) 10% Day to Day evaluation (including attendance) and
   (ii) 10% Final Lab Examination
4. Only one makeup will be allowed

Make-up Policy: There will no make-ups unless for genuine reasons. Prior Permission of the Instructor-in-Charge is required to take a make-up for any component.

Chamber Consultation Hour: To be announced in class.

Notices: All notices shall be displayed only on the **EEE/ECE Notice Board / CMS.**

Academic Honesty and Integrity Policy: Academic honesty and integrity are to be maintained by all the students throughout the semester and no type of academic dishonesty is acceptable.

Syed Ershad Ahmed
Instructor-in-charge
(CS/EEE/ECE/INSTR F215)