

**SECOND SEMESTER 2019-2020**Course Handout Part II

Date: Tue 07 Jan 2020

In addition to part-I (General Handout for all courses appended to the time table) this portion gives further specific details regarding the course.

Course No. : MEL G623

Course Title : ADVANCED VLSI DESIGN *Instructor-in-Charge* :

Surya Shankar Dan

**Prerequisites of the Course:**

- Physics and Modeling of Microelectronic Devices (MEL G631) or equivalent
- VLSI Design (MEL G621) or equivalent

**Scope and Objective of the Course:**

The field of digital VLSI circuits has gone through dramatic evolution and changes. With minimum feature size approaching sub 10 nm, the complexity of the designs and interconnection parasitics has increased dramatically. This has led to new design methodologies and implementation strategies. This course builds on previous courses “VLSI Design” (MEL G621) and “Physics and Modeling of Microelectronic Devices” (MEL G631). It is intended to give a detailed knowledge and experience in design of advanced VLSI circuits at the deep sub- $\mu$  technology nodes in today's and future nano-scale CMOS and Advanced CMOS technologies. Major VLSI design challenges for low-power will be studied in details, followed by careful treatment of several versatile digital, and mixed analog-digital circuit building blocks frequently utilized in VLSI chips. The deep sub- $\mu$  devices behave differently, and bring to the forefront a number of issues that influence reliability, cost, performance, and power dissipation of the digital IC. With communication systems getting more and more complex, there is an ever increasing need for a VLSI designer to understand these issues and new design methods.

**Objective of the Course:**

- Understand deep submicron device engineering
- Understand the power/timing issues, I/O circuit design, clock signal generation/distribution for synchronous and asynchronous VLSI systems
- Understand modeling of wires for delay estimation in deep submicron designs.
- Understanding of high speed computer arithmetic algorithms

**Textbooks:**

1. Kaushik Roy & Sharat C. Prasad, “Low-Power CMOS VLSI Circuit Design”, Wiley
2. Yuan Taur & Tak H. Ning, “Fundamentals of Modern VLSI Devices”, Cambridge University Press

**Reference books/articles:**

1. Publications available online.
2. Jan Rabaey, Anant Chandrakasan & Nikolic, “Digital Integrated Circuits: A Design Perspective”
3. Kang & Leblebici, “”
4. Ken Martin, “”

#	Topics	Page #
1	Long-channel MOSFETs	T2: 113
2	Subthreshold behavior	T2: 125
3	Basic CMOS circuit elements	T2: 224
4	Parasitic elements	T2: 240
5	Sensitivity of CMOS delay to device parameters	T2: 257
6	Performance factors of advanced CMOS devices	T2: 280
7	Physics of power dissipation in MOSFETs	T1: 8
8	Power dissipation in CMOS	T1: 29
9	Low-power VLSI design: Limits	T1: 38
10	Modeling of signals	T1: 56
11	Signal probability calculation	T1: 58
12	Probabilistic techniques for signal activity estimation	T1: 61
13	Statistical techniques	T1: 82
14	Estimation of glitching power	T1: 92
15	Sensitivity analysis	T1: 99
16	Power estimation using input vector compaction	T1: 108
17	Power dissipation in domino CMOS logic	T1: 110
18	Circuit reliability	T1: 113
19	Power estimation at the circuit level	T1: 116
20	High-level power estimation	T1: 119
21	Information-theory based approaches	T1: 122
22	Estimation of maximum power	T1: 125
23	Low-power circuit design style: Clock gated circuits	T1: 203
24	Short-channel MOSFETs	T2: 139
25	MOSFET scaling	T2: 164
26	Threshold voltage	T2: 173
27	MOSFET channel length	T2: 202
28	Leakage currents in deep sub- $\mu$ MOSFETs	T1: 215
29	Deep sub- $\mu$ device design issues	T1: 222
30	Key to minimizing SCE	T1: 224
31	Low-voltage circuit design techniques	T1: 226
32	Testing deep sub- $\mu$ ICs with elevated intrinsic leakage	T1: 240
33	Multiple supply voltage circuit designs: Multi $V_{DD}$ circuits	T1: 245

**Course Plan:**

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35	MOS static RAM memory cell	T1: 255
36	Banked organization of SRAMs	T1: 259
37	Reducing voltage swings on bit-lines	T1: 260
38	Reducing power in the write driver circuits	T1: 263
39	Reducing power in sense amplifier circuits	T1: 265
40	Method of achieving low core voltages from a single supply	T1: 268
41	Energy dissipation in MOSFET channel using an RC model	T1: 273
42	Energy recovery circuit design: Adiabatic circuits	T1: 277
43	Designs with partially reversible logic	T1: 280
44	Supply clock generation	T1: 311
45	Beyond CMOS device technologies	Publications

**Evaluation Scheme:**

# Component	Duration	Marks	Weight-age	Date & time	Evaluation
1 Project 1	To be decided	30	15 %	To be decided	Open
2 *Quiz	45 min	20	10 %	To be decided	Closed
3 Project 2	To be decided	30	15 %	To be decided	Open
4 Mid semester	90 min	40	20%	3/3 , 11:00- 12:30 p.m	.
6 End semester	180 min	80	40 %	04/05 AN	
Total		200	100 %		

\*Only the best performance among all the quizzes will be considered for final grading.

**Project:** The assignments included in the projects will extensively use cadence® EDA tools, synopsys® TCAD tools and python for scripting.

**Chamber Consultation Hour:** Will be announced in class.

**Notices:** All notices related to the course will be put on the CMS and shared through institute email.

**Make-up Policy:** Make up will be given only on genuine reasons. Applications for make-up should be given in advance and prior permission should be obtained for Scheduled tests.

**Academic Honesty and Integrity Policy:** Academic honesty and integrity are to be maintained by all the students throughout the semester and no type of academic dishonesty is acceptable.

**INSTRUCTOR-IN-CHARGE**