Birla Institute of Technology & Science, Pilani
Hyderabad Campus

FIRST SEMESTER 2022-2023

Course Handout Part II

Date: 29-08-2022

In addition to part-I (General Handout for all courses appended to the time table) this portion gives further specific details regarding the course.

Course No	CS / EEE / ECE / INSTR F215
Course Title	Digital Design
Instructor in charge	Dr. Ponnalagu RN
Instructors for Lectures	Prof. S Gurunarayanan. Dr. Ponnalagu RN, Dr .Joyjit Mukherjee
Tutorial Instructors	Dr. Ponnalagu RN, Dr. Joyjit Mukherjee, Dr. S K Chatterjee, Dr. Rajesh Kumar Tripathy
Practical Instructors	Prof. Prabhakar Rao, Prof. Sanket Goel, Dr. Syed Ershad Ahmed, Dr. Harish Vijay Dixit, Dr. Ponnalagu RN, Dr. Sayan Kanungo, Dr. Subhradeep Pal, Dr. Joyjit Mukherjee, Dr. Sandeep Kumar, Dr. Balasubramaniam

Scope and Objective of the Course:

The objective of the course is to impart knowledge to students on the basic concepts of digital logic and the tools, methods and procedures used for designing digital logic circuits for various applications. The course also provides laboratory practice using simulation tools, digital ICs and trainer kits to simulate and implement various operations of digital electronics.

Textbooks:

T1: M. Moris Mano and Michael D. Ciletti "Digital Design", Pearson, 5th Edition, 2013.

T2: G. Raghurama, S. Gurunarayanan, S. Mohan, Karthik, "Laboratory Manual",

Reference books

R1. Neal S. Widmer, Gregory L. Moss & Ronald J. Tocci, "Digital Systems Principles and Applications" Pearson, 12th Edition, 2018.

R2. Charles H. Roth, Jr. and Larry L. Kinney "Fundamentals of Logic Design" Cengage Learning 7th Edition, 2013.

R3: Donald D. Givonne, "Digital Principles and Design" TMH, 2003

Course Plan:

Lecture No.	Learning objectives	Topics to be covered	Chapter in the Text Book
1	Introduction to Digital Systems and Characteristics of	Course Overview. Advantages and disadvantages of digital systems, Evolution of Digital technology terminologies used in digital systems.	**T1**:2.9 **T1**:1.2-1.9

	Digital ICs.		
2	Number system & Codes	Addition and subtraction of binary numbers, octal and hexadecimal numbers, binary codes	**T1**:1.2-1.9
3-4	Boolean algebra and logic gates	Boolean functions, canonical forms, logic gates.	**T1**: 2.1-2.8
5-6	Simplification of Boolean functions	K-Maps (3,4,5 variables)	**T1**: 3.1- 3.8
7	Simplification of Boolean functions	QM Method	**T1:** 3.10
8	Simulation and synthesis	Hardware Description Language (Verilog HDL)	
9	Simplification of Boolean functions	Multi-level and Multi-output Circuits Hazards in Combinational Logic	**R2:** 7.1-7.7 **R2**: 8.4
10-14	Combinational Logic, Arithmetic circuits	Adders, Subtractors, Multipliers, HDL Models of Combinational Circuits.	**T1**: 4.1 – 4.7
15-19	MSI Components	Comparators, Decoders, Encoders, MUXs, DEMUXs	**T1:** 4.8 - 4.11
20-21	Programmable Logic Devices	Read-Only Memory, Programmable Logic Array, Programmable Array Logic	
22-24	Sequential Logic circuits	Latches, Flip-Flops & Characteristic tables,	**T1**: 5.1 - 5.4
25-28	Clocked Sequential Circuits	Analysis of clocked sequential circuits, state diagram and reduction, Design Procedure, HDL Models of Sequential circuits	**T1**: 5.5, 5.7 & 5.8
29-33	Registers & Counters	Shift registers, Synchronous & Asynchronous counters, clock skew & Clock Jitter	**T1**: 6.1 - 6.5
34-35	Memory	Introduction, Random-Access Memory, Memory Decoding	**T1**:7.1 - 7.7
36-38	Design of Digital Systems	Algorithmic State Machines (ASM)	**T1:** 8.4
39-40	Digital Integrated Circuits	RTL, DTL, TTL, ECL & CMOS Gates, Implementation of Simple CMOS circuits	**T1**:10.1 -10.7

List of Lab Experiments

1. Introduction: Familiarization of Simulation Tools and Trainer Kits
2. Boolean function realization
3. Parity Generator and Code Converters
4. Half adder, Full adder and 4-bit Adder
5. BCD Adder
6. Decoders, Multiplexers and Demultiplexers
7. Latches and Flip-Flops
8. Shift registers
9. Counters
10. Arithmetic Logic Unit (ALU)

Evaluation Scheme:

Component	Duration	Weightage (%)	Marks allotted	Date & Time	Nature of Component
Quizzes *	-	10%	30	To be announced	Closed book
Mid Semester Examination	90 Minutes	30%	90	04/11 1.30 - 3.00PM	Closed Book
Regular Lab	During Lab hours	10%	30	Regular Lab classes	Open Book
Final Lab Examination	-	10%	30	To be announced	Open Book
Comprehensive Exam	180 minutes	40%	120	28/12 FN	15%Closed book, 25% Open book
Total		100%	300		

***Quizzes will be conducted in the tutorial sessions**

Chamber Consultation Hour: To be announced in the class

Notices: All notices concerning the course will be displayed in the CMS

Make-up Policy:
1.No make-up will be given for the quiz and laboratory exam evaluation components.
2.For the mid-semester and end-semester examinations, make-up will be given **only for genuine reasons** and in such cases **prior permission from the instructor in charge** need to be obtained.
3. Make-up for the regular laboratory classes will be allowed only for genuine reasons and in such cases prior permission from the respective lab section instructor need to be obtained.

Academic Honesty and Integrity Policy: Academic honesty and integrity need to be maintained by all the students throughout the semester and no type of academic dishonesty is acceptable.

R. N. Ponnalagu

INSTRUCTOR-IN-CHARGE