Birla Institute of Technology & Science, Pilani
Hyderabad Campus

ACADEMIC-GRADUATE STUDIES AND RESEARCH DIVISION
FIRST SEMESTER 2023-2024
Course Handout

Date: 04-08-2023

In addition to part-I (General Handout for all courses appended to the time table) this portion gives further specific details regarding the course.

Course No.	: MEL G626
Course Title	: VLSI Test & Testability
Unit	: 5 (3 0 5)
Instructor-in-Charge	: Syed Ershad Ahmed, Srinivasa R

Course Description : Fault models and types; automated test generation for combinational logic; test generation for sequential logic; need for adding testability logic; design for testability; Adhoc DFT methods; structured DFT; test generation for delay fault; issues in analog circuit testing and testability

Scope and Objective of the Course:

The course describes the theoretical and practical aspects of VLSI Testing and verification. Starting from the basic concepts of verification and testing to advance processor level verification and testing are going to discuss in this course. In addition to that, SoC testing strategy will also be discussed in this course.

The objective of this course is to deal with the study of VLSI design flow, Functional verification, verification flow, simulator architecture and operation, assertions, need for electronic testing, fault modeling, test generation for combinational circuits, test generation for sequential circuits, fault simulation, Built-In Self-Test (BIST), Memory testing, Design for Testability (DFT), SoC test, fault diagnosis, and Analog/RF test.

Textbooks:

1. William K. Lam, Hardware Design Verification: Simulation and Formal Method-Based Approaches- Prentice Hall (2008).
2. Michael. L. Bushnell, and Vishwani. D. Agrawal, Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits, Kluwer Academic Publishers, Third Edition, 2004.

Reference books

1. B. Wile, John C. Goss and W. Rosner, Comprehensive Functional Verification" Morgan Kaufmann, 2005
2. Chris Spear, "System Verilog for Verification," Springer Publications, second edition 2008.
3. Stuart Sutherland, Simon Davidmann, Peter Flake "System Verilog for Design," Springer Publications, second edition 2006.
4. M Abromovici, M A Breuer & A. D. Friedman "Digital Systems Testing and Testable Design ", Jaico Publications, Paperback Impression, 2001.
5. H. Fujiwara, "Logic Testing and Design for testability" MIT Press, 1985.

6. PallabDasgupta, “A roadmap for formal property verification” Springer (2006)

Course Plan:

Lecture No.	Learning objectives	Topics to be covered	Chapter in the Text Book
1 – 2	An Intoduction to Design Verification	VLSI Design flow, Verification principle, and verification methodology	T1 – Ch. 1
3 – 6	Simulator Architectures and operation	The compilers, simulators, simulator taxonomy, operations and applications.	T1 – Ch. 2
7 - 9	Test Scenarios and Coverage	Hierarchical verification, Test plan, and Verification coverage	T1 – Ch. 5
10 – 12	Assertions	Basic temporal operator, logics for temporal specification, system Verilog assertions	T1 – Ch. 5, R6 – Ch. 2,3
13 – 15	Symbolic Representation of Logic and State Spaces	Binary decision diagram (BDD), decision diagram variants, decision diagram-based equivalence checking	T1 – Ch. 8
16 – 17	Formal property verification	Property checking, CTL model checking	T1 – Ch. 9
18 – 19	VLSI Fault Modeling	Defects, errors and faults; structural testing and stuck-at faults	T2 – Ch. 4
20 – 22	Combinational circuit test generation	Test generation algorithms: D, PODEM	T2 – Ch. 7
23 – 25	Sequential circuit test generation	Time-Frame Expansion Method, sequential circuit ATPG	T2 – Ch. 8
26 – 28	Memory Test	Memory fault modeling and testing	T2 – Ch. 9
29 – 31	Delay and IDDQ Test	Delay Test Methodologies, IDDQ testing Methods	T2 – Ch. 12,13
32 – 34	Digital DFT and SCAN design	Scan Design, partial-scan design	T2 – Ch. 14
35 – 37	Built-in-self-test	BITS process, pattern generation, response compaction, etc.	T2 – Ch. 15

38 - 40	Boundary Scan Test	Boundary scan method and standards	T2 – Ch. 16

Evaluation Scheme:

Component	Duration	Weightage (%)	Marks (200)	Date & Time	Nature of Component
Mid-Sem	90 min	20	40	11/10 11.30 -1.00PM	Closed Book
Lab experiments	-	10	20	LAB Timings	Open Book
Lab Assignments	-	10	30	To be announced	Open Book
Seminars	-	20	30	To be announced	Open Book
Comprehensive Exam	180 min	40	80	12/12 AN	Closed Book

Chamber Consultation Hour: To be announced in the class.

Notices: CMS

Make-up Policy: Make-up will be given on **genuine** grounds only. Prior application should be made for seeking the make- up examination.

Academic Honesty and Integrity Policy: Academic honesty and integrity are to be maintained by all the students throughout the semester and any mode of academic dishonesty will not be acceptable.

INSTRUCTOR-IN-CHARGE
MEL G626