BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI

II SEMESTER, 2021-2022

Course Handout (Part -11)

Date: 01-01-2022

In addition to Part-I (General Handout for all courses appended to the time table) this portion gives further specific details regarding the course.

Course No.	**:** MEL G642
Course Title	**:** VLSI Architectures
Instructors	**:** S Gurunarayanan (IC)
Lab Instructors	: G Sahith

Description: Overview of CISC processor architectures; Instruction set architecture of CISC processor; hardware flow-charting methods; implementing microprocessor logic from hard-ware flowcharts; RISC instruction set architecture; Pipelined execution of RISC instructions; pipeline execution unit design; control hazards; design of memory hierarchy.

1a. Scope and Objective of the Course:

To familiarize the student with various architectural techniques used in implementing complex logic functions as VLSI chips to achieve various design objective such as high performance, low cost, high throughput, low-power or a combination thereof. Besides the techniques used for creating efficient dedicated hardware architectures for complex digital functions, the course also covers the architectural techniques and design methods used for designing programmable processors.

It covers the philosophy behind CISC instruction set and its implementation as a microprocessor chip through the creation of optimal datapath and a microprogrammed/ hardwired control unit using the flow -chart method.

Next the concept of Reduced Instruction Set Computer (RISC) architecture which implements a streamlined instruction set on a pipelined execution unit to achieve single cycle execution is covered through an example. Concepts of superscalar architectures are also covered briefly.

Design of Application Specific Instruction Set Processors (ASIP) is covered next to illustrate how high performance, low-power and functional flexibility can be simultaneously addressed through them.

1b. Learning Outcomes of the course:

After completion of the course a student would be able to:

- Gain both an overview of scope and an in-depth understanding of the issues and principles involved in the architecting of fixed-function as well as programmable VLSI circuits.
- Architect and design functional blocks – such as arithmetic functions using combinational / sequential architecting techniques and control circuits that find applications in general purpose as well as application-specific processors with context-specific optimum architectures in terms of speed, gate count and power consumption
- Optimally architect the implementation of sequential computational algorithms
- Optimally architect the implementation of a CISC instruction set architecture
- Optimally architect the implementation of a RISC instruction set architecture
- Optimally architect the implementation of an Application Specific Signal Processor

2. Text Books

(1) Computer Organization and Design- The Hardware Software Interface : 4th Edition
Author: John L. Hennessy & David A. Patterson
Publisher: Elsevier- 2009

(2) Microprocessor Logic Design: Flowchart Method
Author: Nick Tredennick
Publisher: Digital Press, 1987.

3. Reference Books

(1) Digital Design and Synthesis with Verilog HDL.
Author: Eli Sternheim, Rajvir Singh, Rajeev Madhavan and Yatin Trivedi Publisher: Automata Publishing Co., San Jose, CA.

(2) Computer Architecture: A Quantitative

approach Author: John L. Hennessy & David A. Patterson

(3) Embedded DSP Processor Design
Author: Dake Liu; Publisher: Elsevier, 2008

4. Course Plan:

S. No.	Topic: Learning Outcomes	Ref to Text	No. of Lectures
1. 1.1 1.2 1.3 1.4 1.5 1.6	Role of Architecture in VLSI design; Importance of architectural exploration Combinatorial Architectures: Direct mapping of algorithms onto hardware Sequential Architectures: Avoiding duplication of hardware through hardware reuse Mapping algorithms on sequential architectures: The RTL description Design of data path: Choice of functional blocks and data transfer paths between functional units Design of control circuit: The Moore and Mealy Finite State Machines Design Examples : Binary multiplication and binary division Pipelined Architectures: Increasing the throughput Design Examples: Pipelined adder and pipelined multiplier units General purpose computing architectures: Mapping of any algorithms on a standard hardware via the use of that standard hardware's instruction set Design of instruction set for general purpose computing and designing of processor hardware for the instruction set	R2	1-5
2.	CISC Architectures:		
2.1	CISC Instruction set architecture philosophy and example	T2	6-7
2.2	CISC Microprocessor architecting:		
2.21	Block-level architecture (for non-pipelined implementation)	T2	8-9
2.22	R.T. - level design & its capture via hardware flow -charts	T2	10-11
2.23	Block-level architecture for a fetch-decode-execute pipelined implementation	T2	12-13
2.24	Techniques for optimization of control unit using hard-ware flow- charting	T2	14-15
2.25	Techniques for optimization of data-path using hardware flow - charting	T2	16-17
2.26	Implementation of Instruction decoder, control sequencer, Bus Controller and exception handling	T2	18-19
3.	RISC Architectures:		
3.1	RISC Instruction - set architecture philosophy and example	T1	20-21
3.2	RISC microprocessor architecting:		
3.21	Micro architecture: Datapath and Control	T1	22-23

3.22	Single cycle Processor: Implementation	T1	24-25
3.23	Multi cycle Processor : Implementation	T1	26-27
3.24	Pipelined Processor: Implementation	T1	28-30
3.25	Data & Control Hazards, Branch Prediction	T1	31-33
3.26	Advanced Concepts in pipelining	T1	34-35
4.	Application Specific Instruction Set Processor (ASIP) architecture: philosophy and examples	R3	36-38
5.	Memory Sub System Design	R2	39-40

5. Assignments/Labs: Assignments will be given to students during the course from time to time. These will include some design assignments to be implemented using VLSI CAD tools, report submission on some latest topics on design issues of different architectures.

6. Evaluation Schedule:

Components	Duration	Weightage	Date	Time	Remarks
Midterm Test	90 min	25	To be announced	TBD	CB
Take Home Assignments		20	To be announced		OB
Labs Assignments		15	To be announced	(TBA)	OB
Comprehensive	120 min	40	14/05/2022	FN	OB/CB

7. Chamber Consultation Hour: Will be announced in the class.

8. Notices: Notices will be put up on the LMS for the course.

Academic Honesty and Integrity Policy: Academic honesty and integrity are to be maintained by all the students throughout the semester and no type of academic dishonesty is acceptable.

Instructor-in-charge