SECOND SEMESTER 2023-24

Course Handout Part II

Date: 01/01/2024

In addition to part-I (General Handout for all courses appended to the time table) this portion gives further specific details regarding the course.

Course No. : MEL G623
Course Title : ADVANCED VLSI DESIGN
Instructor-in-Charge : Surya Shankar Dan

Course Description:
The field of Digital very large-scale integrated circuits has gone through dramatic evolutions and changes. With minimum feature size approaching 60 nm, the complexity of the designs and interconnection parasitics has increased dramatically. This has led to new design methodologies and implementations strategies. This course builds on previous course MEL G621 VLSI DESIGN. It is intended to give a detailed knowledge and experience in design of advanced VLSI circuits and chips in today's and future nano-scale CMOS technologies. Major VLSI design challenges will be studied, followed by careful treatment of several versatile digital, and mixed analog-digital circuit building blocks frequently utilized in VLSI chips The deep submicron devices behave differently, and bring to the forefront a number of issues that influence reliability, cost, performance, and power dissipation of the digital IC. With communication systems getting more and more complex, there is an ever-increasing need for a VLSI designer to understand these issues and new design methods

Prerequisites of the Course:
- Physics and Modeling of Microelectronic Devices (MEL G631) or equivalent
- VLSI Design (MEL G621) or equivalent

Scope and Objective of the Course:
- Understand deep submicron device engineering
- Understand the power/timing issues, I/O circuit design , clock signal generation/ distribution for synchronous and asynchronous VLSI systems
- Understand modeling of wires for delay estimation in deep submicron designs.
- Understanding of high speed computer arithmetic algorithms

Reference books:
1. IEEE journals
2. William J Dally, John W Poulton, " Digital Systems Engineering"; Cambridge University Press
3. A. Bellaour, M. Elmasry, “Low power digital VLSI design-circuits and systems” , Second Edition, Kluwer academic publishers,
4. R. Best, “Phase Locked Loop”,McGraw Hill Publishers.
5. S. S. Rofail, K. S. Yeo, “Low voltage, Low power Digital BiCMOS Circuits”, Prentice Hall Inc.
6. K. Roy, S.C. Prasad, “Low Power CMOS VLSI Circuit Design”, Wiley Interscience Publication.
7. M. J. S. Smith, “Application Specific Integrated Circuits”, Pearson Education (Singapore) Pte Ltd.
8. Bhaskhar Jayram, "AVHDL PRIMER", Prentice Hall.
9. IEEE Journals of solid state circuits, VLSI system.
10. Miron Abramovici, Melvin A. Breuer, Arthur D. Friedman, “ Digital Systems testing and testable design,” September 1994, Wiley-IEEE Press
11. Martin. Ken, “Digital Integrated Circuit Design”, Oxford University Press, Inc.
12. Michael. L. Bushnell, and Vishwani. D. Agrawal, “Essentials Of Electronic Testing For Digital, Memory And Mixed Signal VLSI Circuits. Kluwer Academic Publishers, Third Edition, 2004
13. Behrooz Parhami, “Computer Arithmetic-algorithms and Hardware design”, Oxford University Press Inc , 2000
14. Sutherland. I., Harris. David, Sproull. Bob, “ Logical Effort-Designing Fast CMOS Circuits”, Morgan Kaufmann Publishers.
15. Eric Bogatin, " Signal integrity Simplified", Prentice Hall Modern Semiconductor Design Series

Course Plan:

Modules	Lecture	References	Learning Outcomes
General Introduction	1		
Timing issues in synchronous VLSI systems and system timing,	6	Text book (ch. 7) / IEEE journals	Knowledge of System design issues
Clock signals distribution and clock generation (All Digital phase locked loop design assignment)	5	Chapter -10 , Ref-3	Knowledge of Clock distribution networks; Generation of clock using DLL and its design
Asynchronous system design	5	Text book (ch. 10) / IEEE journals	Knowledge of Request acknowledge protocols in design
Input/output circuits design with low power constraint,	5	Ref-2	Interfacing circuits
Wire design principles in nanometerregion, signal integrity	6	Ref-2, 15, , IEEE papers	Knowledge of Driver circuits design techniques, lumped/ transmission line modelling signal integrity etc.
High speed computer arithmetic – algorithms and design, Addition / subtraction -- Parallelprefix computation, Multiplication / shift, Logical effort in circuit design	8	Chapter-11, Ref.-12, Ref. 13, IEEE papers	Knowledge of Techniques for highspeed computation
Deep submicron device engineering,	4	Chapter-I, IEEE papers	Knowledge of mos device at submicron level
Memory design		Chapter-12, IEEE papers	Knowledge of Memory organization and design of memory cells
	40		

Evaluation Scheme:

#	Component	Duration	Marks	Date & time	Evaluation
1	Regular Assignments	weekly	60 (30%)	To be announced	Open
2	Literature survey	1 month	10 (5 %)	To be announced	Open
3	Mid semester	90 min	40 (20%)		Closed
4	Course project	3 months	10 (5 %)	To be announced	Open
5	End semester	180 min	80 (40%)		Closed
	Total		200 (100%)		

Project: The assignments included in the projects will extensively use cadence® EDA tools, synopsys® TCAD tools and python for scripting.

Chamber Consultation Hour: Will be announced in class.

Notices: All notices related to the course will be put on the google classroom.

Make-up Policy: Make up will be given only on genuine reasons. Applications for make-up must be given in advance and prior permission should be obtained for scheduled tests.

Academic Honesty and Integrity Policy: Academic honesty and integrity are to be maintained by all the students throughout the semester and no type of academic dishonesty is acceptable.

INSTRUCTOR-IN-CHARGE
MEL G623