BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI
FIRST SEMESTER 2021- 2022
COURSE HANDOUT (PART II)

Date: 20 / 08 / 2021

In addition to Part I (General Handout for all courses appended to the timetable) this portion gives further specific details regarding the course.

Course No	: **ECE(EEE) F434**
Course Title	: **Digital Signal Processing**
Instructor-in-charge	: S. K. Sahoo
Instructors	: Rajesh Kumar Tripathy, Venkateswaran Rajagopalan, BVVSN Prabhakar Rao, Adepu Vivek, Samit Kumar Ghosh

1. Course Description:

This course deals with the design of analog filters like Butterworth, Chebyshev, Elliptic., digital filter design for both IIR & FIR filters. Different filter structures for the realization of digital filters will be discussed. Finite word length effects and Multirate DSP will be introduced. DSP Processor architecture and implementation of DSP algorithms will be part of the course, which will be emphasized upon.

2. Scope and Objective:

The course aims at enumerating the theoretical and practical aspects of modern signal processing in a digital environment. It also aims at discussing few simple application on processing speech and image data.

3. Text Book:

Digital Signal Processing, Sanjit K Mitra, TMH, Third Ed., 2006.

4. Reference Books:

1. "Digital Signal Processing : Principles, Algorithms and Application", John G Proakis & D G Manolakis, PHI, 1998.
2. "Digital Signal Processing: A Practical Approach, Second Edition", Emmanuel C. Ifeachor and Barrie W. Jervis, Pearson education.
3. "Digital Signal Processing: Fundamentals and Applications", Li Tan, Elsevier.
4. "Digital Signal Processing", Oppenhiem & Schafer, Pearson Education Asia, 2002.
5. TI DSP Processor User Manuals
6. Digital Signal Processors, Architecture, Programming and Applications",B. Venkataramani & M Bhaskar, TMH, 2002.
7. MATLAB Help

5. Course Plan:

Lecture No.	Learning Objectives	Topics to be covered	Chapter in the Text Book
1	Overview of the course	Introduction	-------
2	DSP Architectures	General DSP architectural	Class notes

		aspects	
Lecture No.	**Learning Objectives**	**Topics to be covered**	**Chapter in the Text Book**
3	DSP Architectures	Numeric representation used in DSP	Class notes
4,5	DSP Architectures	Architectural details of a typical DSP processor	R5
6-9	Z- Transform and its application	Basics of Z- transform and its use for analysis of LTI systems	Chapter 6
10,11	Discrete time Fourier transform	CTFT, DTFT, Phase and group delay	Chapter 3
12	Finite length discrete transform	DFT, FFT	Chapter 5
13-16	Analog filter design	Butterworth,Chebyshev, Elliptic & Bessel Filters	Chapter 4
17-18	Analog filter design	Design of HP, BP and BS filters	4.5
19	Sampling	Sampling lowpass & bandpass signals	4.2, 4.3
20-22	Simple digital filters	Different LTI systems as frequency selective device.	7.1-7.4
23, 24	Digital Filter design	IIR filter design: IIT, BLT	9
25	Digital Filters	Linear phase FIR filters	7.3
26-29	Digital Filter design	FIR Filter Design	10
30, 31	Digital filter structures	Realization of IIR filters	8.4-8.8
32, 33	Digital filter structures	Realization of FIR filters	8.3, 8.9
34, 35	Finite Word-Length Effects	IIR & FIR Filters	12
36, 37	Multi rate DSP	Decimators & Interpolators	13.1, 13.2
38	Multi rate DSP	Poly phase decomposition	13.3
39	Multi rate DSP	Arbitrary rate sampling rate conversion	13.5
40	Adaptive Digital Filters	Introduction and Concepts of Adaptive filtering, Wiener Filters	RB2 10.1 – 10.3
41	Applications of DSP	Various applications	Class note/ Chapter 14
42	Applications of DSP	Various applications	Class note/ Chapter 14

6. Take Home assignments will be announced in the class.

7. Evaluation Scheme:

S. No.	Evaluation Component	Duration Min.	Mark/ Weightage	Date. time, venue	Nature of Component
1	Midsemester Exam	90	90marks/ 30%	21/10/2021 11.00 - 12.30PM	Open Book
2	Lab	Regular	60marks/ 20%	Regular/ Will be announced	Open Book
3	Quiz		30marks/ 10%	Will be announced	Closed Book
4	Comprehensive	120	120marks/ 40%	18/12 FN	Open Book

8. Chamber Consultation Hours: To be announced in the class.

9. Make-up Policy:

Make Up for any component will be given only in genuine cases. In all cases prior intimation must be given to IC.

There will be no makeup for Lab test and Quiz component.

10. Notices: Notices regarding the course will be displayed on Google class room/CMS.

11.Academic Honesty and Integrity Policy: Academic honesty and integrity are to be maintained by all the students throughout the semester and no type of academic dishonesty is acceptable.

Instructor - in - charge
ECE F434