Birla Institute of Technology and Science – Pilani Hyderabad Campuses

ACADEMIC-GRADUATE STUDIES AND RESEARCH DIVISION FIRST SEMESTER 2022 - 2023 COURSE HANDOUT (PART II)

Date: 12 / 08 / 2023

In addition to Part I (General Handout for all courses appended to the timetable) this portion gives further specific details regarding the course.

Course No : CS G553

Course Title : Reconfigurable Computing
Instructors/in-charge : Subhendu Kumar Sahoo

1.Course Description: Overview of Programmable Logics. FPGA fabric architectures. Logic Elements and Switch Networks. Design and Synthesis of Combinational and Sequential Elements. Placement and Routing. Pipelining and other Design Methodologies. Fine-grained and Coarse-Grained FPGAs. Static and Dynamic Reconfiguration. Partitioning. Hardware/Software Portioning and Partial Evaluation. Systolic Architectures.

2. Scope and Objective

Reconfigurable (adaptive) computing is a novel yet important research field investigating the capability of hardware to adapt to changing computational requirements such as emerging standards, late design changes, and even to changing processing requirements arising at run-time. Reconfigurable computing thus benefits from a) the programmability of software similar to the Von Neumann computer and b) the speed and efficiency of parallel hardware execution.

The purpose of the course reconfigurable computing is to instruct students about the possibilities and rapidly growing interest in adaptive hardware and corresponding design techniques by providing them the necessary knowledge for understanding and designing reconfigurable hardware systems and studying applications benefiting from dynamic hardware reconfiguration.

3.Contents

The course covers the following subjects:

- Reconfigurable computing systems (Fine and coarse-grained architectures and technology)
- Design and implementation (Algorithms and steps to implement algorithms to FPGAs)
- Temporal partitioning (Techniques to reconfigure systems over time)
- Temporal placement (Techniques and algorithms to exploit the possibility of partial and dynamic hardware reconfiguration)
- On-line communication (State-of-the-art techniques about how modules can communicate data at run-time)
- Applications (applications benefiting from dynamic hardware reconfiguration and verification using Xilinx System Design tools and Boards).

4.Background

Basic knowledge in the following areas: digital design, optimization algorithms, and computer architecture.

5.Textbook

- 1. C Bobda, Introduction to Reconfigurable Computing: Architectures, Algorithms, and Applications, Springer, 2007.
- 2. Wolf Wayne, FPGA Based System Design, Pearson Edu, 2004.

Reference Book

- 1. Scott Hauck, André DeHon, Reconfigurable Computing The Theory and Practice of FPGA Based Computation, The Morgan Kaufmann Series in Systems on Silicon, 2007.
- 2. R Vaidyanathan, Trahan Jerry, Dynamic Reconfiguration: Architectures and Algorithms, L, Kluwer Academic, 2003.
- 3. Uwe Meyer-Baese, DSP with FPGAs, Springer-Verlag, 2003.
- 4. Journal papers and Conference publications (will be uploaded in the course website)Course Plan

6.COURSE PLAN

One	Lecture	Learning Objectives	Topics to be covered			
General Purpose Computing Domain Specific Computing	No.					
Domain Specific Computing	01 - 02	Introduction	Introduction application and comparison			
Application Specific Computing Reconfigurable Computing						
O3 - 04 VLSI Technology Wires, Registers and RAM (self study assignment)						
Wires, Registers and RAM (self study assignment)			Application Specific Computing			
Wires and vias Gate delay vs. wire delay Registers and RAM			11 1 0			
Gate delay vs. wire delay Registers and RAM	03 - 04	VLSI Technology				
Reconfigurable Computing Hardware Programmable logic, an overview of Programmable logic logic study assignment Perlogic Synthsic Programmable logic, an overview of Programmable logic synthation Programmable logic lombiandal logic lombiandal Network Delay, Power and Energy Optimization Programmable logic, an overview of Programmable logic, and overlogic study assignment Programmable logic, an overview of Programmable logic study assignment Programmable logic, and overlogic study logic study assignment Programmable logic, and overlogic study assignment Programmable logic, and and energy Optimization Programmable logic, and and logic programmable logic, and and logic programmable logic, and and logic p			Wires and vias			
Or - 08			Gate delay vs. wire delay			
Computing Hardware P.L., PAL, SPLD and CPLD			Registers and RAM			
Hardware Description Languages and Logic Design	05 - 06	Reconfigurable	Programmable logic, an overview of			
Languages and Logic Design O9 - 12 Reconfigurable Computing Device FPGA Architecture, FPGA Fabrics Configuration SRAM Based-FPGAs Programmable I/O, Circuit Design of FPGA Fabrics, Architecture of FPGA Fabrics, Case Studies (Xilinx, Altera, Microsemi etc). Fine - Grained and Course - Grained Reconfigurable Architecture, Case Studies Logic Design Process Design Integration FPGA Design Flow Implementation Approaches Reconfigurable Platform Reconfigurable Platform Reconfigurable Devices (Behavioral Design) Programmable Devices (Behavioral Design) Programmable Platform Programmable Systems Nulti-Level Logic Synthesis UT-Based Technology Mapping Design D		Computing Hardware	PLA, PAL, SPLD and CPLD			
Design Combinational Network Delay, Power and Energy Optimization	07 - 08	Hardware Description	Modeling with HDLs (self study assignment)			
PGA Architecture, FPGA Fabrics Configuration		Languages and Logic	Verilog/VHDL			
Computing Device SRAM Based-FPGAs Permanently Programmed FPGAs Programmable I/O, Circuit Design of FPGA Fabrics, Architecture of FPGA Fabrics, Case Studies (Xilinx, Altera, Microsemi etc). Fine - Grained and Course - Grained Reconfigurable Architecture, Case Studies. 15 - 17 Programming Reconfigurable Systems Reconfigurable Systems 18 - 21 Mapping Designs to Reconfigurable Platform Reconfigurable Platform Reconfigurable Platform 22 - 27 High-Level Synthesis for Reconfigurable Devices (Behavioral Design) 23 - 30 Temporal Placement and Routing 31 - 33 Online Communication 31 - 35 Reconfiguration Reconfiguration Reconfiguration Reconfiguration Reconfigurable Devices Reconfiguration Routing Reconfiguration Routing Reconfiguration Routing Reconfiguration Reconfigurable Devices Reconfiguration Reconfigurable Devices Reconfiguration Reconfigurable Devices Reconfiguration Reconfigurable Devices Reconfigurable Devices Reconfiguration Reconfigurable Devices Reconfigurable Devic		-	Combinational Network Delay, Power and Energy Optimization			
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38 - 40 Applications and Image Processing, Signal Processing, Pattern Matching, etc		<u> </u>				
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7. Evaluation Scheme

EC No.	Evaluation Component	Duration (min)	Weightage (%)	Date & Time	Nature of Component
1.	MID SEM EXAMINATION	90	25	10/10 11.30 - 1.00PM	Closed Book
2.	Lab Assignment/ Lab test/Project and Viva		10+10+20	Will be announced	Open Book
3.	Comprehensive	180	35	09/12/23 (AN)	Closed Book

8.Lab

This course has lab components using Xilinx Vivado design suite. Final design should be implemented in Xilinx FPGAs.

9. Chamber Consultation Hours

Will be announced in the class

10.Notices

Notices regarding the course will be put up on the course web site (Google classroom)

11.Makeup

Make-up will be given on **genuine** grounds only. Prior application should be made for seeking the make- up examination.

12. Academic Honesty and Integrity Policy: Academic honesty and integrity are to be maintained by all the students throughout the semester and no type of academic dishonesty is acceptable.

Instructor - in - charge CS G553