ACADEMIC-GRADUATE STUDIES AND RESEARCH DIVISION
FIRST SEMESTER 2023-2024
COURSE HANDOUT

Date: 01.08.2023

In addition to part I (General Handout for all courses appended to the Timetable), this portion gives further specific details regarding the course.

Course No : **MEL G621**
Course Title : **VLSI Design**
Instructor-in-Charge : **Dr. S Gurunarayanan**
Lab Instructors : **Aalelai Vendhan**
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1. Course Description:

Fundamental structures of VLSI Systems at the lowest levels of system abstraction, namely those associated with the direct application of VLSI devices to particular problems of interest. The broad topics of coverage include Principles of operations of CMOS transistors, various other topologies used in digital VLSI design, logic implementation strategies and performance characterization of VLSI circuits, Low Power Design, different clocking strategies, symbolic layout systems, CMOS subsystems design; case studies.

2. Scope and Objective:

- The course is designed to familiarize students with different design principles used in the **Design of Digital VLSI Circuits & Systems** using CMOS logic with emphasis on high performance**.**
- VLSI design activity will be understood by *Synthesis and then Analysis* at several successive levels of design abstraction.

3. Text Book:

(T1) Essential of VLSI Circuits and Systems Essential of VLSI Circuits and Systems, Kamaran Esharaghian, Douglas A, Puecknell Sholen Eshraghian Publisher: PHI.2009

(T2) CMOS Digital Integrated Circuit, Analysis and Design, Sung-Mo Kang and Yusuf Leblebici, Publisher: McGraw-Hill Companies, Inc.2003

4. Reference Books:

(R1) Digital Integrated Circuits, A Design Perspective, Jan M Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd edition, Prentice Hall, 2005.

5. Course Plan:

Lect Session	Topics to be covered	Reference to Text	Learning Outcome
1	Introduction to VLSI Design	Chapter-1 (T2)	VLSI Design Methodologies
2	Introduction to MOS Physics	2.2(T1), 3.1, 3.2, 3.3(T2)	Basic Electrical Properties of MOS Device
3	MOS electrical Characteristics	2.1, 2.3(T1);3.4(T2)	Current versus Voltage relationships
4-6	MOS Inverter: Static Characteristics	2.4; 2.6; 2.10 (T1), Chapter 4 (T2), Chapter 5 (R1)	Voltage Transfer Characteristics of CMOS Inverters; Performance measure of CMOS Inverters
7-9	MOS Inverters: Switching characteristics	4.6;4,7(T1) Chapter 6 (T2)	Switching characteristics of CMOS inverters
10-12	CMOS Process Technology , Layout and Design Rules	Chapter 3 (T1)	CMOS Fabrication steps, Stick Diagrams and Layout Design rules
13	Scaling of MOS Devices	Chapter 5 (T1)	Constant Voltage Scaling; Full Scaling; Short channel and narrow channel effects
14-19	Combinational MOS Logic Circuits	6.2-6.4,(T1) Chapter 7(T2);	Basic building blocks for combinational logic design, optimization for speed, method of logical effort, Euler method, Ratioed logic, pseudo-NMOS logic, Pass transistor logic, DCVSL
20	Interconnect Parasitic	4.2-4.10(T1) 6.5-6.7 (T2)	Understanding Interconnect , Capacitances, Resistance, Delay models
21-23	Sequential MOS logic Circuits	6.5-6.6(T1) Chapter 7(R1)	Design of Flip-flops, Latches & registers and their performance metrics
24-27	Dynamic Logic Circuits	6.6 (T1) Chapter 7(R1) Chapter 9 (T2)	Dynamic CMOS Circuit techniques, dynamic latches & registers; NORA logic
28-30	Clocking Strategies	6.6 (T1) Chapter 7(R1) Chapter 9 (T2)	Synchronous circuits design and timing metric
31-34	Design of VLSI Arithmetic Modules	8.4-8.5(T1); Chapter 11(R1)	Adders, Multipliers & Shifter architectures

35-38	Aspects of Memory design	Chapter 9 (T1); Chapter 10(T2)	Design of SRAM, DRAM, decoders, sense amplifiers
39-40	Chip I/O Circuits	Chapter13(T2)	ESD Protection Circuits, Input Output circuits

6. Lab Plan:

SL. No	Topics	No of Cycles (2hr/cycle)
1	Tutorial: Overview of Cadence Virtuoso	1
2	MOS IV Characteristics	1
3	CMOS VTC & Transient Analysis	2
4	Static & Combinational Logic Design	2
5	Dynamic & Sequential Logic Design	2
6	Arithmetic Module Design	2

7. Evaluation Scheme:

SL. No	Component & Nature	Weightage	Duration	Date	Nature
1.	Labs Assignments	50 (25%)	Continuous	Weekly	OB
2.	Mid-Semester Exam	40 (20%)	90 min	12/10 4.00 - 5.30PM	CB
3.	Projects/ (Research Paper/Report Writing)	30 (15%)	10-15 days		OB
4.	Comprehensive Exam	80 (40%)	3 hours	16/12 FN	OB/CB

Chamber Consultation Hour: Friday: 4pm to 5pm

Notices regarding the course will be put up on **CMS only.**

Make-up Policy: Make-up will be given on genuine grounds only. Prior application should be made for seeking the make- up examination**.**

Academic Honesty and Integrity Policy: Academic honesty and integrity are to be maintained by all the students throughout the semester and no type of academic dishonesty is acceptable**.**

Instructor-in-Charge

MEL G 621