

**BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI - HYDERABAD CAMPUS**  
**SECOND SEMESTER 2019-2020**  
**COURSE HANDOUT (PART-II)**

Date: 03/12 /2019

In addition to Part I (General Handout for all courses appended to the timetable) this portion gives further specific details regarding the course.

*Course No* : EEE G626  
*Course Title* : Hardware and Software Co-design  
*Instructor-in-charge* : Soumya J

### **1. Scope and Objective:**

FPGA and ASIC based design, Low-Power Techniques in RT Embedded Systems On-chip networking. Hardware Software partitioning and scheduling, Co-simulation, synthesis and verifications, Architecture mapping, HW-SW Interfaces and Re-configurable computing

This course deals with the system-level design of embedded systems comprised of both hardware and software; investigate topics ranging from system modeling to hardware-software implementation; explore analysis and optimization processes in support of algorithmic and architectural design decisions; and gain design experience with case studies using contemporary high-level methods and tools. The course emphasizes a top-down design methodology driven by bottom-up constraints. The topics covered will include Co-design of hardware and software. Concurrency, real-time control, hardware/software interfaces, and error handling.

### **2. Text Book:**

- (T1) Daniel D Gajski, Frank Vahid, Sanjay Narayan, Jie Gong, *Specification and Design of Embedded Systems*, Prentice Hall, 1994.
- (T2) Jorgen Staunstrup, Wayne Wolf, *Hardware / Software Co-Design: Principles and Practice*, Kluwer Academic, 1997

### **3. Reference Books:**

1. G. DeMicheli, R. Ernst and W. Wolf, Readings in Hw/Sw Co-design, M. Kaufmann, 2002,
2. Ahmed A. Jerraya and Jean Mermet eds.: System Level Synthesis, Kluwer 1999.
3. Hardware/Software Codesign. G. DeMicheli and M. Sami (eds.), NATO ASI Series E, Vol. 310, 1996.
4. Sanjaya Kumar, James H. Aylor, Barry W. Johnson, and Wm. A. Wulf. The Codesign of Embedded Systems. Kluwer, 1995
5. Proceedings of IEEE.
6. IEEE Transactions.
7. ACM Transactions

#### 4. Course Plan:

Lecture No.	Topics to be covered	Reference to T1
01, 02	Introduction to Embedded System Design	T1: Ch 1
03, 04,05	Models taxonomy, State-Oriented & Activity Oriented Models, Structure & Data –Oriented Models	T1: Ch 2.1-2.7
06, 07, 08	Architectural Models	T1: Ch 2.8-2.12
09,10, 11	Introduction to Specification Languages	T1: Ch 3.1-3.4
12, 13,14	System-C	----
15, 16	Specification Example: Telephone Answering Machine	T1: Ch 4
17, 18	System Partitioning issues	T1: Ch 6.1-6.3
19, 20, 21	Partitioning algorithms, Functional partitioning of systems	T1: Ch 6.4-6.9
22, 23, 24	Hardware / Software Co-Synthesis	T2: Ch 2
25, 26, 27	Design Quality Estimation	T1: Ch 7
28, 29, 30	Processors & Architectures for Embedded Systems	T2: Ch 4
31, 32, 33, 34	Compilation Techniques	T2: Ch 5
35, 36, 37	Hardware / Software Co-design Environments	T2: Ch.7
38, 39, 40	Recent Trends	-----

#### 5. Evaluation Scheme:

EC No.	Evaluation Component	Type	Duration	Weight	Date
1	Mid Examination	Closed book	1.5 hours	20%	2/3 9.00 - 10.30AM
2	Lab+Assignments+Project+Presentations	Open Book	-	40%	To be announced
3	Comprehensive Exam	Closed Book	3 hours	40%	01/05 FN

#### 6. Chamber Consultation Hour: To be announced in Class

**Notices:** All notices regarding the course will be put up in CMS.

**Make-up Policy:** No make-up without prior permission.

**Academic Honesty and Integrity Policy:** Academic honesty and integrity are to be maintained by all the students throughout the semester and no type of academic dishonesty is acceptable.

Instructor - in - charge  
EEE G626