BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI
Hyderabad Campus.

II SEMESTER 2019-20

Course Handout (Part **-11)**
Date:06-01-2020

In addition to Part-I (General Handout for all courses appended to the time table) this portion gives further specific details regarding the course.

Course No.	**:**	MEL G642
Course Title	**:**	VLSI Architecture
Instructors	**:**	Syed Ershad Ahmed

Course Description :

Overview of CISC processor architectures; Instruction set architecture of CISC processor; hardware flow-charting methods; implementing microprocessor logic from hard-ware flowcharts; RISC instruction set architecture; Pipelined execution of RISC instructions; pipeline execution unit design; control hazards; design of memory hierarchy.

1. Scope and Objective of the Course :

To familiarize the student with various architectural techniques used in implementing complex logic functions as VLSI chips to achieve various design objective such as high performance, low cost, high throughput, low-power or a combination thereof. Besidesthe techniques used for creating efficient dedicated hardware architectures for complex digital functions, the course also covers the architectural techniques and design methods used for designing programmable processors (CISC, RISC, DSP, ASIP Processors).

It covers the philosophy behind CISC instruction set and its implementation as a microprocessor chip through the creation of optimal datapath and a microprogrammed/ hardwired control unit using the flow -chart method.

Next the concept of Reduced Instruction Set Computer (RISC) architecture which implements a streamlined instruction set on a pipelined execution unit to achieve single cycle execution is covered through an example. Concepts of superscalar architectures are also covered briefly.

Design of Application Specific Instruction Set Processor (ASIP) is covered next to illustrate how high performance, low-power and functional flexibility can be simultaneously addressed through them. Other programmable architecture including programmable DSP processors and GPUs are also discussed at some depth.

2. Learning Outcome:

- Understand various architectural techniques used in implementing complex logic functions.
- Understand different processor architectures
- Understand the principles behind implementation of various processors (CISC, RISC etc).
- Understand basics behind design of Application Specific Instruction Set Processor (ASIP).

3. Text Books

(1) Computer Organization and Design- The Hardware Software Interface : 4th Edition
Author: John L. Hennessy & David A. Patterson
Publisher: Elsevier- 2009

(2) Microprocessor Logic Design: Flowchart Method
Author: Nick Tredenick
Publisher: Digital Press, 1987.

4. Reference Books

(1) Verilog HDL: Guide to digital Design and Sytnthesis.
Author: Samir Palnitkar
Publisher: Indian Pearson Education

(2) Computer Organization and Architecture Designing for Performance, Fourth Edition
Author: William Stallings
Publisher: Prentice-Hall, 1997.

(3) DSP Integrated Circuits
J L.Wanhammar
Publisher: Academic Press, 1999.

(4) VLSI digital signal Processing Systems : design and implementation
Keshab K. Parhi
Publisher: India Wiley 1999

(5) Computer Architecture: A Quantitative approach
Author: John L. Hennessy & David A. Patterson

5. Course Plan:

S. No.	Topic	No. of Lectures
1.	Role of Architecture in VLSI design and an overview of architectural techniques.	1
2.	CISC Architectures:	
2.1	CISC Instruction set architecture philosophy and example	1
2.2	CISC Microprocessor architecting:	
2.21	Block-level architecture (for non-pipelined implementation)	1
2.22	R.T. - level design & its capture via hardware flow -charts	2
2.23	Block-level architecture for a fetch-decode-execute pipelined implementation	1
2.24	Techniques for optimization of control unit using hard-ware flow- charting	1
2.25	Techniques for optimization of data-path using hardware flow -charting	1
2.26	Implementation of Instruction decoder, control sequencer, Bus Controller and exception handling	2
3.	RISC Architectures:	
3.1	RISC Instruction - set architecture philosophy and example	2
3.2	RISC microprocessor architecting:	
3.21	Microarchitecture: Datapath and Control	2
3.22	Single cycle Processor	1
3.23	Multi cycle Processor	1
3.24	Pipelined Processor	2
3.25	Data & Control Hazards, Exception Processing	3
4.	Super scalar Processors	2
5.	Specialized Architectures:	
5.1	Programmable DSP Architecture: philosophy and example	2
5.2	Array Processors and GPU architecture: philosophy and example	2
5.3	Extendable Instruction set computer architecture: philosophy and example	2
6.	Application Specific Instruction Set Processor (ASIP) architecture: philosophy and examples	2
7.	Broad criteria for Architecture selection	2
8.	Future Directions: Research Possibilities and Challenges	1

6. **Asignments:** Assignments will be given to students during the course from time to time. These will include some design assignments to be implemented in the VLSI laboratory, report submission on some latest topics on design issues of different architectures.

7. **Evaluation Schedule:**

Components	Duration	Weightage (%)	Date	Time	Remarks
Mid -Term Test	90 min	20 (40M)	4/3	9.00 -- 10.30 AM	CB
Assignments/Mini Project	Regular	20 (40M)	To be Announced Later		OB
Labs/lab Test	Regular	20 (40M)	To be Announced Later		OB
Comprehensive Exam	3 hrs.	40 (80M)	06/05	AN	CB

8. **Chamber Consultation Hour:** Will be announced in the class.

9. **Notices:** Notices will be put up in CMS Only.

10 **Academic Honesty and Integrity Policy:** Academic honesty and integrity are to be maintained by all the students throughout the semester and no type of academic dishonesty is acceptable.

Instructor-in-charge

Syed Ershad Ahmed