Birla Institute of Technology & Science, Pilani
Hyderabad Campus

SECOND SEMESTER 2021-2022
Course Handout Part II

Date: Jan 03, 2022

In addition to Part-I (General Handout for all courses appended to the timetable) this portion gives further specific details regarding the course.

Course No. : MEL G632
Course Title : Analog IC Design
Instructor-in-charge: Dr. Parikshit Sahatiya

1. COURSE DESCRIPTION:

Basic Analog IC Design Issues, Analog Layouts, MOS Switch-- Charge Injection, Current And Voltage Biasing and Reference Generation Circuits, Common Mode Feedback Circuit, Replica Bias, Design, Analysis and Synthesis of Single Stage Amplifiers, Differential Amplifiers, Operational Amplifiers and Operational Transconductance Amplifier Design, Low Power OPAMP , OPAMP/ OTA design in Subthreshold Operation region, Frequency Compensation, Current Mode Analog Circuit Design, Noise- Analysis and Estimation In Amplifiers, emerging trends.

MEL G632 Analog IC Design **3 2 5**

The course describes both theoretical and practical aspects of Analog integrated circuits. Starting from the basic concepts of MOSFET to major analog building blocks; like operational amplifiers, trans-conductance amplifiers, advanced biasing circuits, switched capacitor circuits including in depth understanding of linear building blocks like differential amplifiers, current mirrors, references, comparators, cascode and buffer amplifiers. The characterization and the performance of the linear integrated circuits will be verified by powerful EDA tools like Cadence withstandard CMOS foundry model files.

2. SCOPE AND OBJECTIVE:

This course deals with the analysis and design of analog CMOS integrated circuits, emphasizing fundamentals and new paradigms that student need to master in today's industry. Analog design is art and science at the same time. It is art because it requires creativity and science because a certain level of methodology requires to carry out a design. The objective of this course is to

develop both a solid foundation and methods of analyzing analog circuits by inspection.

3. TEXT BOOK:

T1: B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, 1st ed., 2001.

4. REFERENCE BOOKS:

R1: Paul R. Gray & Robert G. Meyer. Analysis and Design of Analog Integrated Circuits. Wiley, 4th ed., 2010.
R2: David Johns & Ken Martin, Analog Integrated Circuit Design, John Wiley & Sons
2nd ed., 2012.
R3: Phillip E. Allen &Dogulas R. Holberg, CMOS Analog Circuit Design, Oxford University Press,3rd ed., 2013.
R4: Adel S. Sedra et. al., Microelectronic Circuits: Theory and Applications, Oxford University Press,6th., 2013.
R5: R. Jacob Baker, CMOS: Mixed-Signal Circuit Design, Wiley,2008.

COURSE PLAN

Section	Lecture #	Topic	Brief	Reference
I	1 - 2	Introduction to Analog Design	A brief overview of the course and the role of Analog IC Design.	Lect notes/ Ch. 1, Razavi
II	3- 4	Integrated-Circuit Devices and Modelling	Described both the operation and modelling of semiconductor devices	Lect notes/Ch. 2, Razavi
III	5-6	Analog CMOS Subcircuits	Understand the current sink and source, and current mirrors circuits.	Lect notes/ Allen-Ch4
IV	7-8	Basic Single stage Amplifiers	Varity of single stage amplifiers (CS, CD, CG) with active load will be discussed.	Lect notes/ Ch. 3, Razavi
V	9-10	Frequency response	Briefly discussed an introductory	Lect notes/R2

		of single stage amplifiers	view of the frequency response of electronic circuits.	Ch. 4/ Ch. 6, Razavi
VI	11-14	Negative feedback system and stability	Explore how to model negative feedback systems and how to analyze the negative feedback systems.	Lect notes/R2 Ch. 5/ Ch. 6, Razavi
VII	15-20	CMOS operational amplifier	Learn different amplifier topologies and how to design such a high gain amplifiers.	Ch. 9-10, Razavi/Ch. 6-7, R3
VIII	21-23	CMOS Comparators	Explore different analog comparator topologies	Ch. 8 R3
IX	24-26	Output stages and power amplifiers	Analysis and design of a variety of output-stage amplifiers	Ch. 11, R4
X	27-29	Feedback Topologies	Analysis and design of four basic feedback topologies.	Ch. 10, R4
XI	30-33	Bandgap and current reference circuits	Explore how a voltage and current references can be realized, the absolute value of which is highly accurate.	Ch. 11, Razavi
XII	34-37	Phase-locked loops	The analysis and design of PLLs with particular attention to implementation in VLSI topologies.	Ch. 15, Razavi
XIII	38-41	D-to-A and A- to-D converters	Learn the data converter fundamentals and architectures	Ch. 28-29, R5

5. **EVALUATIONSCHEME:**

Component	Duration (min)	Weightage		Date &Time	Remarks
		%	Marks		
Mid Term	90	25	75	As per Timetable	CB
Quiz		10	30		

					OB
Lab		20	60		OB
Project		15	45		OB
Comprehensive Exam	120	30	90	As per Timetable	CB
Total		**100**	**300**		

6. **CHAMBER CONSULTATION HOUR:** To be announced in the class.

7. **NOTICES:CMS**

8. **Makeup Policy:** Make-up only to those who apply before start of test. Those who apply after the start of test will not be granted any make-up. No make-up for Comprehensive test.

9. **Academic Honesty and Integrity Policy:** Academic honesty and integrity are to be maintained by all the students throughout the semester and no type of academic dishonesty is acceptable.

Instructor-in-charge
MEL G632