

BITS-Pilani, Hyderabad Campus
FIRST SEMESTER 2019-2020
Course Handout Part II

Date: May 15, 2019

In addition to Part-I (General Handout for all courses appended to the timetable) this portion gives further specific details regarding the course.

Course No. : MEL G626
Course Title : VLSI Test & Testability
Instructor-in-charge: Saroj Mondal
Instructors : Saroj Mondal

1. COURSE DESCRIPTION:

MEL G626 VLSI Test & Testability

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The course describes theoretical aspects of VLSI Testing and Verification. Starting from the basic concepts of testing to advance processor level testing are going to discuss in this course.

2. SCOPE AND OBJECTIVE:

The objective of this course is to deal with the study of VLSI design flow, Functional verification, verification flow, need of electronic testing, fault modeling, test generation for combinational circuits, test generation for sequential circuits, fault simulation, Built-In Self-Test (BIST), Memory testing, Design for Testability (DFT), SoC test, fault diagnosis, Analog/RF test.

3. TEXT BOOK:

T1: Michael. L. Bushnell, and Vishwani. D. Agrawal, Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits, Kluwer Academic Publishers, Third Edition, 2004.

T2: B. Wile, John C. Goss and W. Rosner, Comprehensive Functional Verification" Morgan Kaufmann, 2005

4. REFERENCE BOOKS:

R1: William K. Lam, "Hardware Design Verification: Simulation and Formal Method-Based Approaches-Prentice Hall (2008)

R2: Chris Spear, " System Verilog for Verification," Springer Publications, second edition 2008.

R3: Stuart Sutherland, Simon Davidmann, Peter Flake "System Verilog for Design," Springer Publications, second edition 2006.

R4: M Abromovici, M A Breuer & A. D. Friedman "Digital Systems Testing and Testable Design ", Jaico Publications, Paperback Impression, 2001.

R4: H. Fujiwara, "Logic Testing and Design for testability" MIT Press, 1985.

R5: Pallab Dasgupta, "A roadmap for formal property verification" Springer (2006)

COURSE PLAN

S.No.	Topic	Lectures
1	Introduction + VLSI design flow	4
2	Introduction to simulators: How they work or how do you do a simulation	3
3	Functional verification and verification challenges, Simulation-based verification (SBV)	11
4	Formal verification (FV): BDD, Formal Boolean equivalence checking, property checking, Semi-formal verification	5
5	Electronic testing basics [Fault modeling: Stuck-at, bridge, delay, and crosstalk fault, Delay faults, Design for Testability (DFT)]	5
6	Fault Simulation	3
7	Test generation for combinational circuits: ATPG algorithms (Boolean Difference, D-algorithm, PODEM, FAN)	3
8	Testability Measures	1
9	Test generation for sequential circuits: Time frame expansion model	2
10	Built-In Self-Test (BIST), Memory test, Fault diagnosis	2
11	Analog/RF test, Test issues in nano-technology	1
	Total	40

4. Evaluation Scheme :

Component	Duration	Marks	Date & Time	Remarks
Mid Sem. Exam	90 Min	20	03/10 11:00 – 12:30 PM	OB
Assignments / project/ Quiz Seminar	(Continuous)	40	(OB)	
Comp. Exam	3 Hours	40	09/12 AN	CB
		100		

5. Chamber Consultation Hours: To be announced in the class.
6. NOTICES: CMS
7. Makeup Policy: Make-up only to those who apply before start of test.
Those who apply after the start of test will not be granted any make-up. No make-up for Comprehensive test.

Instructor-in-charge
MEL G626