Birla Institute of Technology & Science, Pilani
Hyderabad Campus

COURSE HANDOUT (PART II)

Date: 12/ 08 / 2020

In addition to Part I (General Handout for all courses appended to the timetable) this portion gives further specific details regarding the course.

Course No : **MEL G624**
Course Title : **Advanced VLSI Architecture**
Instructor-in-charge : Chetan Kumar V

Description : Instruction set design and architecture of programmable DSP architectures; dedicated DSP architectures for filters and FFTs; DSP transformation and their use in DSP architecture design; Application Specific Instruction set Processor; superscalar and VLIW architectures

1. Scope and Objective:

The course aims at familiarizing students with advanced parallel processing architectures suitable for high-performance computing. It deals with three levels of parallelism – Instruction-Level, Data Level and Thread Level.

2. Text Book:

T1. *Computer Architecture: A Quantitative Approach,* by J.L. Hennessy & D.A. Patterson, Morgan Kaufmann., 5th Ed, 2012.
T2. Modern Processor Design: Fundamentals of Superscalar Processors, John Paul Shen &Mikko.H.Lipasti , Tata McGraw Hill,2011.
T3. DSP Processor Fundamentals, Phil Lapesly , Jeff Bier, Amit Shoham, Edward.A.Lee, Wiley India Edition,2011.

3. Reference Books:

(R1) Parallel Computer Architecture: A Hardware / Software Approach, David E Culler & Jaswinder Pal Singh., Morgan Kauffmann / Harcourt India, 2002.
(R2) Computer Architecture Pipelined& Parallel Processor Design, M.J.Flynn, Narosa Publishing House, 2006
(R3) Advanced Computer Architecture: A Design Space Approach, Sima, Fountain,Kacsuk, Pearson, 2012.
(R3) Journals & Conference Proceedings

*** It is assumed that students have a working knowledge of MIPS Architecture**

4. Course Plan:

No.	Topics to be covered	Reference
1-3	Fundamentals of Quantitative Design and Analysis	T1- Ch. 1, Class Notes
4-9	Memory Hierarchy Design	T1- Ch. 2, Class Notes

10	Introduction to Parallel Processing, ILP	T1 – Ch. 3
11-12	Pipeline architectures	T1- Ch. 3/T2-Ch. 2, Class Notes
13-19	Student Presentations on Cache Optimizations	Self-Study
20-27	Superscalar Architectures (Dynamic Scheduling)	T1- Ch. 3/T2-Ch. 4, 5, Class Notes
28	Introduction to VLIW architectures	T1- Ch. 3, Class Notes
29	Introduction to Type of Multithreading	T1-Ch. 5, Class Notes
30-31	Instruction level Data parallel Architecture- Introduction	T1-Ch. 4, Class Notes
32-34	Vector Processors	T1-Ch. 4, Class Notes
35-37	SIMD Architectures	T1-Ch. 4, Class Notes
38	Instruction to Thread level Parallelism	T1-Ch. 5, Class Notes
39-40	Shared Memory MIMD Architectures	T1-Ch. 5, Class Notes
41-43	Distributed Memory MIMD Architecture	T1-Ch. 5, Class Notes

The material in the text will be supplemented with papers from Journals. Class Notes will include journal papers, e-material

5. Evaluation Scheme:

EC No.	Evaluation Component	Duration (min)	Marks (Weightage %)	Date and Time	Nature of Component
1	Test 1	30 Min	15%	To be announced	Open Book
2	Test 2	30 Min	15%	To be announced	Open Book
3	Test 3	30 Min	10%	To be announced	Open Book
4	Presentation of Case Studies	NA	10%	To be announced	Open Book
5	Assignments	NA	20%	To be announced	Open Book
6	Comprehensive Exam	120 Min	30%	11/12 FN	Open Book/Closed Book

* Details of the assignments will be announced later.

6. Chamber Consultation Hours:*To be Announced*

7. Make-up Policy:

Make Up for any component will be given only in genuine cases. In all cases prior intimation must be given to IC.

9. Notices: Notices regarding the course will be displayed in CMS.

Academic Honesty and Integrity Policy: Academic honesty and integrity are to be maintained by all the students throughout the semester and any mode of academic dishonesty will not be acceptable.

Instructor - in - charge
MEL G624