BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI HYDERABAD CAMPUS
INSTRUCTION DIVISION
FIRST SEMESTER 2021-2022

Course Handout Part II

In addition to Part I (General Handout for all courses appended to the time table) this portion gives further specific details regarding the course.

Course No. **: MEL G621**
Course Title **: VLSI DESIGN**
Instructor-in-charge **: Syed Ershad Ahmed**
Instructors **: Anil Kumar**
Lab-Instructor **: Anil Kumar**

1. Scope and Objective of the Course:

The objective of this course is to understand different design principles used in the **Design of Digital VLSI Circuits & Systems using nMOS and CMOS** with emphasis on for high performance computing. VLSI design activity will be understood by *Synthesis and then Analysis* at several successive levels of design abstraction.

The broad topics of coverage includes Principles of operations of CMOS transistors used as a digital switch and various other topologies used in Digital VLSI Design, Logic implementation strategies and performance characterization of the VLSI circuits, Low Power Design, different clocking strategies, symbolic layout systems, CMOS subsystems design and Memory modules.

2. Student Learning Outcomes.

- Design digital blocks using CMOS logic through static logic and dynamic logic design approaches.
- Compare different Digital VLSI Design methods using set of Performance metrics.
- Create Layouts of Different functional blocks
- Extraction of Interconnect Parasitic and iterate the design to meet the defined performance metrics.
- Design of Digital subsystem and Memory modules

3. Text Books

(a) Essential of VLSI Circuits and Systems
Author: Kamaran Esharaghian, Dauglas A, Puecknell Sholen Eshraghian Publisher: PHI.2009
(b) CMOS Digital Integrated Circuit, Analysis and Design, Sung-Mo Kang and Yusuf Leblebici, Publisher: McGraw- Hill Companies, Inc.2003

4. Reference Books

(a) Digital Integrated Circuits: A Design Perspective Author: Jan Rabey , Prentice Hall, 2005

5. Course Plan

No of Lect.	Topic To be Covered	Learning Objectives	Ref. to Text Book
1	Introduction	Overview of Digital VLSI Design Methodologies	Chapter-I (T2)
1	Introduction to MOS Physics	Basic Electrical Properties of MOS Devices	2.2(T1), 3.1, 3.2, 3.3(T2)

1	Device Characteristics	Understanding Drain-to-Source Current versus Voltage relationships	2.1, 2.3(T1);3.4(T2)
3	Static NMOS/CMOS inverter: voltage-transfer characteristics	Voltage Transfer Characteristics of CMOS Inverters; Performance measure of CMOS Inverters	2.4; 2.6; 2.10 (T1), Chapter 4 (T2), Chapter 5 (R1)
4	MOS Capacitances, Dynamic Behavior of MOS Inverters	Capacitances associated with CMOS devices and switching characteristics of CMOS inverters	4.6;4,7(T1) Chapter 6 (T2)
2	CMOS Process Technology , Layout and Design Rules	CMOS Fabrication steps, Stick Diagrams and Layout Design rules	Chapter 3 (T1)
1	Scaling of MOS Devices	Constant Voltage Scaling; Full Scaling; Short channel and narrow channel effects	Chapter 5 (T1)
5	Combinational CMOS logic circuit :static logic ; optimization for speed, method of logical effort ; Euler diagrams ; Ratioed logic, pseudo-NMOS logic; Pass transistor logic	Building blocks for combinational logic; Examples of structured logic design; Different Design styles; subsystem design	6.2-6.4,(T1) Chapter 7(T2);
2	InterConnect Parasitics	Understanding Interconnect Capacitances, Resistance, Delay models	4.2-4.10(T1) 6.5-6.7 (T2)
3	CMOS Sequential logic Design:,	Design of Flip-flops; Latches & registers	6.5-6.6(T1) Chapter 7(R1)
4	Dynamic and Domino Logic Design	Dynamic CMOS Circuit techniques; Dynamic latches & Registers; NORA logic, Pipelining Approach.	6.6 (T1) Chapter 7(R1) Chapter 9 (T2)
2	Clocking Strategies	Synchronous design, timing metrics,	11.5(T1); 10.1-10.2(R1)
2	PLDs and FPGA based design	PAL and PLA design, Blocks of FPGAs	Study Material
4	Adder architectures	Adders, Multipliers & Shifter Design	8.4-8.5(T1); Chapter 11(R1)
4	Aspects of Memory design	Design of SRAM, DRAM, decoders, sense amplifiers	Chapter 9 (T1); Chapter 10(T2)
1	Chip I/O Circuits	ESD Protection Circuits, Input Output circuits	Chapter13(T2)

5. Evaluation Schedule

Components	Duration	Weightage (%)	Date	Time	Remarks
Mid -Term Test	90 min	30 (60M)			OB
Assignments/Mini Project	Regular	15 (30M)	To be Announced Later		OB
Labs	Regular	10 (20M)	To be Announced Later		OB
Surprise Quizzes	Regular	10 (20M)	To be Announced Later		OB
Comprehensive Exam	3 hrs.	35 (70M)			OB

6. Chamber consultation hour: Will be announced in the class.

7. Notices: All course related notices will be uploaded in CMS.

(Instructor-in charge)
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