Birla Institute of Technology & Science, Pilani
Hyderabad Campus
Second Semester, 2019-2020
Course Handout (Part-II)

06-01-2020

In addition to Part I (General Handout for all courses appended to the Time Table), this portion gives further specific details regarding the course.

Course No. : **CS/ECE/EEE/INSTR F241**
Course Title : Microprocessor Programming & Interfacing
Instructor-in-charge : M.B. Srinivas
Team of Instructors : Suvadip Batabyal, Karumbaiah Chappanda, Soumya J, S K Sahoo, Runa Kumari, Ramakant, Sandeep Kumar, Prashant Wali, Amit Ranjan Azad

Course Description : 8086 - 80486 Programmers model, processor architecture; Instruction set, modular assembly programming using subroutines, macros etc.; Timing diagrams ; Concept of interrupts: hardware & software interrupts, Interrupt handling techniques, Interrupt controllers; Types of Memory & memory interfacing; Programmable Peripheral devices and I/O Interfacing ; DMA controller and its interfacing: Design of processor based system.

Text Book:

T1: Barry B Brey, The Intel Microprocessors .Pearson, Eight Ed. 2009.

Reference book:

R1: Douglas V Hall, Microprocessor and Interfacing, TMH, Second Edition.

R2. Lyla B Das, The x86 Microprocessors: 8086 to Pentium, Multicores, Atom and the 8051 Microcontroller: Architecture, Programming and Interfacing, Second Edition

R3: 8086 family User Manual, Intel Corporation

Detailed Course Plan:

Lect. No.	Learning Objectives	Topics to be covered	Chapter in the Text Book
1.	Introduction to Microprocessor and Microcomputers	Compute Architecture, Memory & I/O organization, CISC/RISC processors	Chapter 1 (T1), Chapter 1 (R1)
2-3	Microprocessor & its architecture	8086 Microprocessor	Chapter 2 (T1), Chapter 2 (R1)
4-6	Assembly Programming	Addressing Modes	Chapter 3 (T1)
7-12	Assembly Programming	Instruction Set & ALP	Chapter 4-6, 8 (T1)
13-15	8086/8088 Hardware Specifications	Pin Out, Modes of operation, Clocking, Buses	Chapter 9 (T1)

16-19	Memory Interface	Memory Devices, Address Decoding- Memory Interface	Chapter -10 (T1)
20-23	I/O Interfacing	Basic I/O interfacing (I/O mapped I/O and Memory mapped I/O) I/O port address decoding	11.1, 11.2 (T1)
24-26	Interrupts	Types of interrupts, Vector tables, Priority Schemes	12.1, 12.2, (T1)
27-29	Programmable Peripheral Devices	8255,8254,ADC,DAC, 8259	11.3-11.6 & 12.3 -12.6 (T1)
30-31	DMA controller	Basic Operation, 8237, Shared Bus, Disk Memory Systems, Video Displays	Chapter -13 (T1)
32-33	Bus Interface	ISA, PCI, Com, USB,AGP	Chapter 15 (T1)
34-36	Advanced Processors	80186-80286	Chapter 16 (T1), Chapter 15 (R1)
37-39	Advanced Processors	80386-80486	Chapter 17 (T1), Chapter 15 (R1)

Evaluation Scheme:

Component	Duration	Weightage (%) and Marks	Date & Time	Nature of Component
Mid-Sem Test	1 ½ Hour	20% (60)	2/3 1.30 -3.00 PM	Closed Book
Quizzes (2)	----	10% (30)	Will be announced	Closed Book
LAB / Project Components	2hrs/week	10% (30)	Day to Day Evaluation	Practicals/Demo (Open Book)
	Project	30% (90)	Will be announced	Open Book
Comprehensive Exam	3 Hours	30% (90)	02/05 FN	Closed+Open Book
TOTAL		100% (300)		

Make-up Policy: There will no make-ups unless for genuine reasons. Prior Permission of the Instructor-in-Charge is required to take a make-up for any component. A make-up test shall be granted only in genuine cases as per institute guidelines.

NO make-up is allowed for quizzes.

Chamber Consultation Hour: Will be announced in the class.

Notices: Notices concerning to this course will be on **CMS**.

Academic Honesty and Integrity Policy: Academic honesty and integrity are to be maintained by all the students throughout the semester and no academic dishonesty of any kind is acceptable.

M.B. Srinivas
Instructor-in-charge
(CS/EEE/ECE/INSTR F241)