Birla Institute of Technology & Science, Pilani
Hyderabad Campus

Academic – Graduate Studies and Research Division
SECOND SEMESTER 2021-2022
(COURSE HANDOUT PART II)

Date:
17.01.2022

In addition to Part-I (General Handout for all courses appended to the time table) this portion gives further specific details regarding the course.

Course No. : **CS G524**
Course Title : **Advanced Computer Architecture**
Instructor-in-Charge : **Prof. G Geethakumari**

Course Description: Basics of Parallelism, Instruction Level Parallelism, Simultaneous Multi-Threading, Design and Optimization Techniques for Cache and DRAM; Pipelining and Super-scalar Techniques, Multiprocessor and Multi-core architecture, Shared Memory and Cache Coherence Issues; Multi-vector and SIMD computers, Performance evaluation methods, Interconnect Design Techniques.

1. Scope and Objectives of the Course:
The scope of the course includes advanced concepts in SISD environment, designing and using high performance SIMD and MIMD computers, system resources such as memory technology and I/O subsystem performance, case studies on multiprocessor and multicore architectures, Hands-on exposure to multi-core programming and TLP.

The main objective of this course is to give the students exposure to

- Instruction level parallelism
- Data level parallelism and vector processors
- Thread level parallelism
- Performance from memory hierarchy perspective
- Multicore programming

2.Textbooks:
(T1): Computer Architecture: A Quantitative Approach, J.L Hennessy & D.A.Patterson, Morgan Kaufmann, 6th Edition, 2017.

3.Reference books
R1: Computer Organization and Architecture: Designing for Performance, William Stallings, 10th Edition, Pearson, 2016.
R2: Parallel Computer Architecture: A Hardware / Software Approach, David E Culler & Jaswinder Pal Singh., Morgan Kauffmann, 2011.
R3: Advanced Computer Architecture, Kai Hwang, Tata McGraw Hill, 2008.
R4: Computer Architecture & Parallel Processing, Hwang & Briggs, McGraw Hill, 2012.

4.Course Plan:

Lecture No.	Learning Objectives	Topics To be covered	Chapter in the Text Book
1	To understand about the importance of quantitative aspects of computer design	Fundamentals of Quantitative Design and Analysis – Introduction	Ch.1
2-3		Dependability, Quantitative principles of Computer Design	Ch.1
4-5	To learn about ILP, practical challenges of implementing ILP	Instruction Level Parallelism and its exploitation – concepts and challenges	Ch.3, Appendix A, Appendix C
6-7		Basic compiler techniques for exposing ILP, reducing branch costs with advanced branch prediction	Ch.3
8		Overcoming branch hazards with dynamic scheduling	Ch.3
9-11		Dynamic scheduling, examples and algorithm, hardware-based speculation	Ch.3
12-13		Exploiting ILP using Multiple issue and static scheduling, advanced techniques for instruction delivery and speculation	Ch.3, Appendix H(online)
14	To understand data level parallelism, GPUs	Data Level Parallelism -introduction	Ch.4
15-17		Vector Architecture, SIMD Instruction Set Extensions for Multimedia	Ch.4
18-19		Graphics Processing Units, detecting and enhancing loop level parallelism	Ch.4
20-23	To explore and understand TLP	Thread Level Parallelism – centralized shared memory architectures, symmetric shared memory architectures	Ch.5
24-26		Distributed shared memory and directory based coherence, synchronization	Ch.5
27 – 29		Models of memory consistency, multiprocessors and their performance	Ch.5, Appendix I(online)
30	To know about the organization of memory hierarchy and learn various optimization techniques at each level	Memory Hierarchy Design - Introduction	Ch.2, Appendix B
31 – 33		Memory Organization – advanced optimizations of cache performance	Ch.2
34 – 35		Virtual Memory and virtual machines	Ch.2
36-37	To study the performance aspects of storage systems	Storage Systems- Introduction, Reliability, Availability & RAID	Appendix D (online appendix)
38-42	To get an insight into the latest architectures	Introduction to multi-core architectures, code optimization for multi-core	Latest reference material, Recent research publications

5.Evaluation Scheme:

EC No.	Evaluation Component	Duration	Weightage (%)	Date& Time	Nature of Component
1	Mid Sem Test	90 min	35	As announced by Time Table Division	Open Book
2	Lab Tests: online programming (*Evenly spaced*) (2 nos.)		25	TBA	Open Book
3	Comprehensive	120 min	40	As announced by Time Table Division	Closed Book

Note: 40% of the evaluation to be completed by midsem grading.
"For Comprehensive exam and Mid-semester Test, the mode (offline/online) and the duration are subject to changes as decided by the AUGSD/Timetable division in future."

6. Consultation Hour: To be announced in the class

7. Notices: Notices regarding the course will be put up on CMS.

8. **Makeup Policy:** No makeup exam allowed without prior permission.

9. **Academic Honesty and Integrity Policy**: Academic honesty and integrity are to be maintained by all the students throughout the semester and no type of academic dishonesty is acceptable.

INSTRUCTOR-IN-CHARGE
CS G524