BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI HYDERABAD CAMPUS
FIRST SEMESTER 2023-2024

Course Handout Part II

Date: 11/8/2023

In addition to part I (General Handout for all courses appended to the time table) this portion gives further specific details regarding the course.

Course No. **: EEE F313/INSTR F313**
Course Title **: ANALOG AND DIGITAL VLSI DESIGN**
Instructor-in-charge **: Sumit K Chatterjee**

1.Scope and Objective of the Course:

The objective of this course is to provide an introduction to the fundamentals and practical considerations pertaining to the design of integrated circuits. The scope encompasses both theoretical and practical aspects of analog and digital integrated circuits starting from the basic concepts of MOSFET to major analog and digital building blocks; The importance of CAD tools in IC system design process is also acknowledgedand stressed upon accordingly.

2. Course Description:

Moore's Law, Y chart, MOS device models; an overview of fabrication of CMOS circuits. Layout design for CMOS inverter and other logical gates. I-V characteristics of MOS devices, design parasitic capacitances, MOS scaling techniques, latch up. Digital circuit design styles for logic, arithmetic and sequential blocks design; device sizing using logical effort; timing issues (clock skew and jitter). Estimation and minimization of energy consumption; Power delay trade-off. Basic and cascaded NMOS/PMOS/CMOS gain stages, Differential amplifier. CMRR, PSRR and slew rate issues, offset voltage , advanced current mirrors; current and voltage references design, common mode feedback circuits.

3. Text Book :

T1: Jan M. Rabaey; Anantha Chandrakasan; Borivoje Nikoli´c, "Digital Integrated Circuits - A Design Perspective", (Second Edition) Prentice-Hall Electronics and VLSI Series. (2003).

T2: Behzad Razavi,"Design of Analog CMOS integrated circuits", McGraw Hill International Edition. 2001.

4. Prime Reference Books

R1: Neil H.E. Weste, David Harris, Ayan Banerjee, "CMOS VLSI Design", 3rd Edition Pearson Education.

Other Reference Books:

Ra) Kang. S.M and Leblebici Y., "CMOS Digital Integrated Circuits: Analysis and Design, McGraw Hill International Editions 3rd Edition 2003.
Rb) Pucknell D.A., Eshraghian K.,"Basic VLSI design, systems and circuits", Third edition, Prentice Hall of India Pvt. Ltd.
Rc) Fabricius E.D., "Introduction to VLSI design", McGraw Hill international editions.
Rd) Gregorian R., Temes G.C.,"Analog Mos integrated circuits for signal processing", Wiley interscience publication.
Re) Sze S.M.,"VLSI Technology", Second edition, McGraw Hill International Edition.
Rf) IEEE Journals of solid state circuits, VLSI system.
Rg) Martin. Ken, "Digital Integrated Circuit Design", Oxford University Press, Inc.
Rh) Johns. David A. and Martin K, "Analog Integrated Circuit Design," John Wily & Sons. Inc. 2002.
Ri) Michael. L. Bushnell and Vishwani. D. Agrawal, "Essentials Of Electronic Testing For Digital, Memory And Mixed Signal VLSI Circuits. Kluwer Academic Publishers, Third Edition, 2004

5. Notices: All notices will be put up on the CMS only

6. Course Plan :

Lect. No.	Learning Objectives	Topic to be covered	Chapter in the Text Book
	Common Topics		
2	1. Introduction to VLSI Design Methodologies	Moore's Law, Y chart, Quality Metrics of Digital Design. VLSI Design flow	Chapter-1**(T1)** /Chapter-1 (R1)
5(7)	2. CMOS Technology, Design Rules, MOS Capacitances, Scaling	MOS device modeling, parasitic capacitances, MOS scaling techniques, latch up. An overview of fabrication of CMOS circuits, layout of other gates.	Chapter-2,3,4 (**T1)**/Chapter-2,3,(4.5) (R1) + Class Notes
	Digital Design I:		
8(15)	3. CMOS Inverter and combinational logic circuits.	Digital circuit design styles for logic, Combinational blocks design.Device sizing using logical effort. Introduction to electrical efforts.	Chapter-5,6**(T1)** /Chapter-4,6 (R1) + Class Notes
8(23)	4. Synchronous system and Sequential circuits design	Synchronous design, timing metrics, Design of flip-flops, Timing issues (clock skew and jitter). Methods to reduce timing hazards.	Chapter-7,10**(T1)** /Chapter-7 (R1) + Class Notes
	Analog Design		
4(27)	1. Advanced Current Sources & sinks; Current Reference circuit,	Basic and cascaded NMOS /PMOS /CMOS gain stages. Advanced current mirrors; current and voltage references design.	Chapter-3,4.5**(T2)** + Class Notes
5(32)	2. Operational amplifier architectures and Feedback circuits.	Differential amplifier, matching of devices, mismatch analysis, common mode feedback circuits	Chapter-8,9**(T2)** + Class Notes
	Digital Design II:		
5(37)	5. Arithmetic Block Design	Designing of adders, multipliers, and shifters	Chapter-11 (**T1**)
3(40)	6. Design verification	An overview of design verification.	Chapter-15 (R1) + Class Notes

7. Evaluation Scheme :

Component	Duration	Weightage(%)	Marks	Date & Time	Nature of Component
Quizzes	30 min	30	60		Closed Book
Mid-Sem Exam	90 min	30	60	14/10 - 9.30 - 11.00AM	Open Book
Comp. Exam	180 min	40	80	20/12 FN	Closed Book

8. ChamberConsultation Hours: Will be discussed in the class.

9. Make up Policy: Make up will be given only on genuine reasons. Applications for makeupshould be given in advance and prior permission should be obtained for Scheduled tests.

10. Academic Honesty and Integrity Policy: Academic honesty and integrity are to be maintained by all the students throughout the semester and no type of academic dishonesty is acceptable.

Instructor-In-Charge
EEE F313/INSTR F313