



FIRST SEMESTER 2021-2022
Course Handout Part II

Date: 20-08-2021

In addition to part-I (General Handout for all courses appended to the time table) this portion gives further specific details regarding the course.

Course No. : CS / EEE / ECE / INSTR F215
Course Title : Digital Design
Instructor-in-Charge : Ankur Bhattacharjee

Scope and Objective of the Course:

The objective of the course is to impart knowledge of the basic tools for the design of digital circuits and to provide methods and procedures suitable for a variety of digital design applications. The course also provides laboratory practice using the digital ICs leading to various operations of digital electronics.

Textbooks:

- T1:** M. Moris Mano and Michael D. Ciletti “Digital Design”, Pearson, 5th Edition, 2013.
T2: Manual for Digital Design Laboratory.

Reference books

- R1.** Neal S. Widmer, Gregory L. Moss & Ronald J. Tocci, “Digital Systems Principles and Applications” Pearson, 12th Edition, 2018.
R2. Charles H. Roth, Jr. and Larry L. Kinney “Fundamentals of Logic Design” Cengage Learning 7th Edition, 2013.
R3: M.Moris Mano and Michael D. Ciletti “Digital Logic and Computer Design”, Pearson,, e-Book, 2016.

Course Plan:

Theory classes:

Lecture No.	Learning objectives	Topics to be covered	Chapter in the Text Book
1	Introduction to Digital Systems and Characteristics of Digital ICs. Number system	Discussion on course curriculum and evaluation procedure. Advantages and disadvantages of digital systems, Evolution of Digital technology terminologies used in digital systems. Binary numbers, two’s and one’s compliment	T1:2.9 T1:1.2-1.9
2	Number system	Addition and subtraction of binary	T1:1.2-1.9



		numbers, octal and hexadecimal numbers, binary codes	
3-4	Boolean algebra and logic gates	Boolean functions, canonical forms, logic gates.	T1: 2.1-2.8
5-6	Simplification of Boolean functions	K-Maps (3,4,5 variables)	T1: 3.1- 3.8
7-8	Simplification of Boolean functions	QM Method	T1: 3.10
9	Simplification of Boolean functions	Mutli-level and Multi-output Circuits Hazards in in Combinational Logic	R2: 7.1-7.7 R2: 8.4
10-14	Combinational Logic, Arithmetic circuits	Adders, Subtractors, Multipliers	T1: 4.1 – 4.7
15-19	MSI Components	Comparators, Decoders, Encoders, MUXs, DEMUXs	T1: 4.8 - 4.11
20-23	Sequential Logic circuits	Flip-Flops & Characteristic tables, Latches	T1: 5.1 - 5.4
24-28	Clocked Sequential Circuits	Analysis of clocked sequential circuits, state diagram and reduction	T1: 5.5, 5.7 & 5.8
29-32	Registers & Counters	Shift registers, Synchronous & Asynchronous counters, clock skew & Clock Jitter	T1: 6.1 - 6.5
33-35	Design of Digital Systems	Algorithmic State Machines (ASM)	T1: 8.4
36-38	Memory and PLDs	RAM, ROM, PLA, PAL	T1: 7.1 - 7.7
39-40	Digital Integrated Circuits	RTL, DTL,TTL,ECL & CMOS Gates, Implementation of Simple CMOS circuits	T1: 10.1 -10.7

List of Lab Experiments



Introduction to LT SPICE for simulating Digital circuits
Exp. 1 Implementation of Majority Circuit with Digital ICs using LT SPICE
Exp. 2 Implementation of Full Adder & Parity Generator with Digital ICs using LT SPICE
Exp. 3 Implementation of 4-bit Adder Subtractor and BCD Adder Digital ICs using LT SPICE
Exp. 4 Implementation of Majority Circuit with Verilog-A using ISE (Gate level Modelling)
Exp. 5 Implementation of Full Adder with Verilog-A using ISE (Data Flow Modelling)
Exp. 6 Implementation of 4-bit Adder & BCD Adder with Verilog-A in ISE (Data Flow Modelling)
Exp. 7 Decoders, multiplexers and Demultiplexers with Digital ICs using LT SPICE
Exp. 8 Latches, flip-flops, Counter with Digital ICs using LT SPICE
Exp. 9 Decoders, multiplexers and Demultiplexers with Verilog-A using ISE
Exp. 10 Latches, flip-flops, Counter with Verilog-A using ISE
Exp. 11 CMOS Inverter Design using LT SPICE
Exp. 12 CMOS Adder using LT SPICE

Evaluation Scheme:

Component	Duration	Weightage (%)	Marks allotted	Date & Time	Nature of Component
Assignment(s) /Quiz	-	10%	20	To be announced	Open Book
Mid Semester Examination	90 Minutes	30%	60	20/10/2021 9.00 - 10.30AM	Open Book
Regular Lab	During Lab hours	15%	30	Regular Lab days	-
Final Lab Examination	-	10%	20	To be announced	Open Book
Comprehensive Exam	120 minutes	35%	70	16/12 FN	Open Book
Total		100%	200		

Chamber Consultation Hour: To be announced in the class

Notices: All notices will be uploaded in Google Classroom for the respective Sections and also in CMS.

Make-up Policy: There will be make-up for the Mid-Semester and End-Semester examination subject to prior approval taken from the IC. No make-up will be allowed for Assignment and/or Quiz.

Lab make-up will be considered only with prior approval taken from the IC in case of medical emergencies. Only one buffer session will be kept for make-up.



Academic Honesty and Integrity Policy: Academic honesty and integrity are to be maintained by all the students throughout the semester and no type of academic dishonesty is acceptable.

Dr. Ankur Bhattacharjee

INSTRUCTOR-IN-CHARGE

