Birla Institute of Technology & Science, Pilani
Hyderabad Campus

FIRST SEMESTER 2023-2024

Course Handout Part II

Date: 11-08-2023

In addition to part-I (General Handout for all courses appended to the timetable) this portion gives further specific details regarding the course.

Course No	CS / EEE / ECE / INSTR F215
Course Title	Digital Design
Instructor in charge	Dr. Joyjit Mukherjee
Instructors for Lectures	Prof. BVVSN Prabhakar Rao, Dr. Joyjit Mukherjee
Tutorial Instructors	Prof. BVVSN Prabhakar Rao, Dr. Joyjit Mukherjee, Prof. Soumya J, Dr. Sourav Nandi, Dr. Subhradeep Pal
Practical Instructors	**Faculty**: Prof. BVVSN Prabhakar Rao, Dr. Joyjit Mukherjee, Prof. Sumit Kumar Chatterjee, Dr. Ankur Bhattacharjee **Research Scholars**: Shuvra Jyoti Bose, Parvathy Nair, Imran Khan, Bishal Kumar Keshari, Gowtham Polumati, Naresh Bahadursha, Vanmathi S

Scope and Objective of the Course:

The objective of the course is to impart knowledge to students on the basic concepts of digital logic and the tools, methods and procedures used for designing digital logic circuits for various applications. The course also provides laboratory practice using simulation tools, digital ICs and trainer kits to simulate and implement various operations of digital electronics.

Textbooks:

T1: M. Moris Mano and Michael D. Ciletti "Digital Design", Pearson, 5th Edition, 2013.

Reference books

R1. Neal S. Widmer, Gregory L. Moss & Ronald J. Tocci, "Digital Systems Principles and Applications" Pearson, 12th Edition, 2018.

R2. Charles H. Roth, Jr. and Larry L. Kinney "Fundamentals of Logic Design" Cengage Learning 7th Edition, 2013.

R3: Donald D. Givonne, "Digital Principles and Design" TMH, 2003

Course Plan:

Lecture No.	Learning objectives	Topics to be covered	Chapter in the Textbook
1	Introduction to Digital Systems and Characteristics of Digital ICs.	Course Overview. Advantages and disadvantages of digital systems, Evolution of Digital technology terminologies used in digital systems.	**T1**:2.9 **T1**:1.2-1.9

2	Number system & Codes	Addition and subtraction of binary numbers, octal and hexadecimal numbers, binary codes	**T1**:1.2-1.9
3-4	Boolean algebra and logic gates	Boolean functions, canonical forms, logic gates.	**T1**: 2.1-2.8
5-6	Simplification of Boolean functions	K-Maps (3,4,5 variables)	**T1**: 3.1- 3.8
7-8	Simplification of Boolean functions	QM Method	**T1:** 3.10
9	Simulation and synthesis	Hardware Description Language (Verilog HDL)	
10	Simplification of Boolean functions	Multi-level and Multi-output Circuits Hazards in Combinational Logic	**R2:** 7.1-7.7 **R2**: 8.4
11-15	Combinational Logic, Arithmetic circuits	Adders, Subtractors, Multipliers, HDL Models of Combinational Circuits.	**T1**: 4.1 – 4.7
16-20	MSI Components	Comparators, Decoders, Encoders, MUXs, DEMUXs	**T1:** 4.8 - 4.11
21-22	Programmable Logic Devices	Read-Only Memory, Programmable Logic Array, Programmable Array Logic	
23-26	Sequential Logic circuits	Latches, Flip-Flops & Characteristic tables,	**T1**: 5.1 - 5.4
27-29	Clocked Sequential Circuits	Analysis of clocked sequential circuits, state diagram and reduction, Design Procedure, HDL Models of Sequential circuits	**T1**: 5.5, 5.7 & 5.8
30-34	Registers & Counters	Shift registers, Synchronous & Asynchronous counters, clock skew & Clock Jitter	**T1**: 6.1 - 6.5
35-37	Memory	Introduction, Random-Access Memory, Memory Decoding	**T1**:7.1 - 7.7
38-39	Design of Digital Systems	Algorithmic State Machines (ASM)	**T1:** 8.4
40	Digital Integrated Circuits	RTL, DTL, TTL, ECL & CMOS Gates, Implementation of Simple CMOS circuits	**T1**:10.1 -10.7

List of Lab Experiments

Exp. 1 Introduction to Hardware Trainer Kit and Verilog HDL
Exp. 2 Implementation & Simulation of Boolean Functions using Logic Gates & Verilog Gate Level Modeling
Exp. 3 Parity Generator and Code Converter using Verilog Data Flow Modeling and Implementation on FPGA Board
Exp. 4 Implementation of Adders and Subtractor on the Digital Trainer Kit
Exp. 5 Verilog: Instantiation and Implementation of Adders on FPGA Kit

Exp. 6 Implementation of BCD to 7-Segment Decoder on Digital Trainer Kit and BCD Adder using Verilog Data Flow Modeling
Exp. 7 Implementation of Decoders, Demultiplexers, and Multiplexers on Digital Trainer Kit
Exp. 8 Implementation of Comparators and Arithmetic Logic Units on Digital Trainer Kit
Exp. 9 Implementation & Simulation of Latches and Flip-Flops using Digital Trainer Kit and Verilog Gate Level Modeling
Exp. 10 Implementation & Simulation of Counters using Digital Trainer Kit and Verilog Data Flow Modeling
Exp. 11 Implementation of Shift Registers using Digital Trainer Kit

Evaluation Scheme:

Component	Duration	Weightage (%)	Marks allotted	Date & Time	Nature of Component
Quizzes	-	10%	20	To be announced	Open book
Mid Semester Examination	90 Minutes	30%	60	11/10 - 9.30 - 11.00AM	Closed Book
Regular Lab	During Lab hours	10%	20	Regular Lab classes	Open Book
Final Lab Examination	-	10%	20	To be announced	Open Book
Comprehensive Exam	180 minutes	40%	80	12/12 FN	Closed Book
Total		100%	200		

Chamber Consultation Hour: To be announced in the class.

Notices: All notices concerning the course will be displayed in the CMS

Make-up Policy:
1.No make-up will be given for the quiz and laboratory exam evaluation components.
2.For the mid-semester and end-semester examinations, make-up will be given **only for genuine reasons** and in such cases **prior permission from the instructor in charge** needs to be obtained.
3. Make-up for the regular laboratory classes will be allowed only for genuine reasons and in such cases prior permission from the respective lab section instructor needs to be obtained.

Academic Honesty and Integrity Policy: Academic honesty and integrity need to be maintained by all the students throughout the semester and no type of academic dishonesty is acceptable.

Dr. Joyjit Mukherjee

INSTRUCTOR-IN-CHARGE