Birla Institute of Technology & Science, Pilani
Hyderabad Campus

FIRST SEMESTER 2024-2025

Course Handout Part II

Date:01-08-2024

In addition to part-I (General Handout for all courses appended to the timetable) this portion gives further specific details regarding the course.

Course No	**CS / EEE / ECE / INSTR F215**
Course Title	Digital Design
Instructor in charge	**Prof. Ponnalagu RN**
Instructors for Lectures	Prof. Ponnalagu RN, Prof. Joyjit Mukherjee, Prof. BVVSN Prabhakar Rao,
Tutorial Instructors	Prof. Ponnalagu RN, Prof. Joyjit Mukherjee, Prof. Niranjan raj, Prof. Pritesh Kumar Yadav, Prof. Soumya J, Prof. BVVSN Prabhakar Rao,
Practical Instructors	**Faculty**: Prof. Ponnalagu, Prof. Syed Ershad Ahmed, Prof. Joyjit Mukherjee, Prof. Niranjan Raj, Prof. Neha Tak **Research Scholars**: Shubham Deepak Yadav, Amgith G.S, Sohel Siraj, Nongthombam Joychandra Singh, Gowtham Polumati, Mou Sarkar, Sajith P M, Vanmathi S, K S Vaishnavi Isha Basumatary, Kandi Mounica, Abbidi Shivani Reddy, Baishali Paul, Nandini Ashok Kumar Trivedi, Shaik Sultan, Pavar Sai Kumar

Scope and Objective of the Course:

The objective of the course is to impart knowledge to students on the basic concepts of digital logic and the tools, methods and procedures used for designing digital logic circuits for various applications. The course also provides laboratory practice using simulation tools, digital ICs and trainer kits to simulate and implement various operations of digital electronics.

Textbooks:

T1: M. Morris Mano and Michael D. Ciletti "Digital Design", Pearson, 6th Edition, 2018.

Reference books

R1. Neal S. Widmer, Gregory L. Moss & Ronald J. Tocci, "Digital Systems Principles and Applications" Pearson, 12th Edition, 2018.

R2. Charles H. Roth, Jr. and Larry L. Kinney "Fundamentals of Logic Design" Cengage Learning 7th Edition, 2013.

R3: Donald D. Givone, "Digital Principles and Design" TMH, 2003

Course Plan:

Lecture No.	Learning objectives	Topics to be covered	Chapter in the Textbook

1	To learn the basic concepts of digital Systems and digital ICs.	Course Overview. Advantages and disadvantages of digital systems, Evolution of digital technology, terminologies used in digital systems.	**T1**:1.1 **T1**:2.9
2	To understand the different number systems and codes used in digital logic systems	Binary, decimal, Octal, Hexadecimal number system and binary codes, Binary arithmetic	**T1**:1.2-1.7
3-4	To understand the Boolean algebra and logic gates used in digital logic systems	Binary Logic, Boolean functions, Canonical forms, logic gates, Boolean laws, theorems and Postulates	**T1**: 1.9, 2.1-2.8
5-7	To simplify Boolean functions using K-map method	Karnaugh map method (3, 4 and 5 variables) for simplifying SOP and POS expressions, K-map with don't care terms	**T1**: 3.1- 3.6
8-9	To simplify Boolean functions using K-map method using QM method	Quine Mc Cluskey (QM) Method	**Class notes**
10-11	To realize Boolean functions using logic gates	Multi-level and Multi-output Circuits, NAND and NOR realization of Boolean functions	**T1: 3.7** **R2:** 7.1-7.7
12-15	To understand the Combinational Logic circuits and Arithmetic circuits in digital logic systems	Analysis and Design of combinational logic circuits, Adders, Subtractors, Multipliers,	**T1**: 4.1 – 4.7
16-18	To study about the medium scale integrated digital logic componenets	Comparators, Decoders, Encoders, Multiplexers, Demultiplexers	**T1:** 4.8 - 4.11
19-22	To understand the concept of Sequential logic circuits	Latches, Flip-Flops and Characteristic tables and characteristic Equations	**T1**: 5.1 - 5.4
23-26	To analyze and design clocked Sequential Circuits	Analysis of clocked sequential circuits, state diagram and reduction, Design of clocked sequential circuits	**T1**: 5.5, 5.7 & 5.8
27-31	To study about the registers and counters in digital logic systems	Shift registers, Synchronous and Asynchronous counters, Clock skew and Clock Jitter	**T1**: 6.1 - 6.5
32-33	To understand the basic concept of memory in digital logic systems	Introduction, Random-Access Memory, Memory decoding, Read-Only Memory,	**T1**:7.1 - 7.5

34-36	To understand the working and design of programmable logic devices	Programmable logic array, Programmable array logic, Introduction to FPGA	**T1**:7.7 - 7.8
37-38	To design state machines	Algorithmic State Machines (ASM)	**T1:** 8.4
39-40	To study and implement digital integrated circuits	RTL, DTL, TTL, ECL and CMOS Gates, Implementation of Simple CMOS circuits	**T1**:10.1 - 10.7

List of Lab Experiments

Exp. 1 Introduction to digital trainer kit and Verilog HDL
Exp. 2 Implementation and Simulation of Boolean Functions using Logic Gates and Verilog Gate Level Modeling
Exp. 3 Parity Generator and Code Converter using Verilog Data Flow Modeling and Implementation on FPGA Board
Exp. 4 Implementation of Adders and Subtractor on the digital trainer kit
Exp. 5 Verilog: Instantiation and Implementation of Adders on FPGA kit
Exp. 6 Implementation of BCD to 7-Segment Decoder on digital trainer kit and BCD Adder using Verilog Data Flow Modeling
Exp. 7 Implementation of Decoders, Demultiplexers, and Multiplexers on digital trainer kit
Exp. 8 Implementation of Comparators and Arithmetic Logic Units on digital trainer kit
Exp. 9 Implementation & Simulation of Latches and Flip-Flops on digital trainer kit and Verilog Gate Level Modeling
Exp. 10 Implementation & Simulation of Counters on digital trainer kit and Verilog Data Flow Modeling
Exp. 11 Implementation of Shift Registers on digital trainer kit

Evaluation Scheme:

Component	Duration	Weightage (%)	Marks allotted	Date & Time	Nature of Component
Quizzes	-	10 %	20	To be announced	Closed Book
Mid Semester Examination	90 minutes	30 %	60		Closed Book
Regular Lab	During lab hours	10 %	20	Regular Lab classes	Open Book
Final Lab Examination	-	10 %	20	To be announced	Open Book
Comprehensive Examination	180 minutes	40 %	80	4.12.2024 (AN)	Closed Book
Total		100 %	200		

Chamber Consultation Hour: To be announced in the class.
Notices: All notices concerning the course will be displayed in the CMS
Make-up Policy:

1. No make-up will be given for the **quizzes and laboratory exam**

2. For the mid-semester and end-semester examinations, make-up will be given ONLY in cases of sickness (hospitalization) or urgency for going out of station. In such a case, the student must produce sufficient proof or must have taken the prior permission from the IC of the course.

3. Make-up for the regular laboratory classes will be allowed only for genuine reasons and in such cases prior permission from the respective lab section instructor needs to be obtained.

Academic Honesty and Integrity Policy: Academic honesty and integrity need to be maintained by all the students throughout the semester and no type of academic dishonesty is acceptable.

Prof. Ponnalagu RN

INSTRUCTOR-IN-CHARGE