Birla Institute of Technology & Science, Pilani
Hyderabad Campus

SECOND SEMESTER 2023-24

Course Handout (Part -11)

Date: 29 12 2023

In addition to Part I (General Handout for all courses appended to the time table) this portion gives further specific details regarding the course.

Course No. : MEL G641
Course Title : CAD for IC Design
Instructor-in-charge : Sumit K Chatterjee

Course Description: Introduction to VLSI design methodologies and supporting CAD tool environment; overview of `C', data structure, graphics and CIF; concepts, structures and algorithms of some of the following CAD tools; schematic editors; layout editors; module generators; silicon compilers; placement and routing tools; behavioral, functional, logic and circuit simulators; aids for test generation and testing.

1. Scope and Objective of the course:

To teach the basic concepts of CAD tools used for IC/VLSI Design process. To be conversant with the use of existing CAD tools and algorithms for all the stages of the design cycle of a VLSI chip design, To study modeling using HDL (VHDL/Verilog) and to study the design issues involved in the development of CAD tools., Current trends in CAD tools for IC/VLSI design.

2. Text Book:

(i) Algorithm for VLSI Physical Automation, 3rd Edition Author: Naveed Sherwani

Publisher, Year: Kluwer Academic Press, 1998

3. Reference Books

(i) An Introduction to CAD for VLSI Author: Stephen M. Trimberger

Publisher, Year: Kluwer Academic Press 1987.

(ii) VLSI Physical Design Automation: Theory and practice Author: Sadiq M Sait and Habib Youssef

Publisher, Year: World Scientific Press, 1999

(iii) Computer Aids for VLSI Design Author: Steven M. Rubin

Publisher, Year: Addison Wesley, 1987

(iv) Simulation in the Design of Digital systems Author: John B. Gosling

Publisher, Year: Cambridge University Press (CUP), 1993

(v) Introduction to VLSI Systems Author: Carver Mead and Lynn Conway Publisher, Year: Addison-Wesley,1980

(vi) A VHDL Primer, 3rd Edition, Author: J. Bhaskar

Publisher, Year: Pearson /Prentice-Hall, 1999

(vii) Verilog HDL Author: Samir Palnitkar

Publisher, Year: Pearson Education Asia, 2007

(viii) Synthesis and Optimization of Digital Circuits Author: Giovanni De Micheli Publisher, Year: Tata McGraw-Hill, 1994

4. Course Plan

Topics	Lectures
An introduction to electronic system design and CAD for IC Design	1
CAD: A general overview	1
Timing and Power Analysis	5
Designing Strategies for Optimization (Area, Speed & Power)	4
High Level and logic Synthesis	4
Hardware Allocation and Assignment	5
Scheduling Algorithms	4
Partitioning	4
Floor-planning and Placement	4
Routing	3
Schematic, Layout and Stick Editors	2
Overview of CIF	1
Simulation (Behavioral , Functional, Logic, Mixed mode, and Fault simulation)	2
TOTAL	**40**

5. Evaluation schedule:

EC No.	Components	Duration	Weightage (%)	Date & Time	Remarks
1.	Midsem Test	90 min.	20%	As per Timetable	Closed Book
2.	Comprehensive Examination	3 Hrs	40%	As per timetable	Closed Book
3.	Project/Seminar/Lab Assignments	Regular	40%		Open Book

6. Chamber consultation hour: Will be announced in the class.

7. Notices: All notices related to the course will be put on the CMS **only**.

8. Make-up policy: Makeup will be given only for genuine reasons (for example, make up seeking on a medical background will be accepted only with a medical certificate from a registered medical practitioner).Applications for make up should be given in advance, and prior permission should be obtained for Scheduled tests.

9. Academic Honesty and Integrity Policy: Academic honesty and integrity are to be maintained by all the students throughout the semester and no type of academic dishonesty is acceptable.

Instructor In-Charge

(MEL G641)