Course:	Computer Organization - ENCM 369
Lab #:	6
Instructor:	N. Bartley
Group Submission for:	B02
Submitted by:	William Fraser
UCID:	30158991
Partner:	Aarsh Shah
UCID:	30150079
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Exercise A: 12-bit two's complement and RISC-V instructions

1. Machine Code for: addi sp, sp, -112
   (I-type instruction)

I-Type

31:20	19:15	14:12	11:7	6:0
imm$_{11:0}$	rs1	funct3	rd	op
12 bits	5 bits	3 bits	5 bits	7 bits

From table B.1

funct3 = 000
op = 0010011

Then

Decimal	2's complement	32-bit sign-extended
$-112 \Rightarrow$	$1001\_0000_2 \Rightarrow$	$[24 \text{ ones}]\_1001\_0000_2$

$sp = 2_{10} = 00010_2$

Therefore Machine Code

1111 1001 0000	00010	000	00010	0010011

2. inputs:

A = 0x7fff_ed80 $\Rightarrow$ 0111_[12 ones]_1110_1101_1000_0000$_2$

B = Value from above $\Rightarrow$ 1111_[12 ones]_1111_1111_1001_0000$_2$

Output: 0111_[12 ones]_1110_1101_0001_0000$_2$

Perform 32-bit adder addition

Exercise B: Integer addition examples

<u>Part I</u>

$$\begin{array}{r} {}^{1011} \\ a = \text{0xb4} = 1011\_0100_2 \\ b = \text{0xb3} = 1011\_0011_2 \\ \hline 0110\_0111_2 \end{array}$$

2's complement: Overflow because MsB carryout doesn't match previous carry out.

Unsigned overflow: Overflow because output is smaller than both a and b.

<u>Part II</u>

$$\begin{array}{r} {}^{11} \\ a = \text{0xd0} = 1101\_0000_2 \\ b = \text{0xe0} = 1110\_0000_2 \\ \hline 1011\_0000_2 \end{array}$$

2's complement: No Overflow because MsB carryout matches previous carry out.

Unsigned overflow: Overflow because output is smaller than both a and b.

<u>Part III</u>

$$\begin{array}{r} {}^{01111} \\ a = \text{0x78} = 0111\_1000_2 \\ b = \text{0x0b} = 0000\_1011_2 \\ \hline 1000\_0011_2 \end{array}$$

2's complement: Overflow because MsB carryout doesn't match previous carry out.

Unsigned overflow: No Overflow because carryout of MsB is 0.

<u>Part IV</u>

$$\begin{array}{r} {}^{001} \\ a = \text{0x35} = 0011\_0000_2 \\ b = \text{0x2d} = 0010\_1101_2 \\ \hline 0101\_1101 \end{array}$$

2's complement: No Overflow because MsB carryout matches previous carry out.

Unsigned overflow: No Overflow because carryout of MsB is 0.

Exercise E: Integer subtraction examples

Part I

a: 0010-0000
b: 1000_1111

$$\begin{array}{r}
\overset{0\,1\,1\,0\,0\quad 0\,0\,0\,1}{} \\
a = \quad 0010\_0000 \\
\text{inverted bits of } b = \quad \underline{0111\_0000} \\
a-b = \quad 1001\_0001
\end{array}$$

Signed overflow occurred because a-b
was a (pos. number) - (neg. number), but
resulted in a neg. number. Wrong Sign.

Unsigned overflow did occur because the
Cout of the MSB is 0.

Part II

a: 1100 - 1000
b: 0110_1110

$$\begin{array}{r}
\overset{1\,0\,0\,0\,0\quad 0\,0\,1\,1}{} \\
a = \quad 1100\_1000 \\
\text{inverted bits of } b = \quad \underline{1001\_0001} \\
0101\quad 1010
\end{array}$$

There is signed overflow because a
(neg. num) - (pos. num) resulted in a
pos. num. This is the wrong sign.

Unsigned overflow does not occur as
the Cout of the MSB is 1.

Part III

a: 1010_1100
b: 1010_0101

$$\begin{array}{r} {}^{1111\,1\;001} \\ a: 1010\_1100 \\ \text{inverted bits of } b = 0101\_1010 \\ \hline 0000\_0111 \end{array}$$

Signed overflow did not occur because it is a larger magnitude negative number subtracting a smaller magnitude number, resulting in a negative number, which is expected.

Unsigned overflow did not occur because the Cout of the MSB is 1.

Part IV

a: 0010_0110
b: 0010_0111

$$\begin{array}{r} {}^{0000\,0\;001} \\ a: 0010\_0110 \\ \text{inverted bits of } b = 1101\_1000 \\ \hline 1111\_1111 \end{array}$$

Signed overflow did not occur because it is a smaller magnitude pos. num subtracting a larger magnitude pos. num, resulting in a negative number, which is expected.
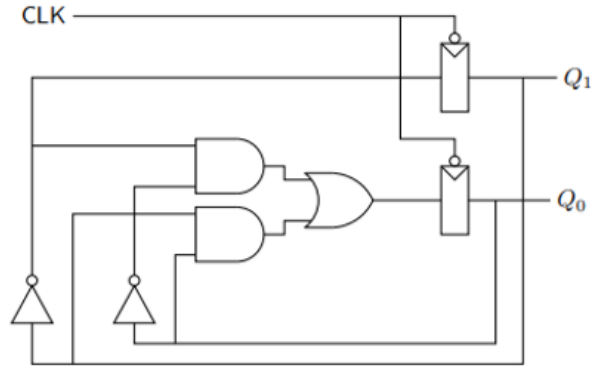
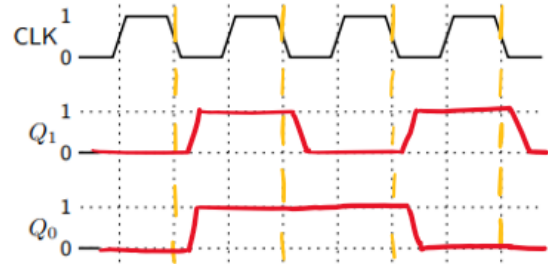Unsigned Overflow did occur because the Cout of the MSB is 0.

Exercise F: Review of D Flip-Flops

Worksheet for Exercise F

Part I

$$Q_0' = Q_0 Q_1 + \overline{Q_0}\,\overline{Q_1} \qquad Q_1' = \overline{Q_1}$$

CLK

Q_1

Q_0

CLK

Q_1

Q_0

Part II

$$Q_0' = A$$
$$Q_1' = Q_0$$
$$Q_2' = Q_1$$

CLK

A

Q_0 Q_1 Q_2

CLK

A

Q_0

Q_1

Q_2