



*Leading Centre of Excellence in Chennai*

**“From Logic to Layout – Build Your Career in Chip Design”**

# Advanced ASIC Design Verification Course



**Industry-Focused  
Training**



**Real-Time  
Project Experience**



**Internship  
+  
Placement  
Support Until  
Secure a Job**

# About

**Silicon Craft VLSI** Training & Research Institute delivers an exclusive, industry-aligned **Advanced ASIC Design Verification** program in semiconductor design. With India's semiconductor sector expanding rapidly, the demand for skilled professionals far outpaces the current talent pool. A career in **semiconductor** design is not only prestigious but also offers highly competitive remuneration, often exceeding traditional software roles.

## Why Choose **Advanced ASIC Design Verification?**

- **High Demand:** 80% of semiconductor jobs are in verification.
- **Core Skillset:** Industry-standard methodologies (System Verilog, UVM, Functional Verification).
- **Future-Ready:** Powering innovations in AI, 5G, Automotive & IoT.
- **Career Growth:** Opportunities with top semiconductor MNCs.

## Our Training Edge

- Hands-on, industry-focused labs
- Mentorship by semiconductor experts
- Innovation-driven, research ecosystem
- Career-Focused Internship Support



## The **Silicon Craft VLSI**

### **Advantage**

#### **1. Innovation-Driven Learning**

Hands-on with the latest design & verification methodologies.

#### **2. Industry-Backed Training**

Built in collaboration with semiconductor experts.

#### **3. End-to-End Growth**

From fundamentals to project execution → we cover it all.

#### **4. Career Pathway**

Internships + placement support Until Secure a Job to launch your career in VLSI.



## COURSE MODULE:

## Advanced ASIC Design Verification Course

### Module 1: Introduction to VLSI

- Introduction to VLSI Design
- ASIC vs FPGA: Choosing the Right Technology
- Introduction to FPGA/ASIC Design Verification flow
- An Introduction to EDA Tools

### Module 2: Advanced Digital Systems

- Number Systems and Conversions
- Logic gates, K-maps, minimization.
- Combinational Circuits - Design and Analysis
- Sequential Circuits – Counters, Shift Registers, Sequence Detectors - Design and Analysis
- Timing Parameters
- Finite State Machines
- Memory – SRAM, DRAM, register files, FIFO.

### Module 3: CMOS Basics

- Introduction to CMOS Technology
- CMOS Fundamentals
- CMOS Invertor Characteristics
- CMOS Fabrication Process
- CMOS Circuit Design Basics
- CMOS Power Consumption
- Low Power Design Techniques

### Module 4: Linux & Productivity

- Linux Basics – shell navigation, permissions, process management.
- VI Editor – editing, searching, macros.
- Shell Scripting (bash) – automation, file operations.
- Make file – compilation automation.
- Git & Version Control – cloning, branching, merging, collaboration.

### Module 5: Advanced Verilog HDL

#### - RTL Modeling & Design Flow

- Verilog Fundamentals
- Data Types and Operators in Verilog
- Modeling Styles – behavioral, structural, dataflow, mixed-style
- Combinational & Sequential Logic – blocking vs non-blocking, latches, FFs, counters.
- Synthesizable RTL Design Principles
- Parameterized & Hierarchical Design – parameters, generate statements, reusable modules.
- Testbench Development – stimulus, tasks/functions, File I/O
- Timing Controls in RTL Design
- Memory & FSMs – ROM, RAM, FIFO, Moore/Mealy FSMs.
- Compiler Directives and System Tasks
- Synthesis Considerations – synthesizable vs non-synthesizable, FPGA/ASIC guidelines.
- Effective Verification Strategies in Verilog
- Self-Checking Testbench Constructs
- Real-World Applications and Case Studies

### Module 6: Static Timing Analysis in Digital Design

- Introduction to Static Timing Analysis (STA)
- Timing Path and Constraints
- Different Types of Clocks and Clock Domains
- Timing Exceptions
- How to Fix Timing Failure
- STA Issues and Solutions
- Methods to Improve Timing

## COURSE MODULE:

## Advanced ASIC Design Verification Course

### Module 7: System Verilog for Verification

- Functional Verification Overview
- Introduction to SystemVerilog
- Advanced Data Types & Arrays in SystemVerilog
- Procedural Statements and Operators
- Virtual Interfaces and Building Verification Environment
- Mailbox, Semaphore, Packages, Compilation Unit
- Object-Oriented Programming and Randomization
- Fork-Join and Inter-Process Synchronization (Threads)
- Program and Clocking Block
- Tasks and Functions
- Constraining and Randomization Techniques
- Functional and Code Coverage Analysis
- Regression Testing Strategies
- Assertions (SVA) – temporal checks.

### Module 8: UVM (Universal Verification Methodology)

- UVM Basics- Components, Objects, configuration.
- UVM Factory Registration
- UVM Phases
- UVM Testbench Architecture
- Configuring a Test Environment
- Analysis Components & Techniques
- Sequences – Virtual Sequences
- Transaction Level Modeling
- The UVM Messaging System
- Register Abstraction Layer
- Debug of SV and UVM
- UVM Callback Mechanism.

### Module 9: Protocols & SoC Concepts

- Memory Access Protocols
- Asynchronous FIFO Design
- Handling Clock Domain Crossing issues
- AMBA Protocol Overview – AXI, AXIS, AXIL, APB
- Mini Project: Design and Verification Using Memories Peripherals and AXI
- UART Protocol
- I2C Protocol
- SPI Protocol

### Module 10: Assertion-Based Verification - SVA (System Verilog Assertions)

- Introduction to Assertion-Based Verification (ABV)
- Immediate Assertions
- Simple Assertions
- Sequences and Sequence Composition
- Advanced SVA Features
- Assertion Coverage
- Advanced Applications and Case Studies

### Module 11: Verification Planning and Management

- Verification Plan Development
- Testbench (TB) Architecture Design
- Coverage Model and Analysis
- Simulation Process Tracking and Management
- Building Regression Test Suite
- Test Suite Optimization and Scalability

## COURSE MODULE:

## Advanced ASIC Design Verification Course

### Module 12: Business Professional Communication and Career Readiness

- Transition from College to Corporate
- Interpersonal Skills and Effective Presentation
- Email Etiquette and Professional Writing
- Resume Writing and Job Application Skills
- Mock Interviews: Technical and HR Rounds
- Interview Skills: Group Discussions and HR Round Preparation

### Module 13: Verification Project

#### - Phase I

- Verification and RTL Sign-off
- Project Specification Analysis
- Defining Verification Plan
- Creating Testbench Architecture
- Implementing Transactors
- Defining Transactions
- Implementing the Coverage Model
- Building the Top-Level Verification Environment
- Building Regression Test Suite
- Coverage Analysis and Coverage Closure
- Documentation and Project Presentation

### Module 14: Final Project in VLSI Design and Verification

- Design Specification Analysis
- Creating the Design Architecture
- Partitioning the Design
- RTL Coding in Verilog
- RTL Functional Verification

- RTL Synthesis
- Building Regression Test Suite
- Coverage Analysis and Coverage Closure
- Documentation and Project Presentation

### Highlights of Our Course

#### Industry-Driven Evaluation: Test and Mock Interviews with Industry Experts Covering Diverse Topics

- Assignments & Quizzes – integrated into every module to reinforce theoretical concepts, strengthen fundamentals, and ensure consistent learning progression.
- Module Tests – conducted for all modules to evaluate conceptual clarity, analytical thinking, and practical problem-solving skills.
- Mini-Projects – hands-on implementation of FSMs, FIFOs, ALUs, UARTs, and protocol IPs (e.g., APB-I2C bridge) to build strong RTL design and verification skills
- Major Projects – advanced design and verification projects including a RISC-V CPU with complete toolchain integration, UVM-based environments for standard on-chip and off-chip protocols, Network-on-Chip (NoC) and Network Interfaces (NI), multiprocessor systems, and real-time image and signal processing applications for FPGA/ASIC platforms.
- Resume Preparation – development of role-based resumes (DV, PD, FPGA, Embedded), project documentation, and GitHub portfolio building to highlight technical depth and practical achievements
- Mock Interviews – 12+ technical rounds across Verilog, Digital Design, SystemVerilog & UVM, plus debugging and HR simulations.

**"Launch Your Semiconductor Career  
with Our Advanced, Hands-On Training Program"**



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