INDIAN INSTITUTE OF TECHNOLOGY PATNA

CS226- Switching Theory Lab

Lab 3: Logic simulation Sub-blocks

Assignment:

(Design and simulate)

In this lab, you will begin to familiarise yourself with some standard blocks. This will help you learn more about logic, and build the fundamental components used various architectures.

Assignment:

P1:

A farmer has a dog, a goat, and a cabbage. The goat can eat cabbage and the dog can eat the goat. However, the dog does not like the cabbage. The farmer needs to cross a river and it can only carry two of the three (dog, goat, and cabbage) at a time in the boat. Let variables x, y, and z denote the position of the dog, goat, and cabbage on the south side of the river (0) or on the north side of the river (1), respectively. Let function F be an output of a logic function that will warn the farmer of anything is in danger.

(a) Write the truth table for the function.
(b) Let variable w denote the farmer position on the south (0) or the north side (1) of the river. Nothing is in danger in the presence of the farmer. Now modify the truth table for the four variable function.

Implement using basic gates and simulate using Logic-sim

(10 points)

P2:

Implement the function wx'y'+yw'z'+yxz+yxw using basic gates (AND, OR, INV)

(5 points)

P3: Write a Boolean equation and simulate in sum-of-products canonical form for each of the truth tables

(a)

A	B	Y
0	0	1
0	1	0
1	0	1
1	1	1

(b)

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

(c)

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

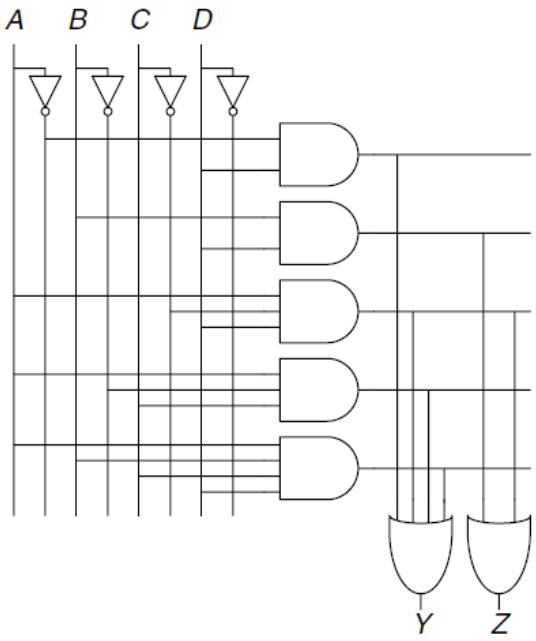
(d)

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

(e)

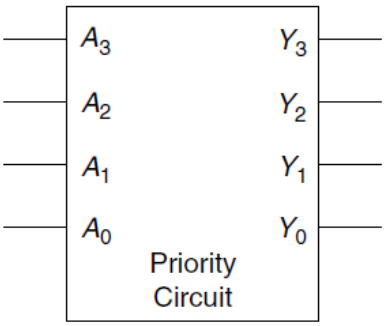
A	B	C	D	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

P4: Generate Truth Table for the following circuit and write Boolean equations and for the given circuit and verify using simulation.



P5: Write Boolean equations and verify.

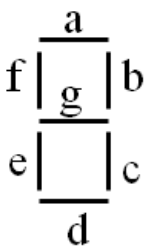
(10 points)

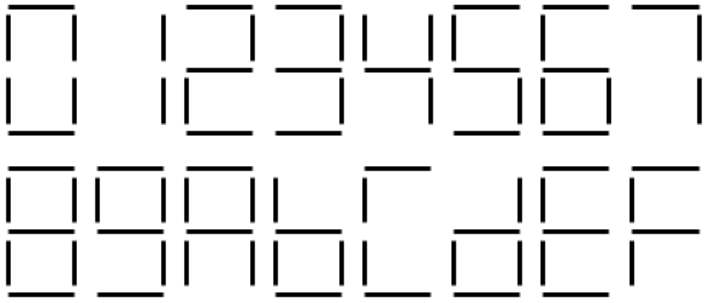


A_3	A_2	A_1	A_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	0
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	0
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	0
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	0
1	0	1	0	1	0	0	0
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	0
1	1	1	0	1	0	0	0
1	1	1	1	1	0	0	0

P6: Complete the truth table and **Write functions a, b, c, d, e, f, and g, and verify**

- **A function to display digits**
- **4 inputs X, Y, Z, W**
- **Seven outputs**
  - **a, b, c, d, e, f, and g**





X Y Z W	a b c d e f g
0 0 0 0	1
0 0 0 1	0
0 0 1 0	1
0 0 1 1	1

0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

Submission:

Submit your .circ file containing your various transistor-level/logic level implementations. Hand written report is required for this assignment. Show the simulations to TAs.

- The simulation files p1.circ, p2.circ, p3.circ, p4.circ, p5.circ, and p6.circ

- Zip the above five files. Zip file name is your role number.

Course work submission through Email: cs225.iitp@gmail.com
(use email subject Lab1_Logicsim_your roll number).
This work is due on: : 25th Jan