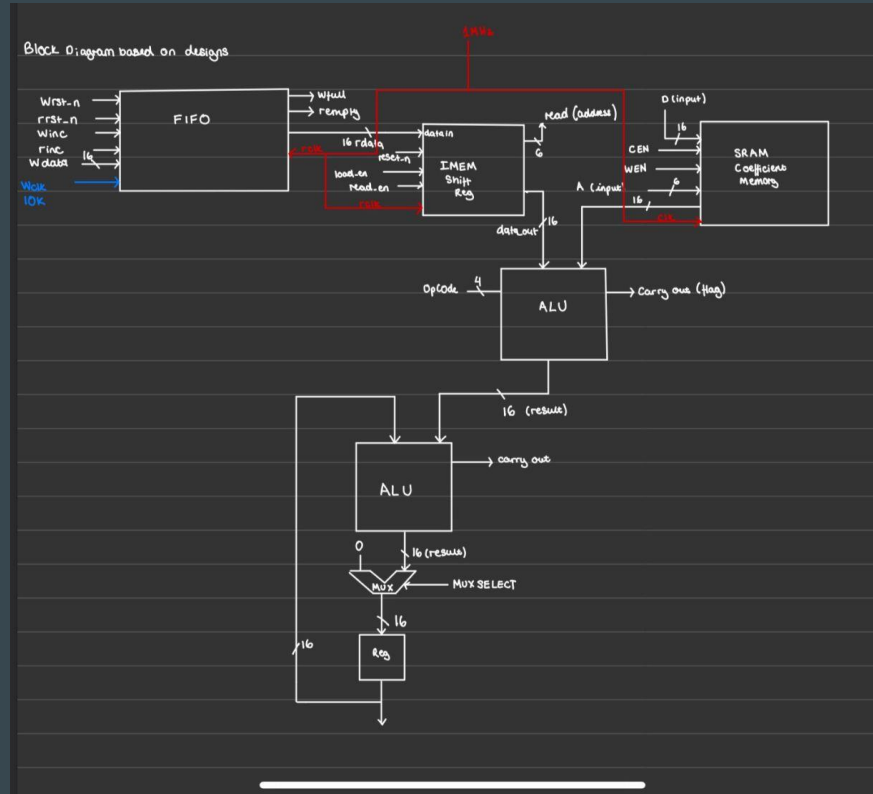# Group 4 - FIR Filter

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Aarya Agarwal (ASA2276) + Stephen Ogunmwonyi(ISO2107)

Architecture

The Metrics

Methods :
- Input: randomly generated 10k 16-bit real-valued numbers
- RTL coding from scratch: Yes
- Throughput: PT with DC-gen. sdf annotation
- Maximum clock frequency: PT with DC-gen. sdf annotation
- Energy efficiency: PT with the DC-gen. sdf and QS-gen. vcd annotations
- Area: DC-gen report
- Accuracy: RMSE against Matlab results in 32-b floating point numbers. Inputs are
- 16-bit and generated by the random function of Matlab

Results:
- Throughput: 22 [kS/s]
- Maximum clock frequency: 1 MHz (Could potentially get faster with some tweaking of pipelining)
- Total Power: 16uW
- Max power: 0.2889 W
- Area: 102245.77 um2
- Accuracy: Worst case: 0% | Average: 98.4%