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|---------------------------------|----------------------------------|---------------------|--------------------|
| Course Name: | Digital Design Laboratory | Semester: | III |
| Date of Performance: | 04 / 10 / 2024 | Batch No: | A1 |
| Faculty Name: | Bharathi Narayan | Roll No: | 16010123012 |
| Faculty Sign & Date: | | Grade/Marks: | ___/25 |

Experiment No: 6
Title: Shift Register

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| Aim and Objective of the Experiment: |
| To implement the SISO, SIPO, PISO, PIPO shift register using Universal IC 74194 |

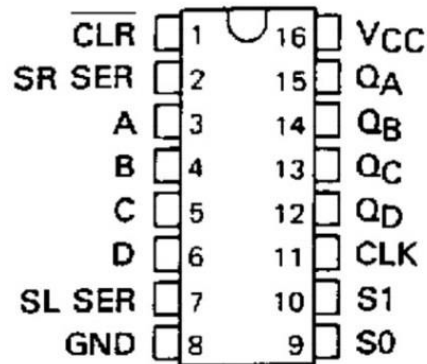
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| COs to be achieved: |
| CO3: Design synchronous and asynchronous sequential circuits. |

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| Tools used: |
| Trainer kits |

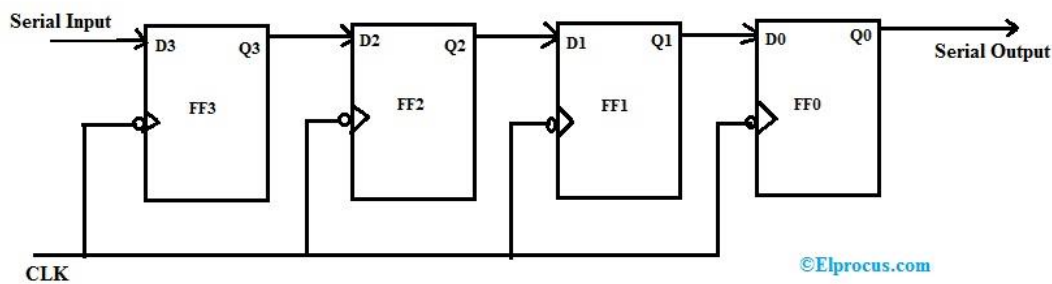
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| Theory: |
| <p>A register is capable of shifting its binary information in one or both directions is known as shift register. The logical configuration of shift register consist of a D-Flip flop cascaded with output of one flip flop connected to input of next flip flop. All flip flops receive common clock pulses which causes the shift in the output of the flip flop. The simplest possible shift register is one that uses only flip flop. The output of a given flip flop is connected to the input of next flip flop of the register. Each clock pulse shifts the content of register one bit position to right.</p> <p>The basic types of shift registers are</p> <ul style="list-style-type: none"> ● Serial In - Serial Out ● Serial In - Parallel Out ● Parallel In - Serial Out ● Parallel In - Parallel Out ● Bidirectional shift registers. |

Pin diagram of IC 74194 and Function table

74LS194 Pinout



Circuit diagram: Serial left shift



| clk | A | B | C | D |
|-----|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 3 | 0 | 1 | 0 | 0 |
| 4 | 1 | 0 | 0 | 1 |
| 5 | 0 | 1 | 0 | 0 |
| 6 | 0 | 0 | 1 | 0 |
| 7 | 0 | 0 | 0 | 1 |

Circuit diagram: Serial right shift

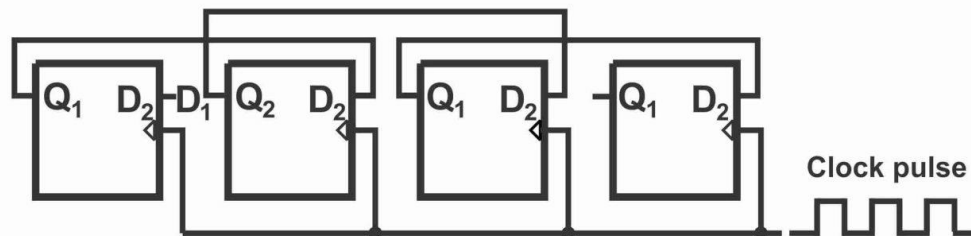
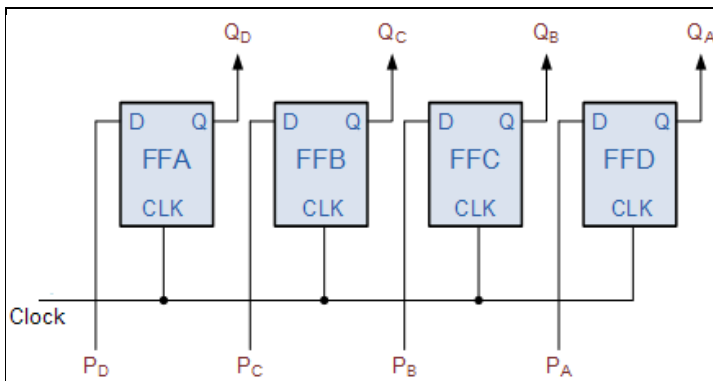


Fig 7.2: Shift-right register.

| clk | A | B | C | D |
|-----|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 2 | 0 | 1 | 0 | 0 |
| 3 | 1 | 0 | 1 | 0 |
| 4 | 1 | 1 | 0 | 1 |
| 5 | 0 | 1 | 1 | 0 |
| 6 | 0 | 0 | 1 | 1 |
| 7 | 0 | 0 | 0 | 1 |

Circuit diagram: Parallel in Parallel out



| clk | A | B | C | D | QA | QB | QC | QD |
|-----|---|---|---|---|----|----|----|----|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 |

Lab Work:

16010123012 Aaryan Shastri

Exp 6

→ Basic data movement through a shift Register

| Clock Pulse No. | QA | QB | QC | QD |
|-----------------|----|----|----|----|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 2 | 0 | 1 | 0 | 0 |
| 3 | 0 | 0 | 1 | 0 |
| 4 | 0 | 0 | 0 | 1 |
| 5 | 0 | 0 | 0 | 0 |

→ SISO (Serial Input)

| CLK | P3 | P2 | P1 | P0 | Q3 | Q2 | Q1 | Q0 |
|-----|----|----|----|----|----|----|----|----|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 3 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 4 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 |

→ SIPO

| CLK | P3 | P2 | P1 | P0 | Q3 | Q2 | Q1 | Q0 |
|-----|----|----|----|----|----|----|----|----|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 2 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 3 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 4 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |

→ PIPO

| CLK | P3 | P2 | P1 | P0 | Q3 | Q2 | Q1 | Q0 |
|-----|----|----|----|----|----|----|----|----|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 2 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 3 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 4 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |

→ PIPO

| CLK | P3 | P2 | P1 | P0 | Q3 | Q2 | Q1 | Q0 |
|-----|----|----|----|----|----|----|----|----|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |

Implementation Details

Procedure

- 1) Locate IC 74196 on Digital trainer kit
- 2) Apply various inputs to appropriate pins as per the mode of operation with reference to the pin configuration of the IC.
- 3) Connect a pulsar switch to the clock input.
- 4) Verify the respective truth tables for different modes with reference to the truth table given in the data sheet of IC 74194.

Post Lab Subjective/Objective type Questions:

1. What is a universal shift register?
A universal shift register is a digital circuit that combines the capabilities of both serial and parallel shift registers, allowing it to perform input/output operations in both modes. It can store data and shift it towards the right or left, as well as load data in parallel.

2. Prepare a truth table for 3 bit SISO left shift with data 011 along with clock pulse

| clk | A | B | C |
|-----|---|---|---|
| 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 |
| 2 | 0 | 0 | 1 |
| 3 | 0 | 1 | 1 |
| 4 | 0 | 0 | 1 |
| 5 | 0 | 0 | 0 |

3. Can a shift register be used as a counter? Give any one application.
Yes, a shift register can be used as a counter by configuring it in a specific way, typically as a serial-in/serial-out or parallel-in/parallel-out shift register. By using feedback from the output to the input and combining it with a clock pulse, the shift register can cycle through a predefined set of states, effectively counting in binary. A shift register can be configured as a ring counter, where a single logic high ("1") circulates through the register. It is used in sequencing applications like state machines, light chasers, and timing control in microprocessors.
4. How many clock pulses are required to enter a byte of data serially into an 8-bit shift register?
To input data, 8 clock pulses are required and to check the output, 7 clock pulses are required.

Conclusion:

Thus, we have studied SISO, SIPO, PISO, and PIPO shift registers, and have implemented and validated their truth tables

Signature of faculty in-charge with Date: