SOMAIYA VIDYAVIHAR UNIVERSITY
K J Somaiya College of Engineering

K. J. Somaiya College of Engineering, Mumbai-77
(A Constituent College of Somaiya Vidyavihar University)
Department of Computer Engineering

Somaiya TRUST

Course Name:	**Digital Design Laboratory**	**Semester:**	**III**
Date of Performance:	**09 / 08 / 24**	**Batch No:**	**A1**
Faculty Name:		**Roll No:**	**16010123012**
Faculty Sign & Date:		**Grade/Marks:**	**___/25**

Experiment No: 4

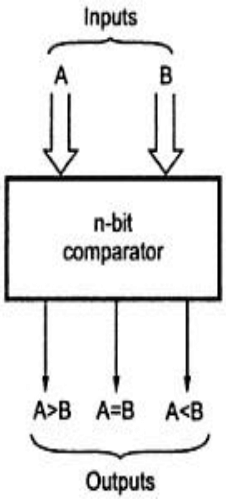
Title: 4-bit magnitude comparator

Aim and Objective of the Experiment:
To design and implement 1-bit comparator using logic gates and verify 4-bit magnitude comparator using IC 7485

COs to be achieved:
CO2: Use different minimization techniques and solve combinational circuits.

Tools used:
Trainer kits

Theory:
Comparator: The comparison of two numbers is an operator that determines one number is greater than, less than (or) equal to the other number. A magnitude comparator is a combinational circuit that compares two numbers A and B and determines their relative magnitude. The outcome of the comparator is specified by three binary variables that indicate whether A>B, A=B (or) A<B.



1-bit Comparator Implementation Details:

Truth Table -

Inputs		Outputs		
B	A	$A > B$	$A = B$	$A < B$
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

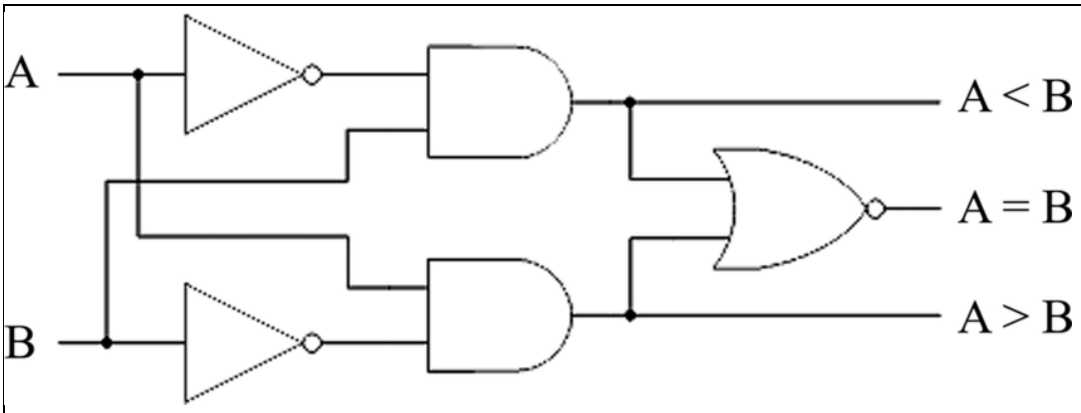
From the Truth Table -

(A<B) = A`B

(A=B) = A`B` + AB

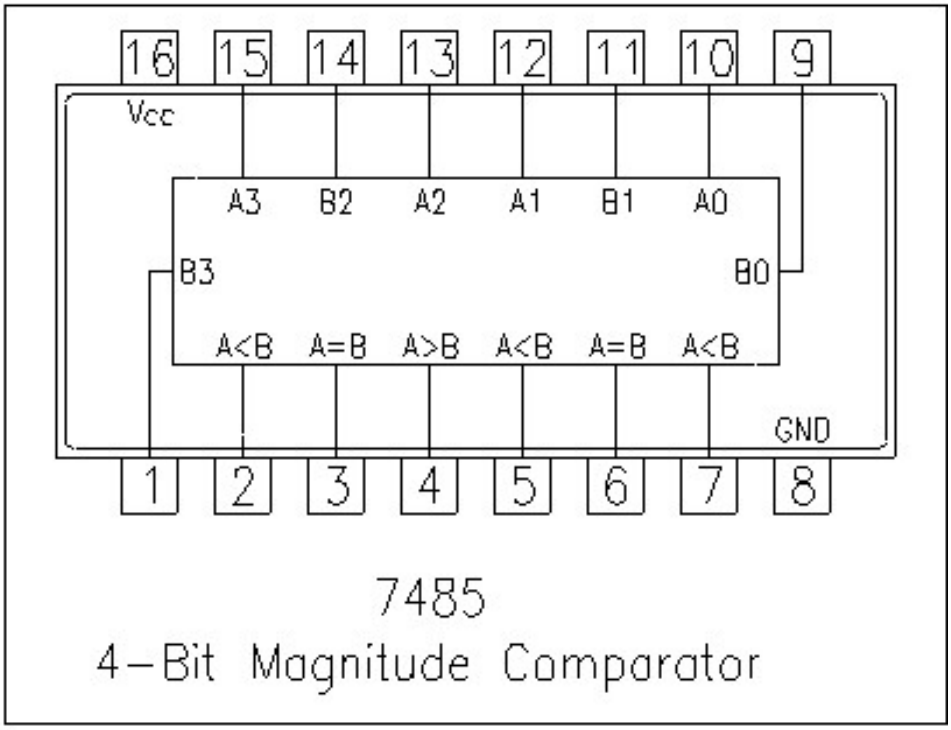
(A>B) = AB`

Logic Diagram of 1-bit Comparator -

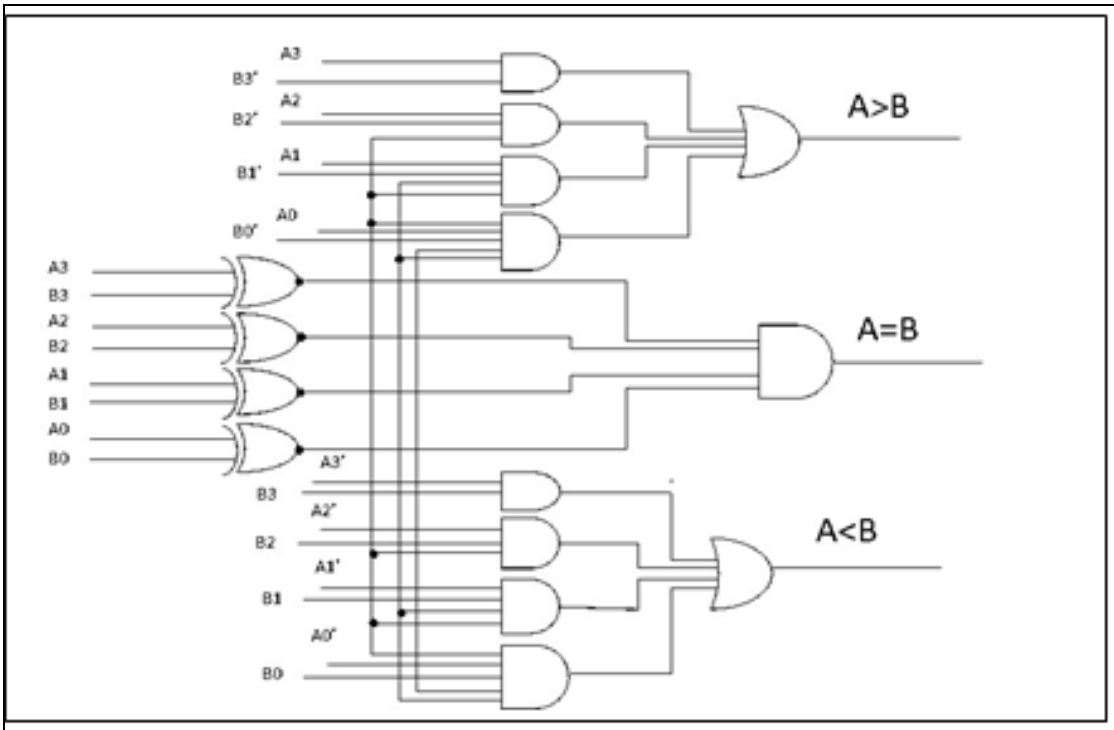


Four Bit Magnitude Comparator Implementation Details:

Pin Diagram of IC 7485



Logic Diagram of IC 7485



Comparing Table

INPUTS of 4 bit Comparator				OUTPUT		
A3, B3	*A2, B2*	*A3, B3*	*A2, B2*	*A3, B3*	*A2, B2*	*A3, B3*
A3 > B3	X	X	X	H	L	L
A3 < B3	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	H	L	L
A3 = B3	A2 < B2	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 >B0	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H

Where H = High Output, L = Low Output, X = Don't Care

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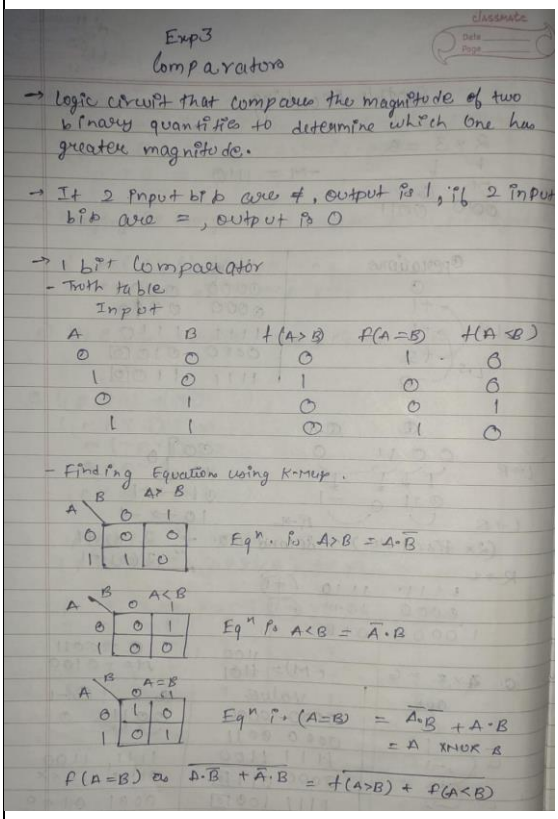
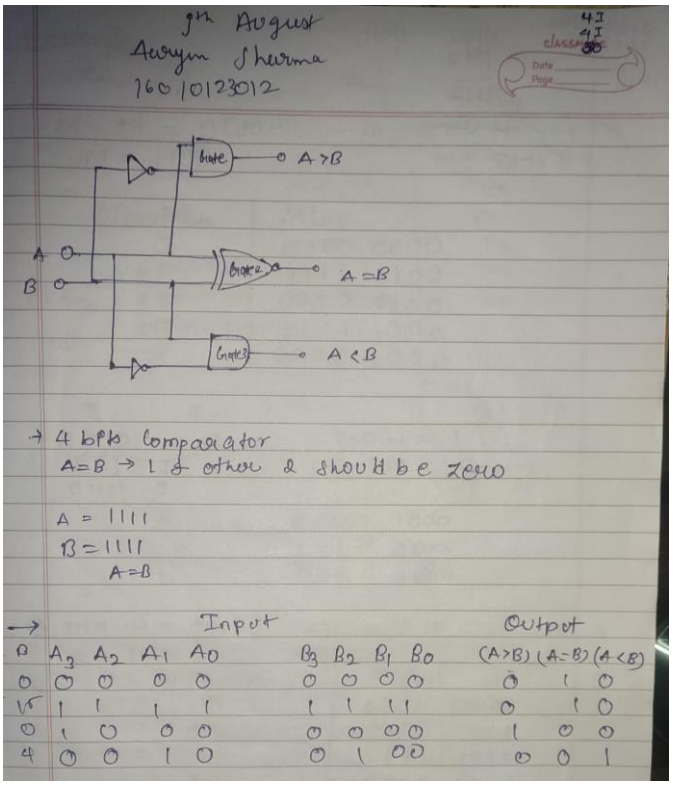
Lab Work –





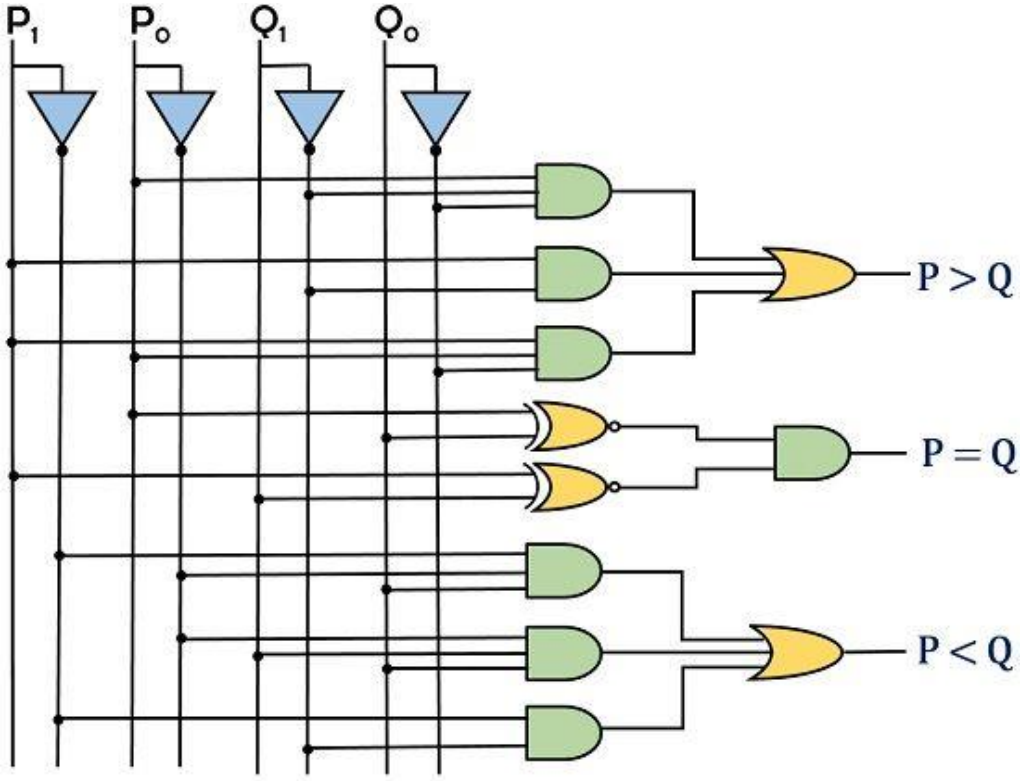
Implementation Details

Procedure:

1) Locate the IC 7485 on the trainer kit.
2) Connect 1st input no. to A3-A0 input slot and 2nd to B3-B0.
3) Connect the output $Y_{A>B}$, $Y_{A<B}$ and $Y_{A=B}$ to the output indicators.
4) Switch ON the power supply and monitor the output for various input combinations.

Post Lab Subjective/Objective type Question

1. Design 2-bit magnitude comparator.



Logic Circuit of 2-bit Magnitude Comparator

Electronics Coach

2. How can we implement 5-bit magnitude comparator using IC 7485.
   We will need two 7485 chips because each can only compare 4 bits. The first 7485 compares the lower 4 bits of the two 5-bit numbers. The output of this first comparison is then fed into the second 7485, which compares the most significant bit (the 5th bit) along with the results from the first chip. This setup allows us to determine whether one 5-bit number is greater than, less than, or equal to the other.
   The process involves connecting the appropriate inputs and cascading the outputs to handle all 5 bits.

3. Virtual Lab for 8 bit digital comparator using Virtual Lab (Digital Logic Design) Perform simulation.
   Virtual Labs (vlabs.ac.in)
   Give feedback for the experiments of virtual lab using somaiya email id.

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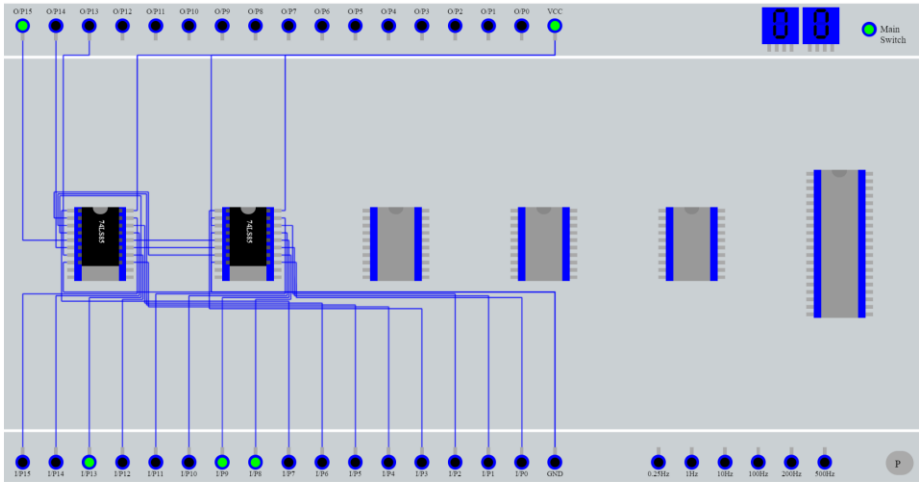
Virtual Labs

Design of 8-bit digital Comparator using MSI ICs



DM74LS85 4-Bit Magnitude Comparators

General Description

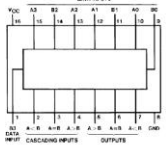
These 4-bit magnitude comparators perform comparison of straight binary or BCD codes. Three fully-decoded decisions about two, 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B, and A = B outputs of a stage handling less-significant bits are connected to the corresponding inputs of the next stage handling more significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the A = B input. The cascading path is implemented with only a two-gate-level delay to reduce overall comparison times for long words.

Features

Typical power dissipation: 52 mW
Typical delay (4-bit words): 24 ns

Connection Diagram

Dual-In-Line Package



Order Number 54LS85DMQB, 54LS85FMQB, 54LS85LMQB, DM54LS85J, DM54LS85W, DM74LS85M or DM74LS85N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Function Table

Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

H = High Level, L = Low Level, X = Don't Care

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage 7V
Input Voltage 7V
Operating Free Air Temperature Range
DM54LS and 54LS −55°C to +125°C
DM74LS 0°C to +70°C
Storage Temperature Range −65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	DM54LS85			DM74LS85			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	(Note 1) Typ	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.8	1.6	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			2.4	4.4	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

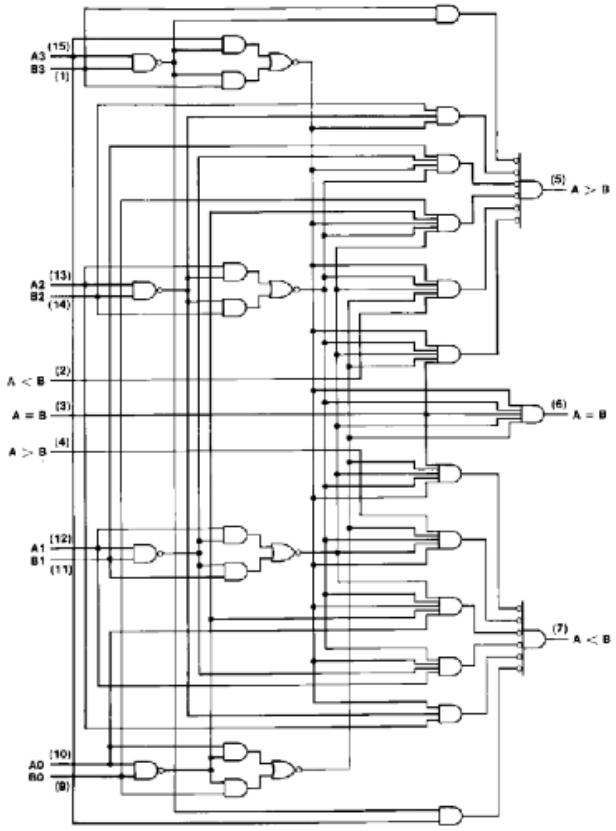
Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	3	10	4	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	10	4	15	ns

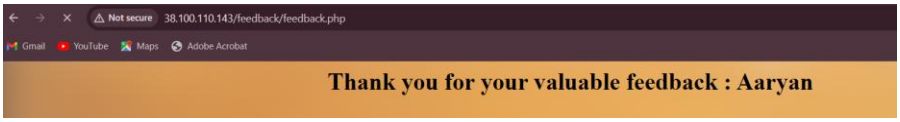
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C
Note 2: No more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From Input	To Output	Number of Gate Levels	R_L = 2 kΩ				Units
					C_L = 15 pF		C_L = 50 pF		
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low-to-High Level Output	Any A or B Data Input	A < B, A > B	3		36		42	ns
			A = B	4		40		40	
t_{PHL}	Propagation Delay Time High-to-Low Level Output	Any A or B Data Input	A < B, A > B	3		30		40	ns
			A = B	4		30		40	
t_{PLH}	Propagation Delay Time Low-to-High Level Output	A < B or A = B	A > B	1		22		26	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output	A < B or A = B	A > B	1		17		26	ns
t_{PLH}	Propagation Delay Time Low-to-High Level Output	A = B	A = B	2		20		25	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output	A = B	A = B	2		17		26	ns
t_{PLH}	Propagation Delay Time Low-to-High Level Output	A > B or A = B	A < B	1		22		26	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output	A > B or A = B	A < B	1		17		26	ns

Logic Diagram





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Conclusion:
We successfully performed and learnt about 1 bit, 2bits and 4bits comparator

Signature of faculty in-charge with Date: