Course Name:	**Digital Design Laboratory**	**Semester:**	**III**
Date of Performance:	**13 / 09 / 2024**	**Batch No:**	**A1**
Faculty Name:	**Bharti Narayan**	**Roll No:**	**16010123012**
Faculty Sign & Date:		**Grade/Marks:**	**___/25**

Date: 12/September/2024

Sub: Smart India Hackathon 2024 – Nomination

I am pleased to nominate the below team from our college to participate in Smart India Hackathon 2024. AISHE code No for our college is U-1085.

Team: MINE MASTERS

	Name	Gender (M/F)	Email id	Mobile no.	Stream	Academic Year
Team Leader	Anuj Madke	M	anuj.madke@somaiya.edu	8424061440	Computer Engineering	Second
Team Member	Ashvatth Joshi	M	ashvatth.j@somaiya.edu	9867651733	Computer Engineering	Second
Team Member	Ritessh Santra	M	ritesh.santra@somaiya.edu	9372450624	Electronics and Computer Engineering	Second
Team Member	Aaryan Sharma	M	aaryan.sharma@somaiya.edu	9004630738	Computer Engineering	Second
Team Member	Sahana G Iyer	F	sahanag.iyer@somaiya.edu	9833901733	Electronics and Computer Engineering	Second
Team Member	Ambuj K. Rai	M	ambuj.rai@somaiya.edu	9326525876	Computer Engineering	Second

I do hereby declare that all the above information given by me are true to the best of my knowledge and belief.

Sincerely,
Dr. S. K. Ukarande
Principal

Experiment No: 7
Title: Asynchronous Counter

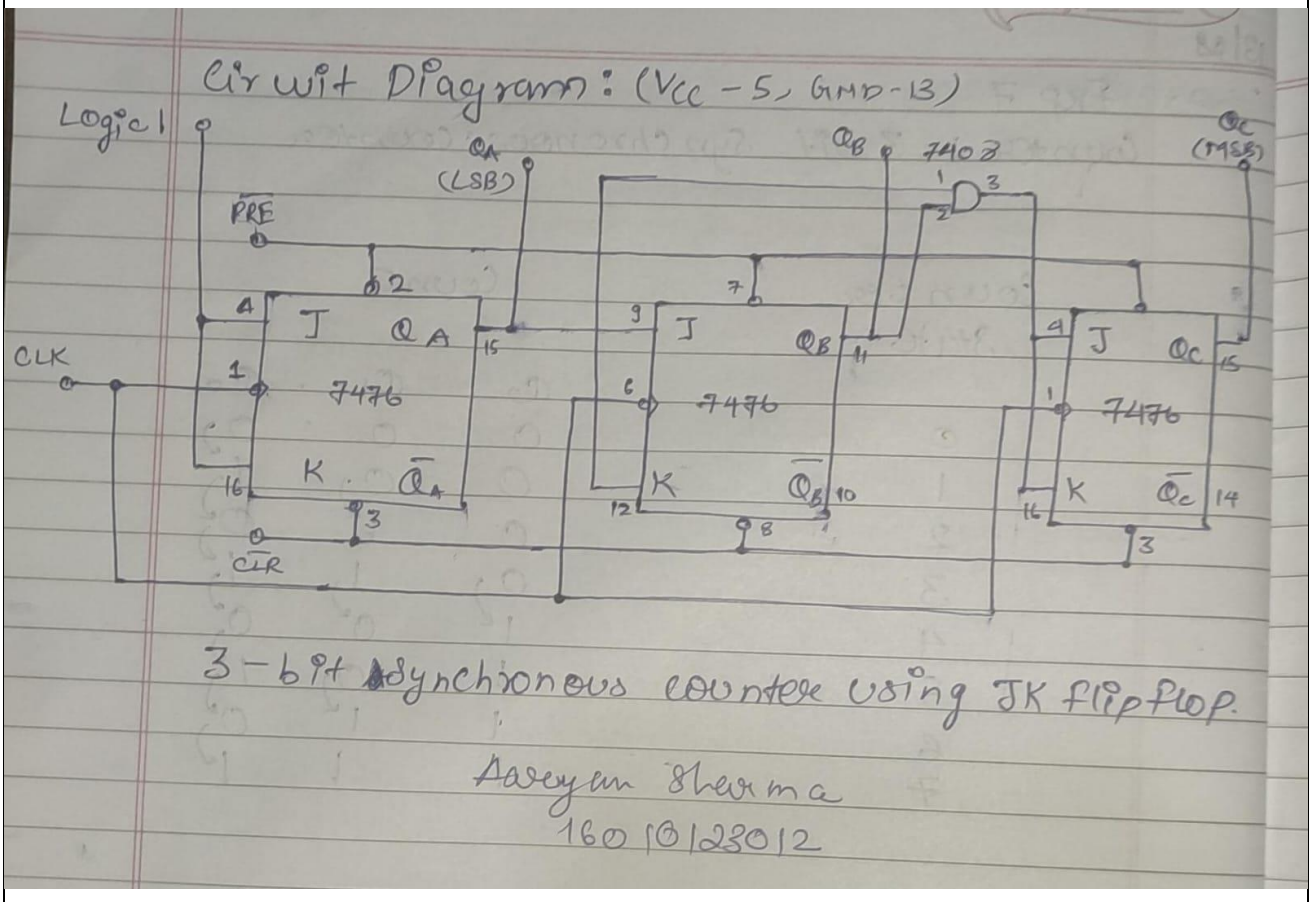
Aim and Objective of the Experiment:
To design and implement 3 bit Asynchronous up counter using JK Flip Flop

COs to be achieved:
CO3: Design synchronous and asynchronous sequential circuits.

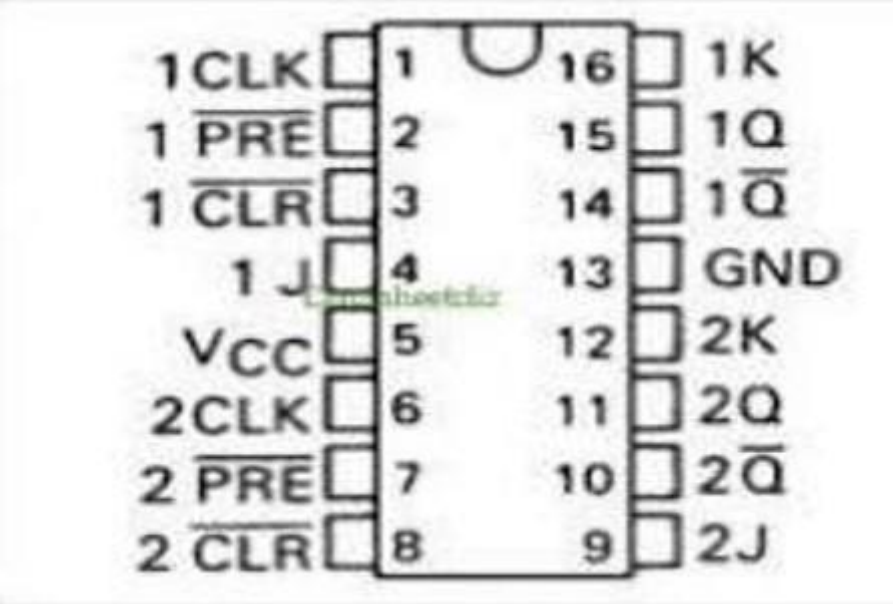
Tools used:
Trainer kits

Theory:

Circuit diagram of 3-bit Asynchronous Up counter using JK FF (IC 7476)



Pin diagram of JK FF (IC 7476)



Implementation Details

Procedure

1) Locate IC 7476 JK FF on Digital trainer kit
2) Apply various inputs to appropriate pins as per the circuit diagram of the 3 bit Asynchronous up counter with reference to the pin configuration of the IC.
3) Make sure of Reset and Clear Pins connections with reference to data sheet information.
4) Connect a pulsar switch to the clock input.
5) Verify the working and prepare a truth table.

Post Lab Subjective/Objective type Questions:

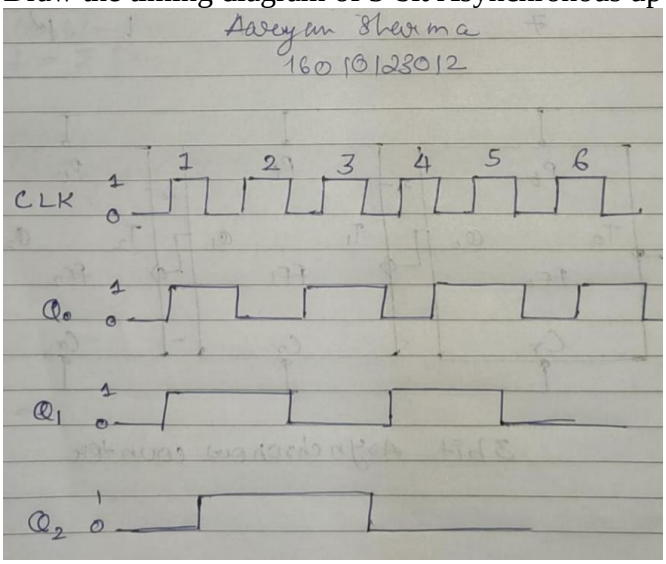
1. How JK FF need to be configured to use for counter operation?
   To configure a JK flip-flop for counter operation, set J and K inputs to HIGH, provide a clock signal, and optionally connect multiple flip-flops in series for a multi-bit counter. We need to ensure that we handle the Clear and Pre-set inputs appropriately to avoid unintended resets or pre-setting's.

2. What changes are required to use the same counter as 3-bit asynchronous down counter?
   To convert a 3-bit asynchronous counter into a down counter:

1. **Invert the Clock Signal:** Use NOT gates to invert the clock signal for each flip-flop, ensuring they toggle on the falling edge of the previous flip-flop's output.
2. **Set J and K Inputs to HIGH:** Ensure both J and K inputs are HIGH to enable toggling mode.

3. **Connect Flip-Flops in Series:** Each flip-flop's clock input should be driven by the inverted Q output of the preceding flip-flop.
   This configuration will allow the 3-bit counter to count downwards with each clock pulse.

3. Draw the timing diagram of 3-bit Asynchronous up counter.



4. What is mod n concept used in counters?
   The mod n concept is crucial for designing counters in digital electronics, as it defines the range of counts the counter can perform before rolling over. Understanding the modulus helps in choosing the right type of counter for a given application and in designing circuits that meet specific counting requirements.

5. For Mod-5 counter how many JK FFs are required?
   For a mod-5 counter, you need 3 JK flip-flops. The additional logic is required to manage the reset condition so that the counter only counts from 0 to 4 and then starts over.

Conclusion:

We have successfully completed this experiment and learned how to make a 3-bit asynchronous counter using JK flip flops.

Signature of faculty in-charge with Date: