Course Name:	**Digital Design Laboratory**	**Semester:**	**III**
Date of Performance:	**25 / 10 / 2024**	**Batch No:**	**A1**
Faculty Name:	**BHARATI NARAYAN**	**Roll No:**	**16010123012**
Faculty Sign & Date:		**Grade/Marks:**	**___/25**

Experiment No: 8
Title: 1-bit adder on VHDL

Aim and Objective of the Experiment:
To implement 1-bit adder on VHDL

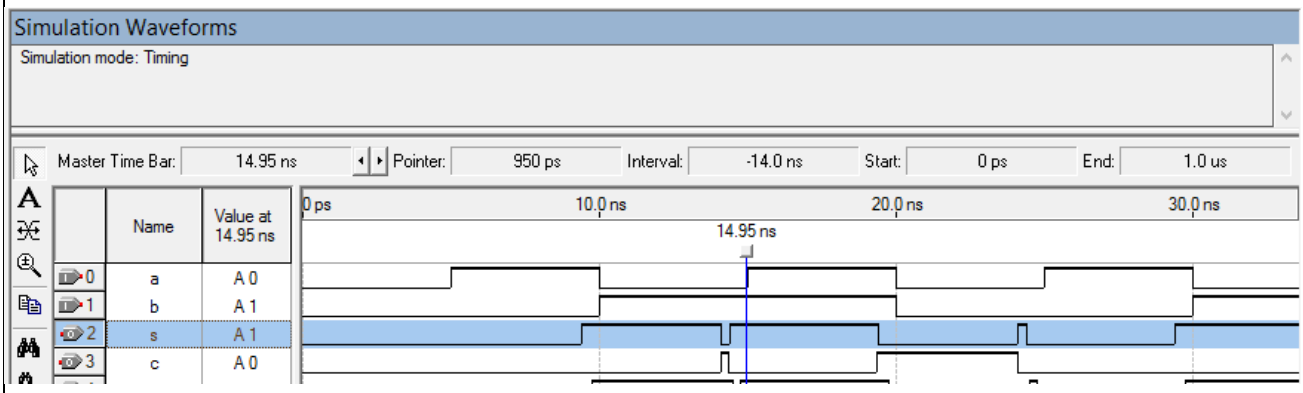
COs to be achieved:
CO4: Implement digital networks using VHDL

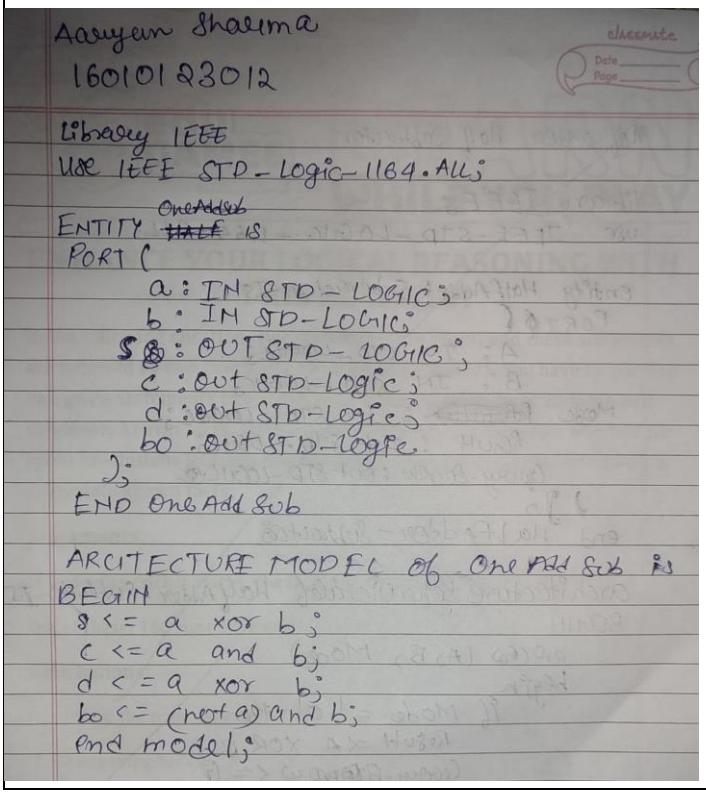
Tools used:
Quartus, ModelSim

Theory:
A 1-bit adder, a fundamental component of digital circuits, performs binary addition of two 1-bit numbers. It utilizes logic gates to generate the sum and carry-out outputs. A half-adder adds two bits without considering the carry from the previous stage, while a full-adder accounts for the carry input. Using VHDL, a hardware description language, the 1-bit adder can be designed as a combinational circuit. VHDL facilitates the creation of a structural and behavioral description of the adder. In practice, this simple unit serves as a building block for constructing larger multi-bit adders, enabling arithmetic operations in microprocessors and digital systems.

Implementation Details
library IEEE; use IEEE.STD_LOGIC_1164.ALL; entity OneAddSub is   Port (

```
a : in STD_LOGIC;
b : in STD_LOGIC;
s : out STD_LOGIC;
c : out STD_LOGIC
);
end OneAddSub;
architecture Behavioral of OneAddSub is
begin
s <= a XOR b;
c <= a AND b;
end Behavioral;
```





```
Aaryan Sharma
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Library IEEE
USE IEEE STD_LOGIC_1164.ALL;
ENTITY OneAddSub IS
PORT (
    a : IN STD_LOGIC;
    b : IN STD_LOGIC;
    s : OUT STD_LOGIC;
    c : out STD_LOGIC;
    d : out STD_LOGIC;
    bo : OUT STD_LOGIC
);
END OneAddSub

ARCHITECTURE MODEL of OneAddSub is
BEGIN
s <= a xor b;
c <= a and b;
d <= a xor b;
bo <= (not a) and b;
end model;
```

Post Lab Subjective/Objective type Questions:

1. How can 1-bit adder be used to implement a 4-bit adder?
   To create a 4-bit adder using 1-bit adders, you can connect four 1-bit adders in sequence. Each 1-bit adder accepts two single-bit inputs along with a carry-in (except for the first one, which doesn't need it) and produces a sum and a carry-out.
   The carry-out from each 1-bit adder is linked to the carry-in of the next higher bit's adder. Each 1-bit adder sums the corresponding bits from two 4-bit numbers (A and B), along with any carry from the previous bit position. The final carry-out from the fourth 1-bit adder indicates an overflow if the result exceeds 4 bits. This arrangement of 1-bit adders allows us to construct an n-bit adder by chaining together n individual 1-bit adders.

2. What is VHDL used for?
   VHDL (VHSIC Hardware Description Language) is mainly utilized for designing, modeling, simulating, and implementing digital systems, especially complex integrated circuits (ICs) such as FPGAs and ASICs. It allows designers to describe the structure and behavior of digital circuits at various abstraction levels, ranging from high-level behavioral descriptions to detailed gate-level implementations. VHDL is widely employed in electronic design automation (EDA) for the development and testing of digital logic.

Conclusion:

In this experiment, we successfully created a 1-bit adder using VHDL, showcasing key principles of digital design and hardware description languages. This work emphasizes the significance of VHDL in digital design, as it enables accurate structural and behavioral modeling of circuits like adders, which are crucial components of more complex digital systems.

Signature of faculty in-charge with Date: