Tutorial 8:

1. $t_p = \max\{t_{p_i}\} + d$
   $= 90 + 10$
   $= 100$ ns.

   a. $(K+n-1) \cdot t_p$
   $= (4+1000-1) \cdot 100$
   $= 100300$ ns.

   b. $n \cdot t_n$
   $= 1000 \cdot (60+50+90+80)$
   $= 1000 \cdot 280$
   $= 280000$ ns.

   c. Throughput for pipelined execution
   = no. of instructions executed per unit time
   $= 1000 / 100300$ task/ns.
   $= 0.01$ task/ns.

2. $t_p = \max(150, 120, 160, 140) + 5$
   $= 165$ ns.
   $n = 1000 \quad K = 4 \quad \therefore$ total time $(1000+4-1) \cdot 165$
   $= 1003 \cdot 165$
   $= 165495$ ns
   $= 165.5$ μs

3. for four stage $t_{p_4} = \max(800, 500, 400, 300) + \text{delay}$
   $= 800 + 0 = 800$ picoseconds
   So execution time for 1 instruction = 1 clock cycle = 800 pico sec
   for two stage $t_{p_2} = \max(600, 350) + \text{delay}$
   $= 600 + 0 = 600$ picoseconds
   Execution time for 1 instruction = 600 picoseconds
   Throughput for 4 stage = 1 instruction / 800 ns.
   " " 2 stage = 1 instruction / 600 ns.

So increase $1/600 - 1/800$

So % of increase with respect to the previous one

$$\left(\frac{1/600 - 1/800}{1/800}\right) \times 100\ \%$$

$$= \left(\frac{200}{600 \times 800} \times 800\right) \times 100\ \%$$

$$= 33.33\ \%$$

4. cycle time in designing D1 = max(3,2,4,2,3) + delay

= 4 + 0 = 4 ns.

Execution time for 100 instructions in design D1.

= (K+n-1) · 4

= (5+100-1) · 4

= 416 ns.

Execution time for 100 instruction in design D2

= (K+n-1) · 2

= ~~208 ns~~

= (8+100-1) · 2

= 214 ns.

[cycle time = 2+0 → delay = 2ns.

So time saved = (416 - 214) = 202 ns.

5. P1 → cycle time = max (1,2,2,1) + delay = 2 ns

clock freq. = 1/2 = 0.5 GHz.

P2 → clock freq. = 1/max(1, 1.5, 1.5, 1.5) = 1/1.5 = 0.67 GHz

P3 → " = 1/max (0.5, 1, 1, 0.6, 1) = 1/1 = 1 GHz

P4 → " = 1/max (0.5, 0.5, 1, 1, 1.1) = 1/1.1 = 0.91 GHz.

so P3 has highest clock freq.