Home Assignment 2
Due Date(22-04-2019)

Q 1. Draw the gate diagram, write state table, characteristic table and excitation table for the S-R(with NAND gate), D, J-K, T flip flop.

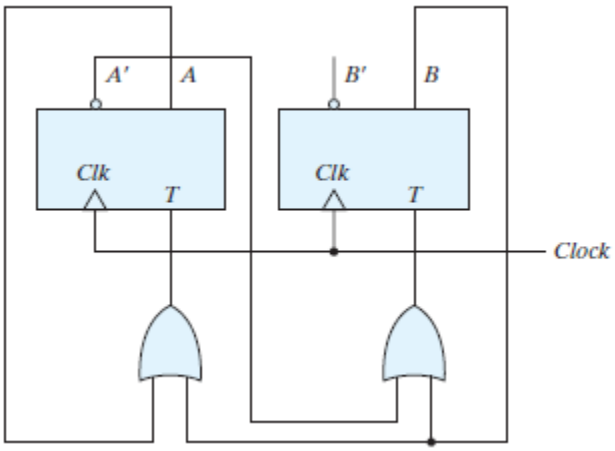
Q 2. Convert D flip flop to J-K flip flop. (Design J-K flip flop using D flip flop).

Q 3. Convert D flip flop to T flip flop.

Q 4. Convert S-R flip flop to J-K flip flop.

Q 5. Explain the differences among a truth table, a state table, a characteristic table, and an excitation table. Also, explain the difference among a Boolean equation, a state equation, a characteristic equation, and a flip-flop input equation.

Q 6. Derive the state table and the state diagram of the sequential circuit shown in Figure.



Q 7. Make 4 bit asynchronous UP/Down counter in single unit.

Q 8. Design synchronous counter for the following sequence using T flip flop:

0 – 4 – 8- 12 – 1 – 5 – 9 – 13- 2- 6- 10 – 14- 3- 7- 11- 15-0

Q 9. Design 4 bit SISO, PIPO register using D flip flop.

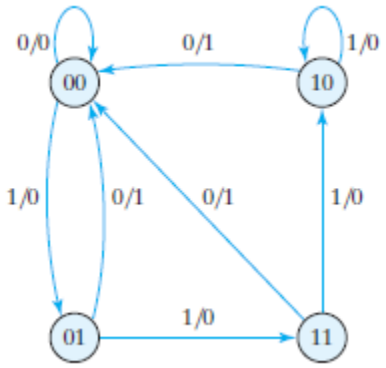
Q 10. Design BCD Ripple counter (Asynchronous counter). (Mod- 9 counter)

Q 11. Design 4 bit Mod -12 asynchronous counter.

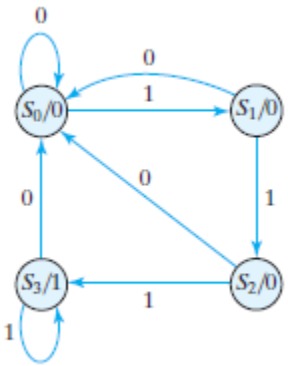
Q 12. Draw the circuit of johnson counter. (self study)

Q 13. Determine the state transitions and output sequence that will be generated when an input sequence of 010110 is applied to the circuit and it is initially in the state 00.

Design Hardware for the following state diagram.



Q 14. Design hardware for the following moore state machine using D flip flop.



Q 15. What is the main difference between an **initial** statement and an **always** statement in Verilog HDL?

Q 16. Write Verilog code for q7, q8, q11, q14.