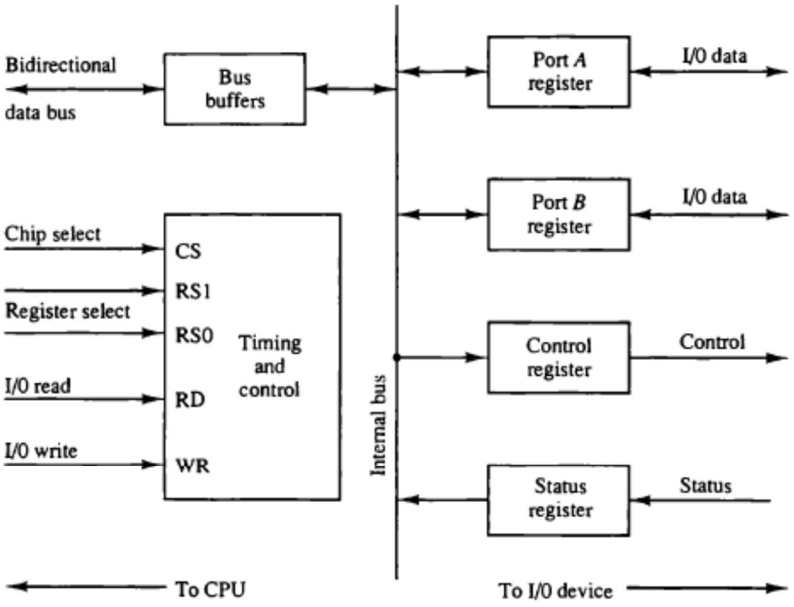
TUTORIAL 10

1.



CS	RS1	RS0	Register selected
0	×	×	None: data bus in high-impedance
1	0	0	Port *A* register
1	0	1	Port *B* register
1	1	0	Control register
1	1	1	Status register

The addresses assigned to the four registers of the I/O interface of the above figure are equal to the binary equivalent of 12, 13, 14, and 15. Show the external circuit that must be connected between an 8-bit I/O address from the CPU and the CS, RS1, and RS0 inputs of the interface.

2. Six interfaces of the type shown in the previous figure, are connected to a CPU that uses an I/O register of eight bits. Each one of six chip select (CS) inputs is connected to a different address line. Thus, the high-order address line is connected to the CS input of the first interface unit and the sixth address line is connected to the CS input of sixth interface unit. The two low-order address lines are connected to RS1 and RS0 of all six interface units. Determine the 8-bit address of each register in each interface.

3. Information is inserted into a FIFO buffer at a rate of m bytes per second. The information is deleted at a rate of n bytes per second. The maximum capacity of the buffer is k bytes.

   a. How long does it take for an empty buffer to fill up when m > n?

   b. How long does it take for a full buffer to empty when m < n?

   c. Is the FIFO Buffer required if m = n?

4. How many characters per second can be transmitted over a 1200-baud line in each of the following modes? (A character code consists of 8 bits.)

   a. Synchronous serial transmission.

   b. Asynchronous serial transmission with two stop bits.

   c. Asynchronous serial transmission with one stop bit.

5. A CPU with a 20 MHz clock is connected to memory unit whose access time is 40 ns. Formulate a read and write timing diagrams using a READ strobe and a WRITE strobe. Include the address in the timing diagram.