Tut 3:

1. a. Memory capacity 2048 bytes.
one RAM chip size 128 X 8
So Reqd. no. of RAM chip = $\frac{2048}{128}$ = 16 chips.

b. $2048 = 2^{11}$ ∴ 11 address bus lines should be used to access 2048 bytes.
each RAM chip of size 128 X 8 ⇒ $128 = 2^7$.
so 7 address lines will be common to ~~each~~ all chips.

c. total no. of lines of address bus = 11.
common no. to ~~ea~~ all the chips 7.
So 4 lines must be decoded for chip select
there are 16 chips.
So 4 X 16 decoder needs to be used.

2. The cache consists of 64 lines.
64 lines are divided into four line sets.
So, in 1 set there are four-lines.
∴ 4 lines in 1 set.
So 64 lines in $\frac{1}{4} \times 64 = 16$ sets.
So the cache is divided into 16 sets of 4 lines each.
So 4 bits are required to identify the set no.
Now main memory consists of 4K blocks = $2^2 \cdot 2^{10}$
$= 2^{12}$ blocks
So total address lines = 12.
4 bits are required to identify set no.
So length of tag field = 12 - 4 = 8.
each word length $128 = 2^7$.
So 7 bits are required to specify the word.

∴ Main memory address =

Tag	set	word
8	4	7

3. Match logic for one word

$$M_i = \prod_{j=1}^{n} (A_j F_{ij} + A_j' F_{ij}' + K_j')$$

$$= \prod_{j=1}^{n} [(A_j \oplus F_{ij})' + K_j']$$

So, $M_i' = \sum_{j=1}^{n} (A_j \oplus F_{ij}) \cdot K_j$ [Match logic complement for all the words of Associative Memory