Tutorial 4 (Don't Care, Decoder)

ECSE104L

1. Simplify the following Boolean function F, together with the don't-care conditions d.
   a. F (A,B,C,D) = ∑(0, 6, 8 13, 14)
      d(A,B,C,D) = ∑(2,4,10)

   b. F (A,B,C,D) = ∑(2,4,7, 10,12)
      d(A,B,C,D) = ∑(0,6,8)

2. Draw the logic diagram for the following Verilog description and convert into behavioural Verilog code

```
module Circuit_A (A, B, C, D, F);
input A, B, C, D;
output F;
wire w, x, y, z, a, d;
    or (x, B, C, d);
    and (y, a ,C);
    and (w, z ,B);
    and (z, y, A);
    or (F, x, w);
    not (a, A);
    not (d, D);
endmodule
```

3. Design BCD to Excess-3 Code decoder truth table is as follows

Truth Table for Code Conversion Example

Input BCD	Output Excess-3 Code
A B C D	**w x y z**
0 0 0 0	0 0 1 1
0 0 0 1	0 1 0 0
0 0 1 0	0 1 0 1
0 0 1 1	0 1 1 0
0 1 0 0	0 1 1 1
0 1 0 1	1 0 0 0
0 1 1 0	1 0 0 1
0 1 1 1	1 0 1 0
1 0 0 0	1 0 1 1
1 0 0 1	1 1 0 0