

# CS-2110 A/B/C Quiz 2 (C)

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TOTAL POINTS

**100 / 100**

QUESTION 1

1 1A 4 / 4

✓ + 4 pts Correct (D)

+ 0 pts incorrect

QUESTION 2

2 1B 4 / 4

✓ + 4 pts Correct (B)

+ 0 pts Incorrect

QUESTION 3

3 1C 6 / 6

Addressability = 40

✓ + 2 pts 40

+ 1 pts 5 bytes

Address Space = 128

✓ + 2 pts 128

+ 1 pts  $2^7$

Total Memory = 640

✓ + 2 pts 640 bytes

+ 1 pts  $2^7 * 5$  bytes,  $2^7 * 40$  bits, 5120 bits

+ 0 pts incorrect

QUESTION 4

4 1D 4 / 4

✓ + 4 pts Correct (all x's)

+ 0 pts incorrect

QUESTION 5

1E 8 pts

5.1 1Ei 4 / 4

✓ + 2 pts Correct (No)

✓ + 2 pts Explanation\*\* must\*\* state that a larger grouping can be made or writing down the simplified boolean expression.

+ 0 pts incorrect

5.2 1Eii 4 / 4

✓ + 2 pts Correct (No)

✓ + 2 pts Explanation\*\* must\*\* state that a larger grouping can be made or writing down the simplified boolean expression.

+ 0 pts incorrect

QUESTION 6

1f 24 pts

6.1 1Fi 4 / 4

✓ + 2 pts Correct (True)

✓ + 2 pts Explanation describes the correct components that are used to build a flip-flop in any reasonable way. \*\*(Also give full points if they state False and we can use one less NOT gate by using Q' as input to second latch).\*\*

+ 0 pts incorrect

## 6.2 1Fii 4 / 4

- ✓ + 2 pts Correct (True)
- ✓ + 2 pts Explanation mentions one of the following:
  - Synchronization
  - Ensure we do not skip through states
  - Any other valid reasoning related to edge triggered logic
- + 0 pts incorrect

## 6.3 1Fiii 4 / 4

- ✓ + 2 pts Correct (False)
- ✓ + 2 pts Explanation must state one of the following:
  - Gated D latches are level triggered
  - Only updates on a high level
  - Any other valid reasoning
- + 0 pts incorrect

## 6.4 1Fiv 4 / 4

- ✓ + 2 pts Correct (True)
- ✓ + 2 pts Explanation must state one of the following:
  - We need 6 bits to represent 37 states
  - 6 bits can only represent 64 states at most
  - or any other valid reasoning
- + 0 pts incorrect

## 6.5 1Av 4 / 4

- ✓ + 2 pts Correct (False)
- ✓ + 2 pts Explanation states at least one of the following:
  - Sequential logic depends on current and past inputs
- + 0 pts incorrect

## 6.6 1Fvi 4 / 4

- ✓ + 2 pts Correct (False)
- ✓ + 2 pts Explanation must state that a gated d-latch only has two inputs: WE and data \*\*(must include what the two inputs are)\*\*
  - + 0 pts incorrect
  - + 4 pts True with explanation that the names of the input do not matter and could also be WE and D

## QUESTION 7

### 7 2A 6 / 6

- ✓ + 6 pts Fully Correct (by row)
  - 0 1 1
  - 0 0 1
  - 1 0 0
  - 0 1 0
  - 1 1 1
  - 1 0 1
  - 0 1 0
  - 1 0 0
- + 5.25 pts 1 incorrect row
- + 4.5 pts 2 incorrect rows
- + 3.75 pts 3 incorrect rows
- + 0 pts 4 or more rows incorrect

## QUESTION 8

### 8 2B 9 / 9

- KMAP (N1)
- ✓ + 3 pts Fully correct (by row)
    - 0 0 1 1
    - 1 0 0 1
  - + 2 pts one cell incorrect
  - + 1 pts two cells incorrect

+ 0 pts 2+ incorrect

KMAP (NO)

✓ + 3 pts Fully correct

- 1 0 0 0

- 0 1 0 1

+ 2 pts one cell incorrect

+ 1 pts two cells incorrect

+ 0 pts 2+ incorrect

KMAP (Output)

✓ + 3 pts Fully correct

- 1 1 1 0

- 1 1 1 0

+ 2 pts one cell incorrect

+ 1 pts two cells incorrect

+ 0 pts 2+ incorrect

+ 0 pts incorrect

QUESTION 9

9 2C 10 / 10

Sum of products

✓ + 5 pts Fully correct ( $AC' + BC'D + A'B'CD + BCD'$ )

+ 2.5 pts one mistake

+ 0 pts incorrect

Circuit

✓ + 5 pts Fully correct (matches SOP, \*\*propagate errors\*\*)

!/[IMG\_F236040BED55-1.jpeg](!/files/17ced4a3-6f39-4ba9-9da4-e77498473fd)

+ 1 pts OR4 gate

+ 4 pts All AND gates match SOP

+ 3 pts 3 AND gates match SOP

+ 2 pts 2 AND gates match SOP

+ 1 pts 1 AND gate matches SOP

+ 0 pts incorrect

QUESTION 10

10 3A 5 / 5

✓ + 5 pts Correct (Fully correct)

!/[IMG\_4944177E8769-1.jpeg](!/files/eb1842b0-092b-4725-991b-0bc9a462ef60)

- 1 pts Uses \_bubbles\_ instead of inverter

- 1 pts connects Q' instead of Q to output

- 2 pts write enabled should not be inverted

- 2 pts forgets NOT gate

+ 0 pts very incorrect or use gates other than NAND2 and NOT

QUESTION 11

11 3B 7 / 7

✓ + 7 pts Correct

!/[IMG\_61DCEBABA1FD-1.jpeg](!/files/805b2f7d-8ac1-4e2d-8e5c-2b488147c5fc)

+ 6 pts one error

+ 5 pts two errors

+ 4 pts three errors

+ 0 pts 3+ errors

QUESTION 12

12 3C 6 / 6

Groupings

✓ + 3 pts Fully correct

(/files/4d22858d-b2c4-4627-984e-31b1612000d0)

- + 2 pts one incorrect/extraneous grouping
- + 1 pts two incorrect/extraneous groupings

SOP

✓ + 3 pts correct ( $AB' + AC + A'BD$ ) or correct  
translation based on groupings

- + 0 pts incorrect translation from kmap  
groupings
- + 0 pts incorrect

QUESTION 13

13 3D 7 / 7

Groupings

✓ + 4 pts Fully correct

(/files/7d97a1c5-a521-46db-a5d6-1707766e7e90)

- + 3 pts one incorrect/extraneous grouping
- + 2 pts two incorrect/extraneous groupings

SOP

✓ + 3 pts correct ( $B'D' + A'C'D' + A'CD$ ) or correct  
translation based on groupings

- + 0 pts incorrect translation from kmap  
groupings
- + 0 pts incorrect

Your Initials: AP

Name [PRINT CLEARLY]: AARYAN POTDAR

GT username (e.g. gburdell3): apotdar 31

CS 2110: Computer Organization and Programming  
Gupta/Conte/Adams Fall 2023

QUIZ 2  
VERSION C

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of honor and integrity by refusing to betray the trust bestowed  
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[MUST sign:] DalP

- THIS IS A CLOSED BOOK, CLOSED NOTES EXAM
- NO CALCULATORS
- This examination handout has **9** pages.
- Do all your work in this examination handout.
- Only the front of exams sheets will be scanned. Do **not** write your answer on the back of the exam sheets.
- Please write your initials at the top of each page
- WHERE NEEDED, SHOW ALL YOUR INTERMEDIATE RESULTS TO RECEIVE FULL CREDIT

*In case you forgot, here  
are some good facts to  
know:*

| Hex | Dec    |
|-----|--------|
| 1   | 2      |
| 2   | 4      |
| 3   | 8      |
| 4   | 16     |
| 5   | 32     |
| 6   | 64     |
| 7   | 128    |
| 8   | 256    |
| 9   | 512    |
| 10  | 1024   |
| 11  | 2048   |
| 12  | 4096   |
| 13  | 8192   |
| 14  | 16,384 |
| 15  | 32,768 |
| 16  | 65,536 |

| Problem | Points | Score |
|---------|--------|-------|
| 1       | 50     |       |
| 2       | 25     |       |
| 3       | 25     |       |
| TOTAL   | 100    |       |

*More good facts to  
know:*

$$\begin{aligned}1K &= 2^{10} \\1M &= 2^{20} \\1G &= 2^{30} \\1T &= 2^{40} \\1P &= 2^{50} \\1E &= 2^{60}\end{aligned}$$

GOOD LUCK!

1. [50 pts] Answer the following short questions. Show your work (where needed) to receive full credit.

(a) At approximately which of the times below would a ~~D-latch~~'s output change to the value 0? Assume the flip-flop initially stores a 1. (Circle your answer)

(1a) Ans: (flip-flop)

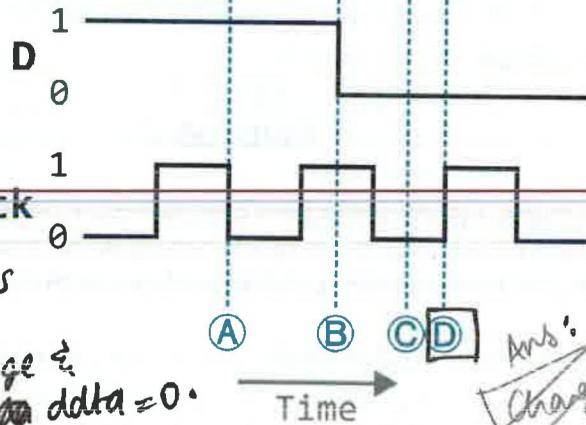
Assuming the flip flop is activated by rising edge,

Value change to 0 at Clock

time = D. Note: Flip-flops

are edge-triggered.

at D, there is a rising edge & data = 0.



Circle one: Time=(A), Time=(B), Time=(C), or Time=(D)

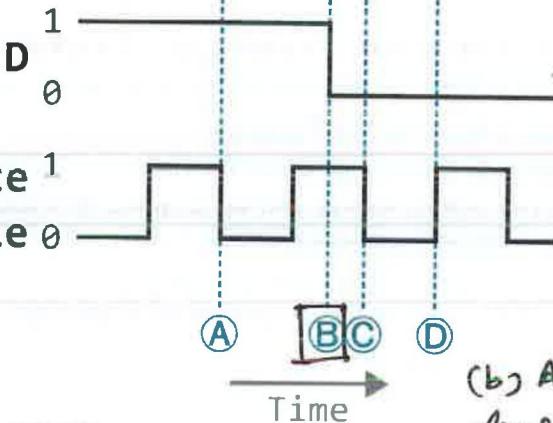
~~GATED~~

(b) At approximately which of the times below would a D ~~latch~~'s output change to the value 0? Assume the latch initially stores a 1. (Circle your answer)

~~D flip flops are edge triggered.~~

Ans. Value change

Write Enable



Circle one: Time=(A), Time=(B), Time=(C), or Time=(D)

Note if flip flop  
is rising edge-triggered  
then the 0  
will be recorded  
at time=D

(b) Ans: Gated D-latches are level triggered. Value in  
clock changes to 0 at  
time = B →

(c) You have acquired a new laptop for college. Your new computer uses 7-bit addresses, and each address points to 5 bytes. Please answer the following about the memory in your new computer (write a decimal number): (Please pay attention to units)

$$5 \text{ bytes} = 5 \times 8 \\ = 40 \text{ bits}$$

Addressability: 40 bits

WE is level at 1  
& Data changes to 0  
(level triggered)

$$2^7 \text{ locations} \\ = 128$$

Address space: 128 locations

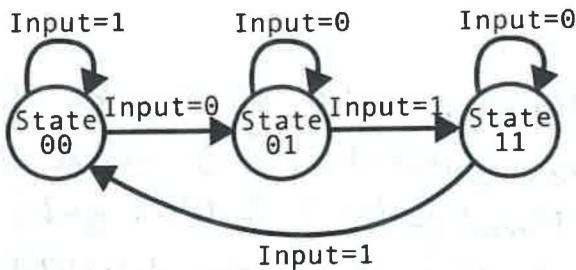
$$\text{Total Memory} = \frac{128 \times 40}{8} = 128 \times 5 \\ = 640 \text{ bytes}$$

$$128 \times 5 = 640$$

2

$$= \frac{5 \cdot 2^3 \cdot 2^7}{2^3} = 5 \cdot 2^7 = 640$$

(d) Fill in the missing last 4 cells of the truth table for the following state machine to ensure a minimal logical expression *could* be found with a K-map. N1 and N0 are the next state bits.



| S1 | S0 | Input | N1 | N0 |
|----|----|-------|----|----|
| 0  | 0  | 0     | 0  | 1  |
| 0  | 0  | 1     | 0  | 0  |
| 0  | 1  | 0     | 0  | 1  |
| 0  | 1  | 1     | 1  | 1  |
| 1  | 0  | 0     | X  | X  |
| 1  | 0  | 1     | X  | X  |
| 1  | 1  | 0     | 1  | 1  |
| 1  | 1  | 1     | 0  | 0  |

*Hint: You do NOT need to solve a K-map to answer this question.*

Reason:  
10 state (where  $S1=1 \wedge S0=0$ ) is never reached in the state machine.  
To find minimum logic expr. w/ Kmap, we fill these w/ Xs as we don't care of them.

(e) Will the following K-map groupings produce a minimal logical expression? Why or why not?

B'C' B'C BC BC'

|    |   |   |   |   |
|----|---|---|---|---|
| A' | 0 | 1 | 1 | 0 |
| A  | 1 | 1 | 1 | 1 |

$A + A'C \rightarrow$  actual solution:  $A + C$

(2) Will these two groupings produce a minimal logical expression? Why or why not?

Your answer:

No, you need the (largest  $2^2$ ) grouping possible. We can make a group of 4 ( $2^2$ ) with Red box. However, it's not the case here, so we won't get minimal expression.

B'C' B'C BC BC'

|    |   |   |   |   |
|----|---|---|---|---|
| A' | 0 | 1 | 1 | 0 |
| A  | 0 | 1 | 1 | 0 |

Your answer:

We have Two groups. The largest grouping would be 1 group of 4 giving the solution:  $C = \overline{C}$ . However,

Current selection gives soln:  $B'C + BC$

$$= C \cdot (B' + B) = C(1)$$

$$= C$$

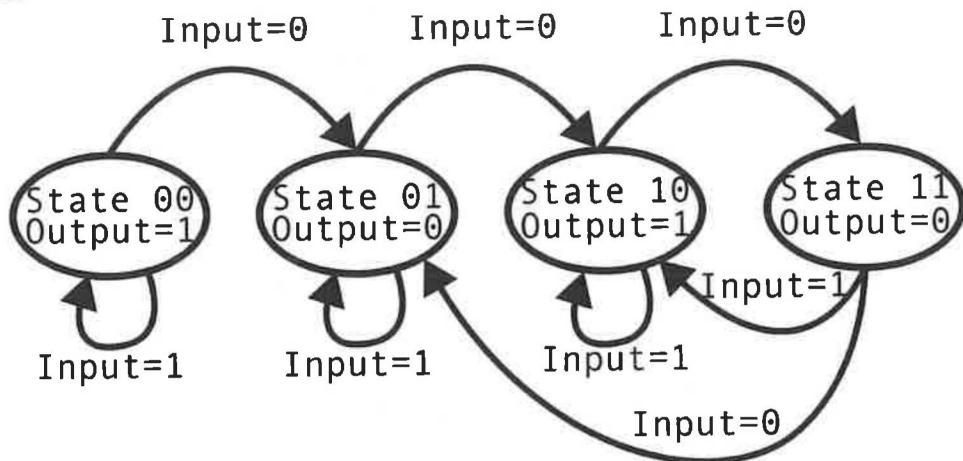
$\therefore$  We get min. log. expression with simplification as seen above.

(f) Answer the following true/false questions by circling "true" or "false," and then give a reason for each answer:

|   |   |
|---|---|
| <input checked="" type="radio"/> TRUE<br>TRUE or FALSE  | I can build a flip-flop with 2 RS latches along with 3 NOT gates and 4 NAND gates. Why or why not?<br><br>A flip-flop consists of 2 gated D latches $\not\equiv$ 1 Not gate.<br>each gated-D latch is made of 1 RS-latch $\not\equiv$ 2 NAND gates $\not\equiv$ 1 NOT gate.<br>Total = 2 RS latches + 4 NAND gates + 3 NOT Gates. |
| <input checked="" type="radio"/> TRUE<br>TRUE or FALSE  | The clock signal and edge-triggered logic are useful for building state machines. Why or why not?<br><br>Clock signal & edge-triggered logic can be used to simultaneously change the states of machines/system. They are composed of sequential logic required for state machines.   |
| <input type="radio"/> FALSE<br>TRUE or FALSE            | Gated D Latches are edge-triggered. Why or why not?<br><br>Gated D latches are edge-triggered. They are level triggered. WE must be 1 to write ifp data to op.  |
| <input checked="" type="radio"/> TRUE<br>TRUE or FALSE  | To implement a finite state machine with 37 states, I only need 6 bits of memory. Why or why not?<br><br>$2^6 = 64$ possible outcomes. 37 is less than 64, hence, 6 bit memory is enough to store 37 states.  |
| <input checked="" type="radio"/> FALSE<br>TRUE or FALSE | The output of sequential logic only depends on past inputs. Why or why not?<br><br>Although dependent on past ip, we can alter sequential logic w/ current ip input.<br>Hence, it depends on past & current input.  |
| <input checked="" type="radio"/> FALSE<br>TRUE or FALSE | A Gated D Latch has 2 inputs: S and R. Why or why not?<br><br>Gated D latch has 2 inputs: D $\rightarrow$ data we want to be written to latch $\not\equiv$ WE (write-enabled).<br>SR are ip for RS-latch.   |

2. [25 pts] Answer the following questions about sequential logic. Show your work.

- (a) Complete the truth table for the following state machine diagram (note that output in the diagram refers to the current output for that state):



| S1 | S0 | Input | N1 | N0 | Output |
|----|----|-------|----|----|--------|
| 0  | 0  | 0     | 0  | 1  | 1      |
| 0  | 0  | 1     | 0  | 0  | 1      |
| 0  | 1  | 0     | 1  | 0  | 0      |
| 0  | 1  | 1     | 0  | 1  | 0      |
| 1  | 0  | 0     | 1  | 1  | 1      |
| 1  | 0  | 1     | 1  | 0  | 1      |
| 1  | 1  | 0     | 0  | 1  | 0      |
| 1  | 1  | 1     | 1  | 0  | 0      |

- (b) Convert the following truth table to a K-map. You do not need to find K-map groupings! The top-left cell of the K-maps below corresponds to the truth table column for that output.

| S1 | S0 | I | N1 | N0 | Output |
|----|----|---|----|----|--------|
| 0  | 0  | 0 | 1  | 0  | 1      |
| 0  | 0  | 1 | 0  | 1  | 1      |
| 0  | 1  | 0 | 0  | 1  | 1      |
| 0  | 1  | 1 | 0  | 0  | 1      |
| 1  | 0  | 0 | 1  | 1  | 0      |
| 1  | 0  | 1 | 1  | 0  | 0      |
| 1  | 1  | 0 | 0  | 0  | 1      |
| 1  | 1  | 1 | 1  | 0  | 1      |

| N1 | S1'S0' | S1'S0 | S1S0 | S1S0' |
|----|--------|-------|------|-------|
| I  | 0      | 0     | 1    | 1     |
| I' | 1      | 0     | 0    | 1     |

| N0 | S1'S0' | S1'S0 | S1S0 | S1S0' |
|----|--------|-------|------|-------|
| I  | 1      | 0     | 0    | 0     |
| I' | 0      | 1     | 0    | 1     |

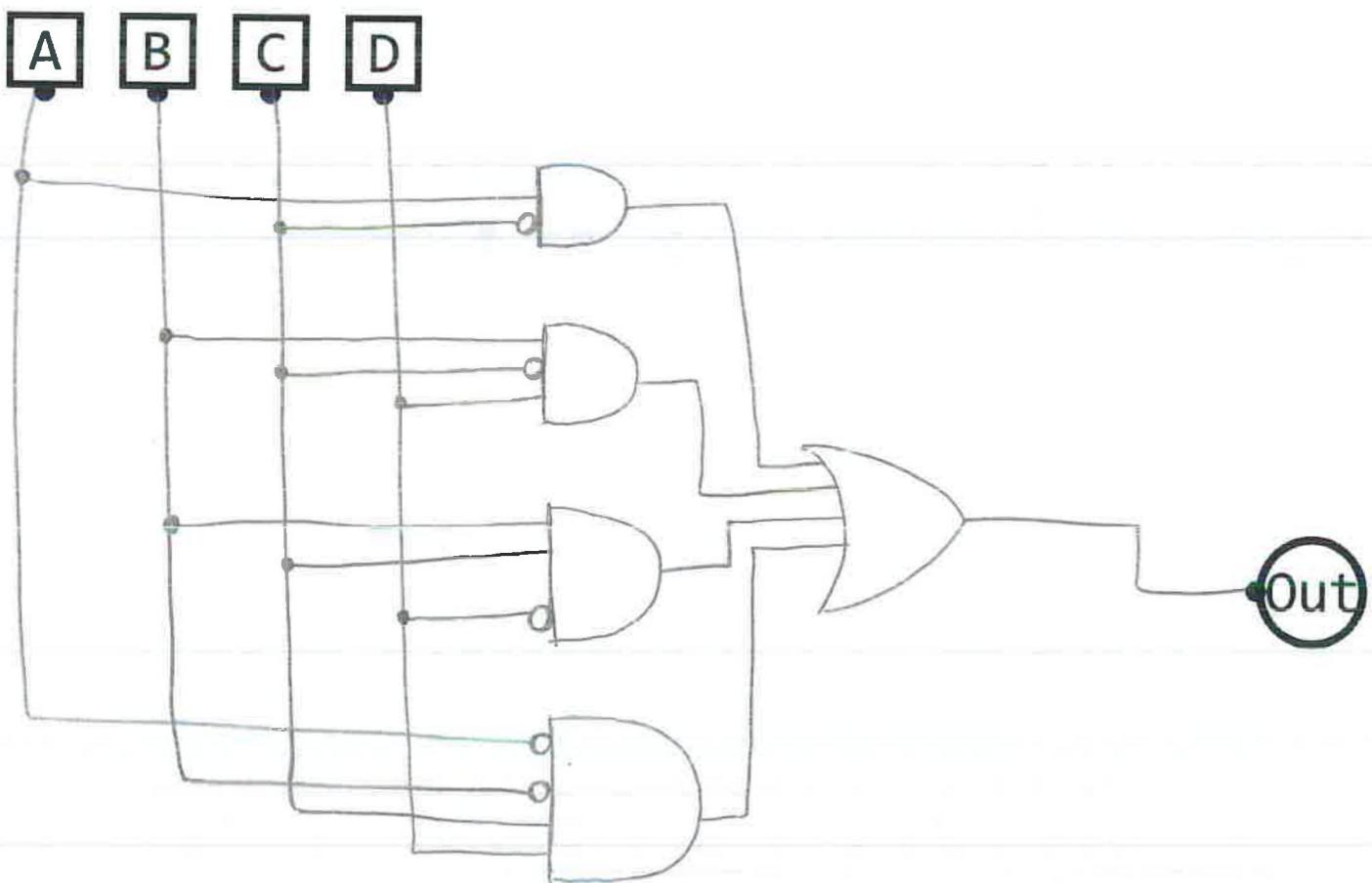
| Output | S1'S0' | S1'S0 | S1S0 | S1S0' |
|--------|--------|-------|------|-------|
| I      | 1      | 1     | 1    | 0     |
| I'     | 1      | 1     | 1    | 0     |

- (c) Convert the following K-map groupings to a Sum-of-Products (SOP) equation. Then draw a circuit using only AND and OR gates (possibly with bubbled inputs) that performs your equation:

|        | $C'D'$ | $C'D$ | $CD$ | $CD'$ |
|--------|--------|-------|------|-------|
| $A'B'$ | 0      | 0     | 1    | 0     |
| $A'B$  | 0      | 1     | 0    | 1     |
| $AB$   | 1      | 1     | 0    | X     |
| $AB'$  | 1      | 1     | 0    | 0     |

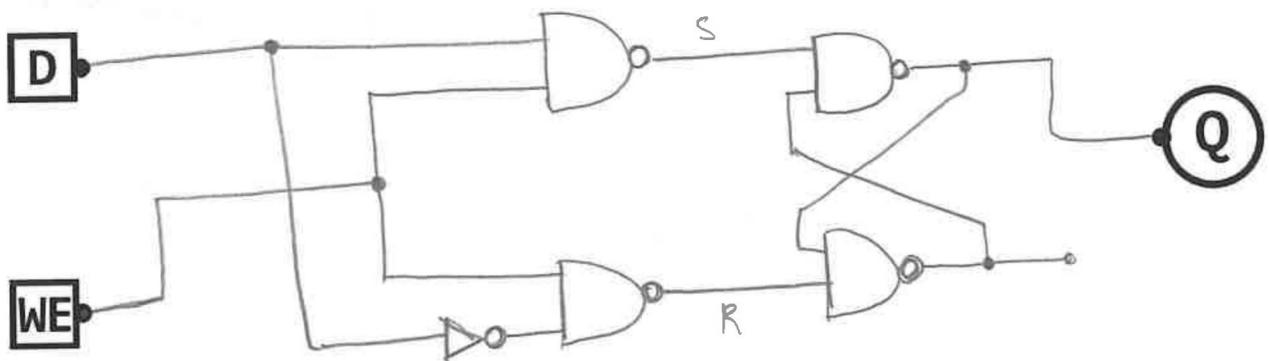
SOP Expression:  $Ac' + Bc'D + BCD' + A'B'CD$

Circuit:



3. [25 pts] Answer the following questions about sequential logic. **Show your work.**

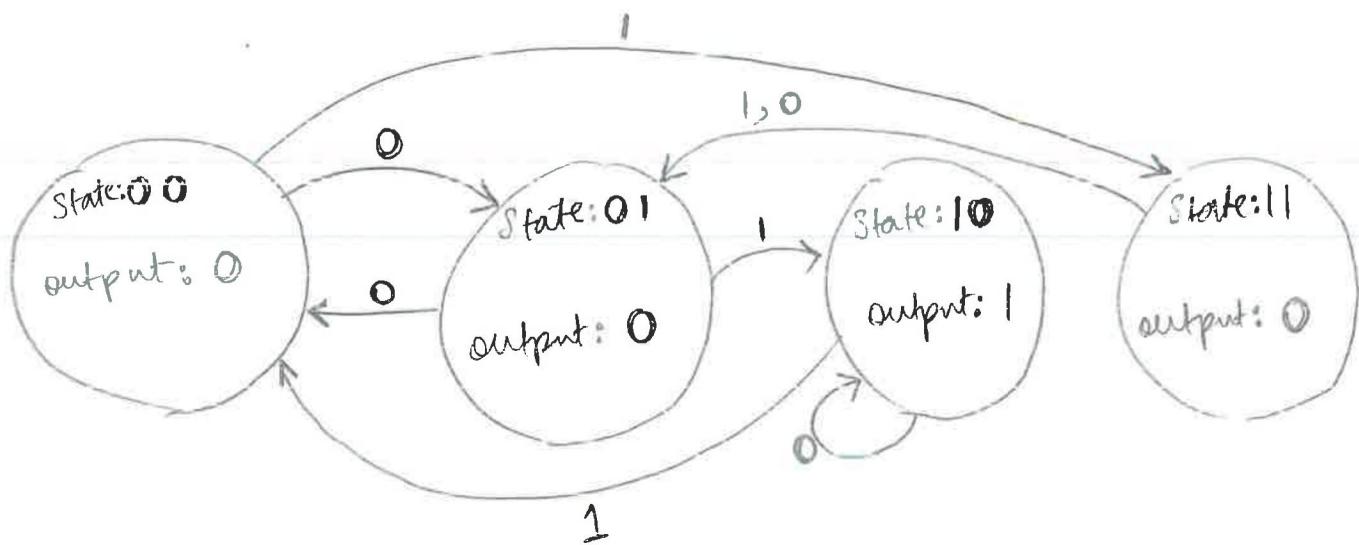
- (a) Draw a Gated D-Latch using only NAND2 gates and NOT gates. Do **not** use bubbles on the inputs of gates.



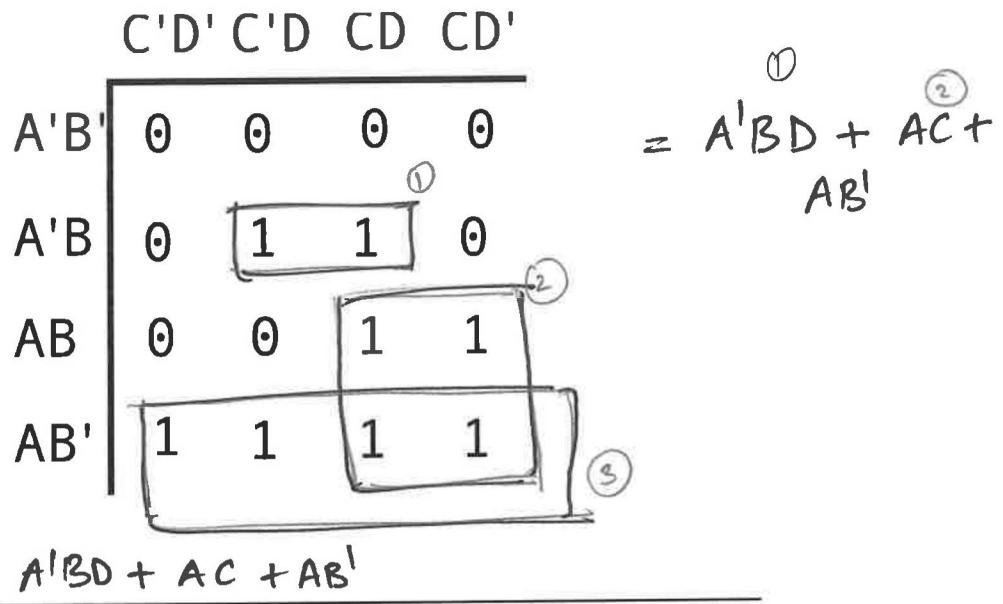
- (b) Based on the following truth table, re-draw the finite state machine diagram. Follow a format similar to the state transition diagram in Q2(a): Represent each state with a circle containing the state number. Draw state transitions as arrows, clearly labeling them with the respective inputs. Write the output as "Output=0" or "Output=1" inside the circle for the corresponding state.

| S1 | S0 | I | N1 | N0 | Output |
|----|----|---|----|----|--------|
| 0  | 0  | 0 | 0  | 1  | 0      |
| 0  | 0  | 1 | 1  | 1  | 0      |
| 0  | 1  | 0 | 0  | 0  | 0      |
| 0  | 1  | 1 | 1  | 0  | 0      |
| 1  | 0  | 0 | 1  | 0  | 1      |
| 1  | 0  | 1 | 0  | 0  | 1      |
| 1  | 1  | 0 | 0  | 1  | 0      |
| 1  | 1  | 1 | 0  | 1  | 0      |

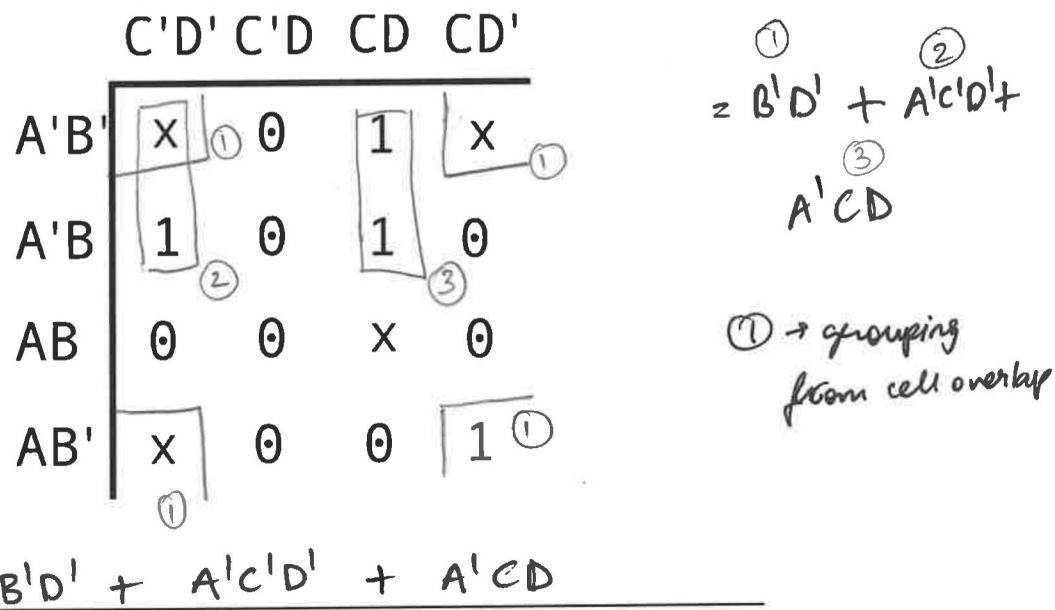
→ based on  
Q.2(a), the  
o/p refers to  
current state o/p



- (c) Find and draw the ideal groupings for the following K-map and write a Sum-of-Products (SOP) formula:



- (d) Find and draw the ideal groupings for the following K-map and write a Sum-of-Products (SOP) formula:



$\text{d}m = \text{d}A$

$\text{d}A$



$$\text{d}m = \text{d}A = \rho \cdot \Delta A$$

$$dm_A = dm_B$$

$\text{d}A$

$\text{d}m = \text{d}A$