DOOR SECURITY CONTROL

Group 14

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ACKNOWLEDGEMENTS

We would like to thank Professor K.R. Anupama for providing us with the opportunity to broaden our knowledge through the course Microprocessors and Interfacing(CS F241) and for her continued guidance throughout the design of the assignment. We would also like to thank the Teaching Assistants for their continuous support.

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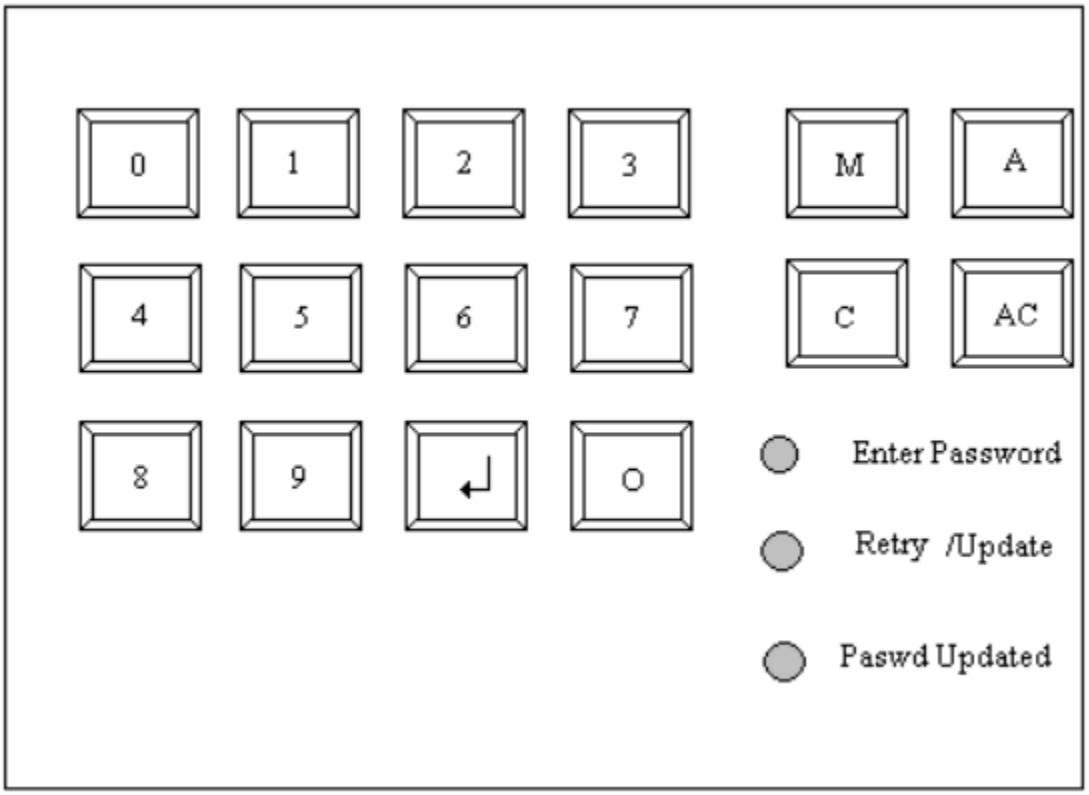
PROBLEM STATEMENT

Description: This system controls the opening and closing of a door based on password entry. If the password is correct the person can enter. Each person is given two chances to enter the correct password. On failure an alarm is sounded. Inside the room a button is available when the button is pressed the door opens for I Min, so that the person can leave the room.

User Interface: There are three set of passwords: (1) User (2) Master (3) Alarm off



- The Master password is used by the security Personnel for updating Password of the day. Pressing the M button activates this mode. The system glows Enter Password LED asking the personnel to enter the password. The master password is a 16-digit value. The master is given only a single chance to enter the password. If authenticated, the retry/Update LED glows. If there is a failure in authentication

the alarm is sounded. When the retry/ Update LED glows the user has to enter password of the day. This is 12-digit value. Once this value has been accepted by the system the Passwd Updated LED glows.

- User has to press the O key when he wants to enter the room. The Enter Password LED prompts the user to enter the password. The user is given C/AC option as well. If the first attempt fails, the RETRY LED glows. The user is allowed to re-enter password, on authentication door opens for a period of 1 Min. On Failure an ALARM is sounded.
- To Turn-off the Alarm the A button has to be pressed. Enter Password LED glows prompting user to enter the 14-digit password for turning of alarm, no retries are allowed. If authentication is successful then the alarm is turned off.
- To leave the room a button is available inside the room, when the button is pressed the door opens for 1 Minute so that the person can leave the room.

ASSUMPTIONS

1) Once the user has entered a mode, it is necessary to complete the entire procedure. Pressing any other mode buttons like M, O or A while another mode is being executed will not change the mode.
2) No two operations can be carried out together. (For example, the user can't be accessing the lock from outside and simultaneously someone else can't be pressing the button on the other side of the door).
3) The original Master Password, Alarm Password and Locking Password are pre-stored in the system.
4) If the user enters the wrong Alarm password, the system gets stuck in that state with the alarm permanently turned on until the system is restarted physically.
5) The time taken during opening and closing of the door is negligible. So we can close the door and lock it approximately at the same time.

COMPONENTS USED

1) **8086** – 16-bit microcontroller	*Quantity - 1*
2) **8284** – Clock generator	*Quantity - 1*
3) **74LS245** – Transceiver: For Demultiplexing Data bus	*Quantity - 2*
4) **74LS373** – Octal Latch: For Demultiplexing Address bus	*Quantity - 3*
5) **74LS138** – 3-to-8 decoder.	*Quantity - 3*
6) **2716** – 2k ROM chips.	*Quantity - 4*
7) **6116** – 2k RAM Chips.	*Quantity - 4*
8) **8255** – Programmable Peripheral Interface: It is used to interface I/O devices and external components with the microprocessor.	*Quantity - 1*
9) **8254** – Programmable Interval Timer. It is used to track time for interrupts.	*Quantity - 1*
10) **ULN2003A** – Darlington 7 transistor array is used as it provides high current gain needed to drive the stepper motor and alarm.	*Quantity - 1*
11) **Optical Relay**	*Quantity - 1*
12) **Button** – It is used to open the door from inside the room	*Quantity - 1*
13) **Buzzer (ABI-009-RC)**– It is used to raise an alarm when wrong password is entered.	*Quantity - 1*
14) **LEDs** – Indicates status	*Quantity - 3*
15) **Hex-keypad** - 4x4 keypad array to take input from the User.	*Quantity - 1*
16) **8259** - Priority Interrupt Controller	*Quantity - 1*
17) **TIDA-0447** - Texas Instruments Brushless DC Motor	*Quantity - 1*
18) **FEM3500 -** Electromagnetic Lock	*Quantity - 1*
19) **TB67H450FNG -** H Bridge	*Quantity - 1*

ADDRESS MAP

Memory Interfacing:

Size of ROM chip 2716 - 2K
Size of RAM chip 6116 - 2K

Total amount of ROM used = 4K
Total amount of RAM used = 4K

ADDRESSES:

ROM1(odd & even)- 00000 - 00FFF
RAM1(odd & even)- 01000 - 01FFF
RAM2(odd & even)- 02000 - 02FFF
ROM2(odd & even)- FF000 - FFFFF

I/O MAPPING:

8255(1) Port A:- 60h
8255(1) Port B:- 62h
8255(1) Port C:- 64h
8255(1) Control Register:- 66h

8255(2) Port A:- 68h
8255(2) Port B:- 6Ah
8255(2) Port C:- 6Ch
8255(2) Control Register:- 6Eh

8254 Counter 0:-74h
8254 Counter 1:- 76h
8254 Counter 2:- 78h
8254 Control Register:- 7Ah

INTERRUPT VECTOR TABLE

ISR name	Vector No.	Starting address in IVT	Address of CS & IP	Value stored
ISR0	40h	100h	IP: 00100h 00101h CS: 00102h 00103h	00h 04h 00h 00h
ISR1	41h	104h	IP: 00104h 00105h CS: 00106h 00107h	00h 08h 00h 00h

DATASHEETS

1.) 2716- 2K ROM Chip

MM2716E

National Semiconductor

MOS EPROMs
PRELIMINARY

MM2716E 16,384-Bit (2048 × 8) UV Erasable PROM Extended Temperature Range

General Description

The MM2716E is a high speed 16k UV erasable and electrically reprogrammable EPROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements.

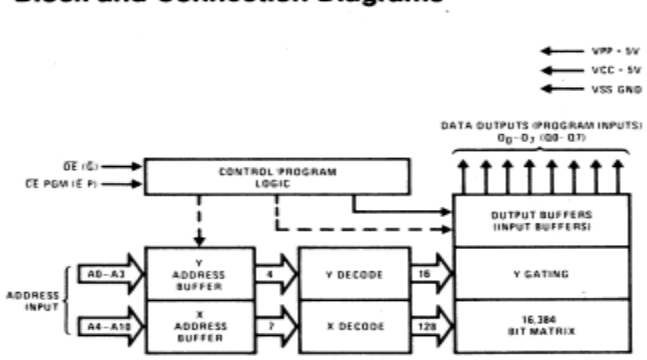
The MM2716E is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

This EPROM is fabricated with the reliable, high volume, time proven, N-channel silicon gate technology.

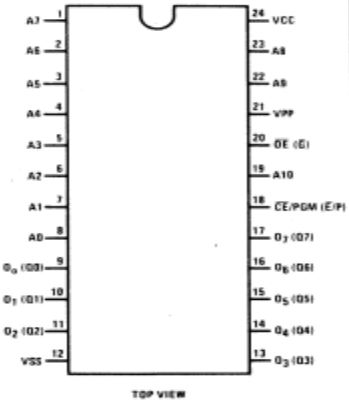
Features

- −40°C to +85°C
- 2048 x 8 organization
- 550 mW max active power, 137.5 mW max standby power
- Low power during programming
- Access time — 450 ns
- Single 5V ±10% power supply
- Static—no clocks required
- Inputs and outputs TTL compatible during both read and program modes
- TRI-STATE® output

Block and Connection Diagrams*



Dual-In-Line Package



TOP VIEW

Order Number MM2716QE
See NS Package J24CQ

Pin Connection During Read or Program

MODE	PIN NAME/NUMBER				
	$\overline{CE}$/PGM ($\overline{E}$/P) 18	$\overline{OE}$ ($\overline{G}$) 20	VPP 21	VCC 24	OUTPUTS 9–11, 13–17
Read	VIL	VIL	5	5	DOUT
Program	Pulsed VIL to VIH	VIH	25	5	DIN

*Symbols in parentheses are proposed industry standard

Pin Names

A0–A10	Address Inputs
O_0–O_7 (Q0–Q7)	Data Outputs
$\overline{CE}$/PGM ($\overline{E}$/P)	Chip Enable/Program
$\overline{OE}$ ($\overline{G}$)	Output Enable
VPP	Read 5V, Program 25V
VCC	Power (5V)
VSS	Ground

5-18

2.) 6116- 2K RAM Chip

CMOS Static RAM
16K (2K x 8-Bit)

IDT6116SA
IDT6116LA

Features

- High-speed access and chip select times
  - *Military: 20/25/35/45/55/70/90/120/150ns (max.)*
  - *Industrial: 20/25/35/45ns (max.)*
  - *Commercial: 15/20/25/35/45ns (max.)*
- Low-power consumption
- Battery backup operation
  - *2V data retention voltage (LA version only)*
- Produced with advanced CMOS high-performance technology
- CMOS process virtually eliminates alpha particle soft-error rates
- Input and output directly TTL-compatible
- Static operation: no clocks or refresh required
- Available in ceramic and plastic 24-pin DIP, 24-pin Thin Dip, 24-pin SOIC and 24-pin SOJ
- Military product compliant to MIL-STD-833, Class B

Description

The IDT6116SA/LA is a 16,384-bit high-speed static RAM organized as 2K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology.

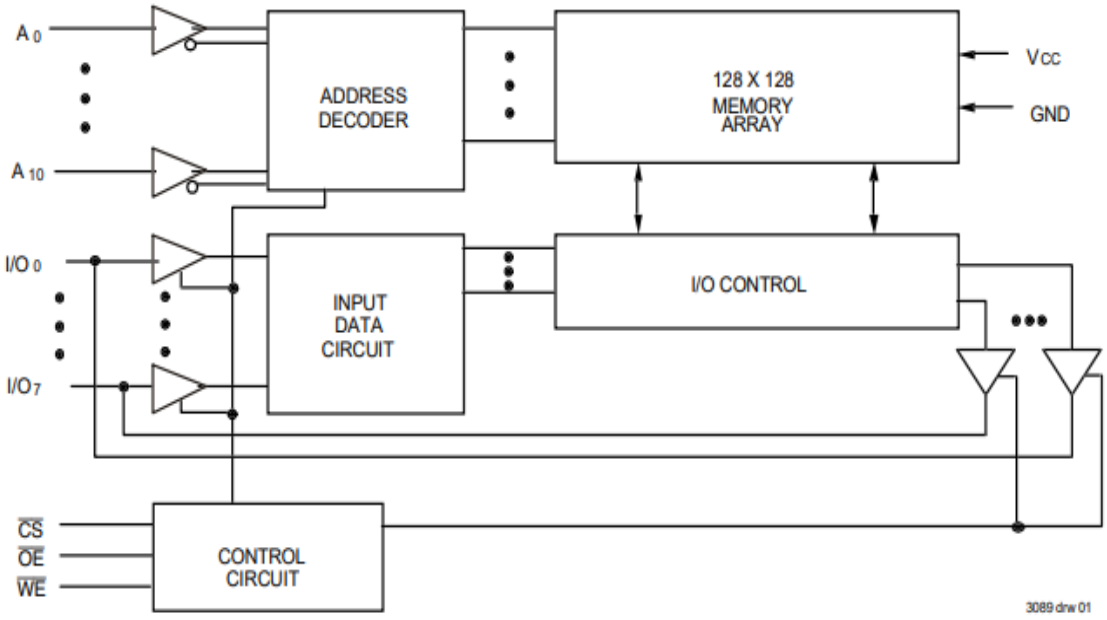
Access times as fast as 15ns are available. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes HIGH, the circuit will automatically go to, and remain in, a standby power mode, as long as $\overline{CS}$ remains HIGH. This capability provides significant system level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1µW to 4µW operating off a 2V battery.

All inputs and outputs of the IDT6116SA/LA are TTL-compatible. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

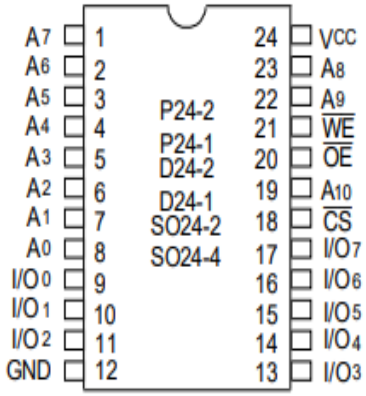
The IDT6116SA/LA is packaged in 24-pin 600 and 300 mil plastic or ceramic DIP, 24-lead gull-wing SOIC, and 24-lead J-bend SOJ providing high board-level packing densities.

Military grade product is manufactured in compliance to the latest version of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

Functional Block Diagram



Pin Configurations



3089 drw 02

DIP/SOIC/SOJ

Top View

Pin Description

Name	Description
A_0 - A_{10}	Address Inputs
I/O_0 - I/O_7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power
GND	Ground

3089 tbl 01

Truth Table(1)

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O
Standby	H	X	X	High-Z
Read	L	L	H	$DATA_{OUT}$
Read	L	H	H	High-Z
Write	L	X	L	$DATA_{IN}$

3089 tbl 02

NOTE:
1. H = V_{IH}, L = V_{IL}, X = Don't Care.

Capacitance (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	pF

3089 tbl 03

NOTE:
1. This parameter is determined by device characterization, but is not production tested.

Absolute Maximum Ratings(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

3089 tbl 04

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} +0.5V.

3.) 8255 Chip

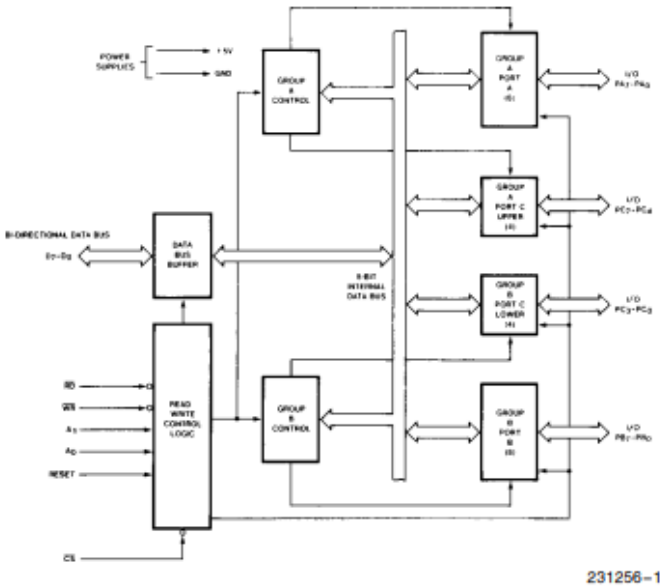
82C55A
CHMOS PROGRAMMABLE PERIPHERAL INTERFACE

- **Compatible with all Intel and Most Other Microprocessors**
- **High Speed, "Zero Wait State" Operation with 8 MHz 8086/88 and 80186/188**
- **24 Programmable I/O Pins**
- **Low Power CHMOS**
- **Completely TTL Compatible**
- **Control Word Read-Back Capability**
- **Direct Bit Set/Reset Capability**
- **2.5 mA DC Drive Capability on all I/O Port Outputs**
- **Available in 40-Pin DIP and 44-Pin PLCC**
- **Available in EXPRESS**
  — Standard Temperature Range
  — Extended Temperature Range

The Intel 82C55A is a high-performance, CHMOS version of the industry standard 8255A general purpose programmable I/O device which is designed for use with all Intel and most other microprocessors. It provides 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. The 82C55A is pin compatible with the NMOS 8255A and 8255A-5.

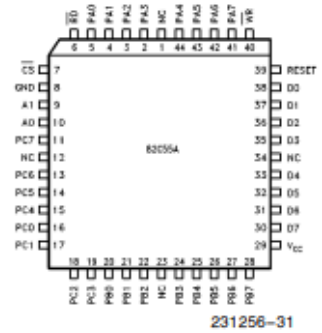
In MODE 0, each group of 12 I/O pins may be programmed in sets of 4 and 8 to be inputs or outputs. In MODE 1, each group may be programmed to have 8 lines of input or output. 3 of the remaining 4 pins are used for handshaking and interrupt control signals. MODE 2 is a strobed bi-directional bus configuration.

The 82C55A is fabricated on Intel's advanced CHMOS III technology which provides low power consumption with performance equal to or greater than the equivalent NMOS product. The 82C55A is available in 40-pin DIP and 44-pin plastic leaded chip carrier (PLCC) packages.

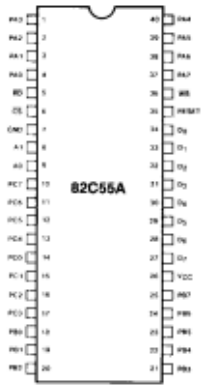


231256-1

Figure 1. 82C55A Block Diagram



231256-31



231256-2

Figure 2. 82C55A Pinout
Diagrams are for pin reference only. Package sizes are not to scale.

Table 1. Pin Description

Symbol	Pin Number Dip	Pin Number PLCC	Type	Name and Function
PA_{3-0}	1–4	2–5	I/O	**PORT A, PINS 0–3:** Lower nibble of an 8-bit data output latch/ buffer and an 8-bit data input latch.
$\overline{RD}$	5	6	I	**READ CONTROL:** This input is low during CPU read operations.
$\overline{CS}$	6	7	I	**CHIP SELECT:** A low on this input enables the 82C55A to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and WR are ignored otherwise.
GND	7	8		**System Ground**
A_{1-0}	8–9	9–10	I	**ADDRESS:** These input signals, in conjunction $\overline{RD}$ and $\overline{WR}$, control the selection of one of the three ports or the control word registers.

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Input Operation (Read)
0	0	0	1	0	Port A - Data Bus
0	1	0	1	0	Port B - Data Bus
1	0	0	1	0	Port C - Data Bus
1	1	0	1	0	Control Word - Data Bus
					Output Operation (Write)
0	0	1	0	0	Data Bus - Port A
0	1	1	0	0	Data Bus - Port B
1	0	1	0	0	Data Bus - Port C
1	1	1	0	0	Data Bus - Control
					Disable Function
X	X	X	X	1	Data Bus - 3 - State
X	X	1	1	0	Data Bus - 3 - State

PC_{7-4}	10–13	11,13–15	I/O	**PORT C, PINS 4–7:** Upper nibble of an 8-bit data output latch/ buffer and an 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.
PC_{0-3}	14–17	16–19	I/O	**PORT C, PINS 0–3:** Lower nibble of Port C.
PB_{0-7}	18–25	20–22, 24–28	I/O	**PORT B, PINS 0–7:** An 8-bit data output latch/buffer and an 8-bit data input buffer.
V_{CC}	26	29		**SYSTEM POWER:** + 5V Power Supply.
D_{7-0}	27–34	30–33, 35–38	I/O	**DATA BUS:** Bi-directional, tri-state data bus lines, connected to system data bus.
RESET	35	39	I	**RESET:** A high on this input clears the control register and all ports are set to the input mode.
$\overline{WR}$	36	40	I	**WRITE CONTROL:** This input is low during CPU write operations.
PA_{7-4}	37–40	41–44	I/O	**PORT A, PINS 4–7:** Upper nibble of an 8-bit data output latch/ buffer and an 8-bit data input latch.
NC		1, 12, 23, 34		No Connect

4.) 8254 Chip

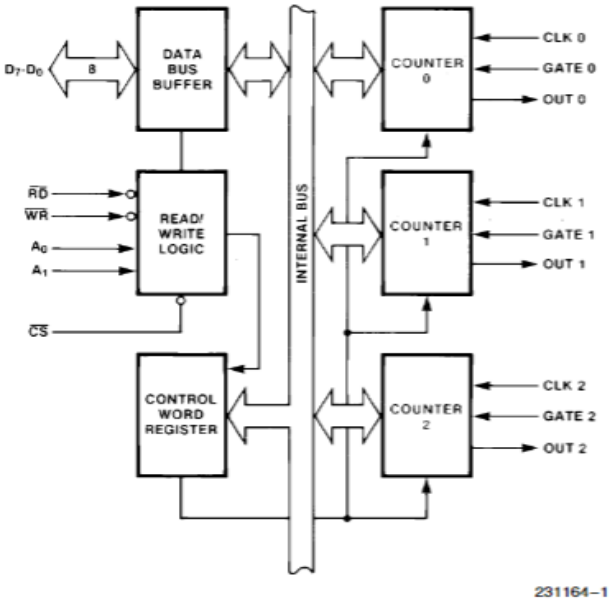
intel

8254
PROGRAMMABLE INTERVAL TIMER

- **Compatible with All Intel and Most Other Microprocessors**
- **Handles Inputs from DC to 10 MHz**
  - **— 8 MHz 8254**
  - **— 10 MHz 8254-2**
- **Status Read-Back Command**
- **Six Programmable Counter Modes**
- **Three Independent 16-Bit Counters**
- **Binary or BCD Counting**
- **Single + 5V Supply**
- **Available in EXPRESS**
  - **— Standard Temperature Range**

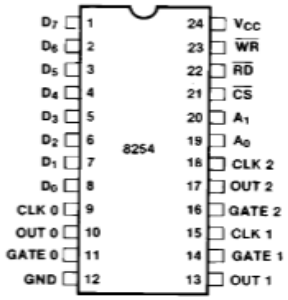
The Intel 8254 is a counter/timer device designed to solve the common timing control problems in microcomputer system design. It provides three independent 16-bit counters, each capable of handling clock inputs up to 10 MHz. All modes are software programmable. The 8254 is a superset of the 8253.

The 8254 uses HMOS technology and comes in a 24-pin plastic or CERDIP package.



231164-1

Figure 1. 8254 Block Diagram



231164-2

Figure 2. Pin Configuration

September 1993

Order Number: 231164-005

Table 1. Pin Description

Symbol	Pin No.	Type	Name and Function
D_7–D_0	1–8	I/O	**DATA:** Bi-directional three state data bus lines, connected to system data bus.
CLK 0	9	I	**CLOCK 0:** Clock input of Counter 0.
OUT 0	10	O	**OUTPUT 0:** Output of Counter 0.
GATE 0	11	I	**GATE 0:** Gate input of Counter 0.
GND	12		**GROUND:** Power supply connection.
V_{CC}	24		**POWER:** +5V power supply connection.
$\overline{WR}$	23	I	**WRITE CONTROL:** This input is low during CPU write operations.
$\overline{RD}$	22	I	**READ CONTROL:** This input is low during CPU read operations.
$\overline{CS}$	21	I	**CHIP SELECT:** A low on this input enables the 8254 to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and $\overline{WR}$ are ignored otherwise.
A_1, A_0	20–19	I	**ADDRESS:** Used to select one of the three Counters or the Control Word Register for read or write operations. Normally connected to the system address bus.

A_1	A_0	Selects
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Word Register

CLK 2	18	I	**CLOCK 2:** Clock input of Counter 2.
OUT 2	17	O	**OUT 2:** Output of Counter 2.
GATE 2	16	I	**GATE 2:** Gate input of Counter 2.
CLK 1	15	I	**CLOCK 1:** Clock input of Counter 1.
GATE 1	14	I	**GATE 1:** Gate input of Counter 1.
OUT 1	13	O	**OUT 1:** Output of Counter 1.

FUNCTIONAL DESCRIPTION

General

The 8254 is a programmable interval timer/counter designed for use with Intel microcomputer systems. It is a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The 8254 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in software, the programmer configures the 8254 to match his requirements and programs one of the counters for the desired delay. After the desired delay, the 8254 will interrupt the CPU. Software overhead is minimal and variable length delays can easily be accommodated.

Some of the other counter/timer functions common to microcomputers which can be implemented with the 8254 are:

- Real time clock
- Event-counter
- Digital one-shot
- Programmable rate generator
- Square wave generator
- Binary rate multiplier
- Complex waveform generator
- Complex motor controller

Block Diagram

DATA BUS BUFFER

This 3-state, bi-directional, 8-bit buffer is used to interface the 8254 to the system bus (see Figure 3).

5.) Hex Keypad

PARALLAX

Web Site: www.parallax.com
Forums: forums.parallax.com
Sales: sales@parallax.com
Technical: support@parallax.com

Office: (916) 624-8333
Fax: (916) 624-8003
Sales: (888) 512-1024
Tech Support: (888) 997-8267

4x4 Matrix Membrane Keypad (#27899)

This 16-button keypad provides a useful human interface component for microcontroller projects. Convenient adhesive backing provides a simple way to mount the keypad in a variety of applications.

Features

- **Ultra-thin design**
- **Adhesive backing**
- **Excellent price/performance ratio**
- **Easy interface to any microcontroller**
- **Example programs provided for the BASIC Stamp 2 and Propeller P8X32A microcontrollers**

Key Specifications

- **Maximum Rating: 24 VDC, 30 mA**
- **Interface: 8-pin access to 4x4 matrix**
- **Operating temperature: 32 to 122 °F (0 to 50°C)**
- **Dimensions:**
  Keypad, 2.7 x 3.0 in (6.9 x 7.6 cm)
  Cable: 0.78 x 3.5 in (2.0 x 8.8 cm)

Application Ideas

- **Security systems**
- **Menu selection**
- **Data entry for embedded systems**

https://www.parallax.com/product/4x4-matrix-membrane-keypad/

How it Works

Matrix keypads use a combination of four rows and four columns to provide button states to the host device, typically a microcontroller. Underneath each key is a pushbutton, with one end connected to one row, and the other end connected to one column. These connections are shown in Figure 1.

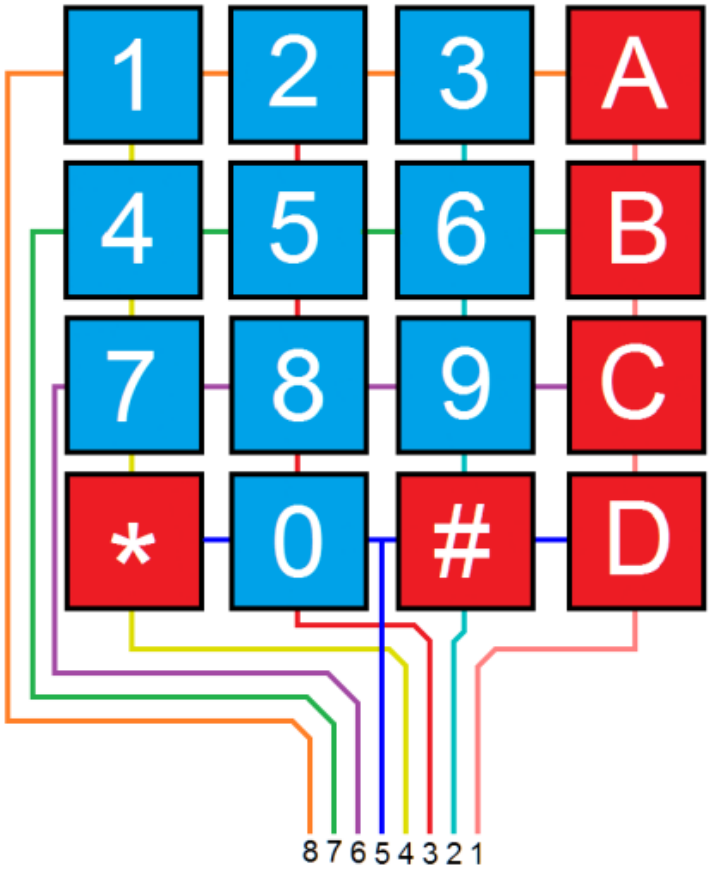


Figure 1: Matrix Keypad Connections

In order for the microcontroller to determine which button is pressed, it first needs to pull each of the four columns (pins 1-4) either low or high one at a time, and then poll the states of the four rows (pins 5-8). Depending on the states of the columns, the microcontroller can tell which button is pressed.

For example, say your program pulls all four columns low and then pulls the first row high. It then reads the input states of each column, and reads pin 1 high. This means that a contact has been made between column 4 and row 1, so button 'A' has been pressed.

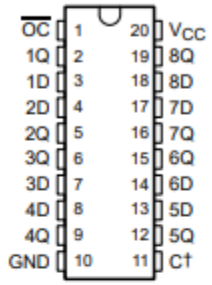
6.)SN74LS373

SN54LS373, SN54LS374, SN54S373, SN54S374, SN74LS373, SN74LS374, SN74S373, SN74S374
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

SDLS165B – OCTOBER 1975 – REVISED AUGUST 2002

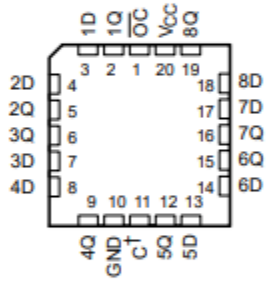
- **Choice of Eight Latches or Eight D-Type Flip-Flops in a Single Package**
- **3-State Bus-Driving Outputs**
- **Full Parallel Access for Loading**
- **Buffered Control Inputs**
- **Clock-Enable Input Has Hysteresis to Improve Noise Rejection ('S373 and 'S374)**
- **P-N-P Inputs Reduce DC Loading on Data Lines ('S373 and 'S374)**

SN54LS373, SN54LS374, SN54S373, SN54S374 . . . J OR W PACKAGE
SN74LS373, SN74S374 . . . DW, N, OR NS PACKAGE
SN74LS374 . . . DB, DW, N, OR NS PACKAGE
SN74S373 . . . DW OR N PACKAGE
(TOP VIEW)



† C for 'LS373 and 'S373; CLK for 'LS374 and 'S374.

SN54LS373, SN54LS374, SN54S373, SN54S374 . . . FK PACKAGE
(TOP VIEW)



† C for 'LS373 and 'S373; CLK for 'LS374 and 'S374.

description

These 8-bit registers feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The high-impedance 3-state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pullup components. These devices are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'LS373 and 'S373 are transparent D-type latches, meaning that while the enable (C or CLK) input is high, the Q outputs follow the data (D) inputs. When C or CLK is taken low, the output is latched at the level of the data that was set up.

The eight flip-flops of the 'LS374 and 'S374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs are set to the logic states that were set up at the D inputs.

Schmitt-trigger buffered inputs at the enable/clock lines of the 'S373 and 'S374 devices simplify system design as ac and dc noise rejection is improved by typically 400 mV due to the input hysteresis. A buffered output-control ($\overline{OC}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

$\overline{OC}$ does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered, even while the outputs are off.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

7.) SN74LS245

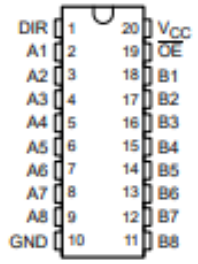
SN54LS245, SN74LS245
OCTAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SDLS146A – OCTOBER 1976 – REVISED FEBRUARY 2002

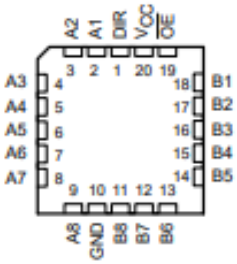
- **3-State Outputs Drive Bus Lines Directly**
- **PNP Inputs Reduce dc Loading on Bus Lines**
- **Hysteresis at Bus Inputs Improves Noise Margins**
- **Typical Propagation Delay Times Port to Port, 8 ns**

TYPE	I_{OL} (SINK CURRENT)	I_{OH} (SOURCE CURRENT)
SN54LS245	12 mA	–12 mA
SN74LS245	24 mA	–15 mA

SN54LS245 . . . J OR W PACKAGE
SN74LS245 . . . DB, DW, N, OR NS PACKAGE
(TOP VIEW)



SN54LS245 . . . FK PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can disable the device so that the buses are effectively isolated.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74LS245N	SN74LS245N
	SOIC – DW	Tube	SN74LS245DW	LS245
		Tape and reel	SN74LS245DWR	
	SOP – NS	Tape and reel	SN74LS245NSR	74LS245
	SSOP – DB	Tape and reel	SN74LS245DBR	LS245
–55°C to 125°C	CDIP – J	Tube	SN54LS245J	SN54LS245J
		Tube	SNJ54LS245J	SNJ54LS245J
	CFP – W	Tube	SNJ54LS245W	SNJ54LS245W
	LCCC – FK	Tube	SN54LS245FK	SN54LS245FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

8.) Buzzer ABI-009-RC

Buzzer

pro-SIGNAL

Features

- Black in colour
- With internal drive circuit
- Sealed structure
- Wave solderable and washable
- Housing material: Noryl

RoHS Compliant

Applications

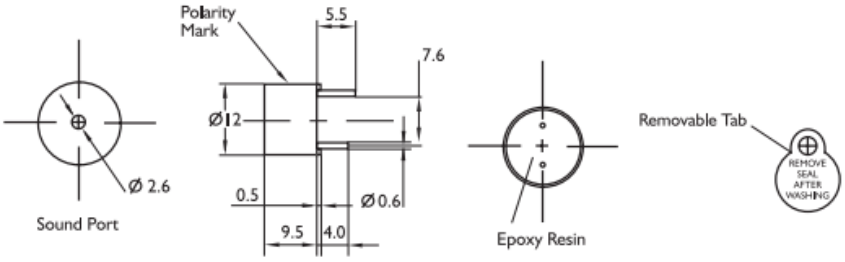
- Computer and peripherals
- Communications equipment
- Portable equipment
- Automobile electronics
- POS system
- Electronic cash register

Specifications:

Rated Voltage	: 6V DC
Operating Voltage	: 4 to 8V DC
Rated Current*	: ≤30mA
Sound Output at 10cm*	: ≥85dB
Resonant Frequency	: 2300 ±300Hz
Tone	: Continuous
Operating Temperature	: -25°C to +80°C
Storage Temperature	: -30°C to +85°C
Weight	: 2g

*Value applying at rated voltage (DC)

Diagram



Dimensions : Millimetres
Tolerance : ±0.5mm

Part Number Table

Description	Part Number
Buzzer, Electromech, 6V DC	ABI-009-RC

9.) ULN2003A Darlington Transistor

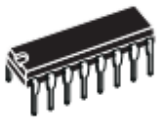
ULN2001, ULN2002
ULN2003, ULN2004

Seven Darlington array

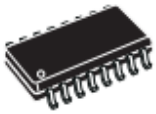
Datasheet – production data

Features

- Seven Darlingtons per package
- Output current 500 mA per driver (600 mA peak)
- Output voltage 50 V
- Integrated suppression diodes for inductive loads
- Outputs can be paralleled for higher current
- TTL/CMOS/PMOS/DTL compatible inputs
- Inputs pinned opposite outputs to simplify layout



DIP-16



SO-16 (Narrow)

These versatile devices are useful for driving a wide range of loads including solenoids, relays DC motors, LED displays filament lamps, thermal printheads and high power buffers.

The ULN2001A/2002A/2003A and 2004A are supplied in 16 pin plastic DIP packages with a copper leadframe to reduce thermal resistance. They are available also in small outline package (SO-16) as ULN2001D1/2002D1/2003D1/ 2004D1

Description

The ULN2001, ULN2002, ULN2003 and ULN 2004 are high voltage, high current Darlington arrays each containing seven open collector Darlington pairs with common emitters. Each channel rated at 500 mA and can withstand peak currents of 600 mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout.

The versions interface to all common logic families:

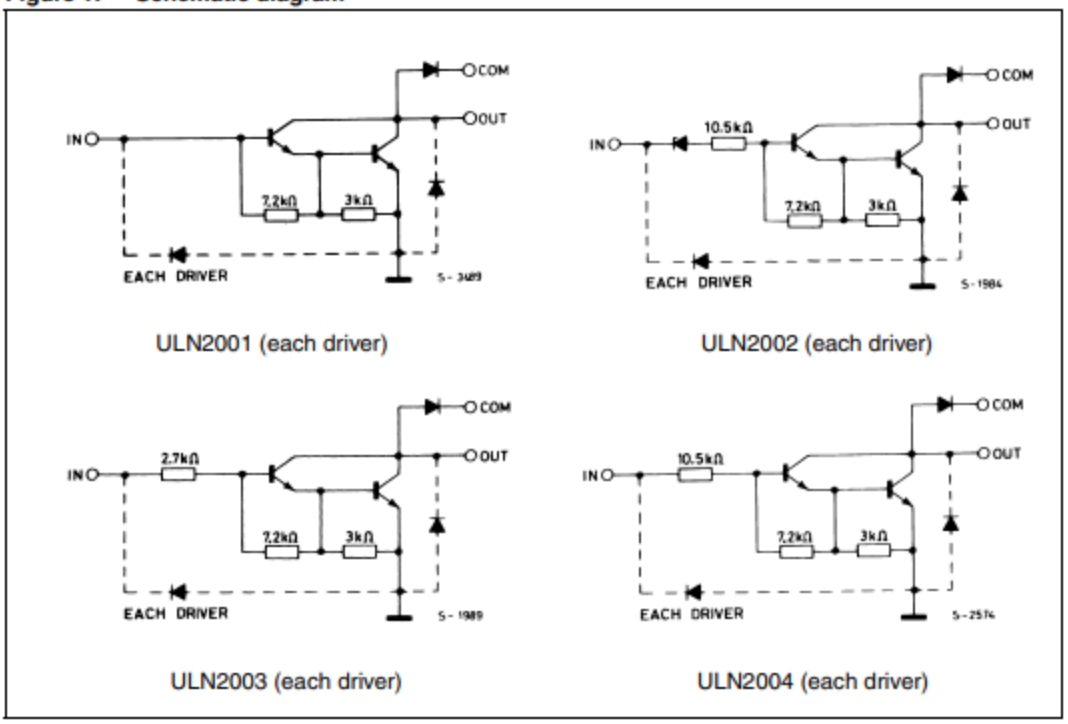
- ULN2001 (general purpose, DTL, TTL, PMOS, CMOS)
- ULN2002 (14 - 25 V PMOS)
- ULN2003 (5 V TTL, CMOS)
- ULN2004 (6 - 15 V CMOS, PMOS)

Table 1. Device summary

Order codes	
ULN2001A	ULN2001D1013TR
ULN2002A	ULN2002D1013TR
ULN2003A	ULN2003D1013TR
ULN2004A	ULN2004D1013TR

1 Diagram

Figure 1. Schematic diagram



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19.) 8259 Programmable Interrupt Controller

intel

8259A
PROGRAMMABLE INTERRUPT CONTROLLER
(8259A/8259A-2)

- 8086, 8088 Compatible
- MCS-80, MCS-85 Compatible
- Eight-Level Priority Controller
- Expandable to 64 Levels
- Programmable Interrupt Modes
- Individual Request Mask Capability
- Single +5V Supply (No Clocks)
- Available in 28-Pin DIP and 28-Lead PLCC Package
  (See Packaging Spec., Order #231369)
- Available in EXPRESS
  — Standard Temperature Range
  — Extended Temperature Range

The Intel 8259A Programmable Interrupt Controller handles up to eight vectored priority interrupts for the CPU. It is cascadable for up to 64 vectored priority interrupts without additional circuitry. It is packaged in a 28-pin DIP, uses NMOS technology and requires a single +5V supply. Circuitry is static, requiring no clock input.

The 8259A is designed to minimize the software and real time overhead in handling multi-level priority interrupts. It has several modes, permitting optimization for a variety of system requirements.

The 8259A is fully upward compatible with the Intel 8259. Software originally written for the 8259 will operate the 8259A in all 8259 equivalent modes (MCS-80/85, Non-Buffered, Edge Triggered).

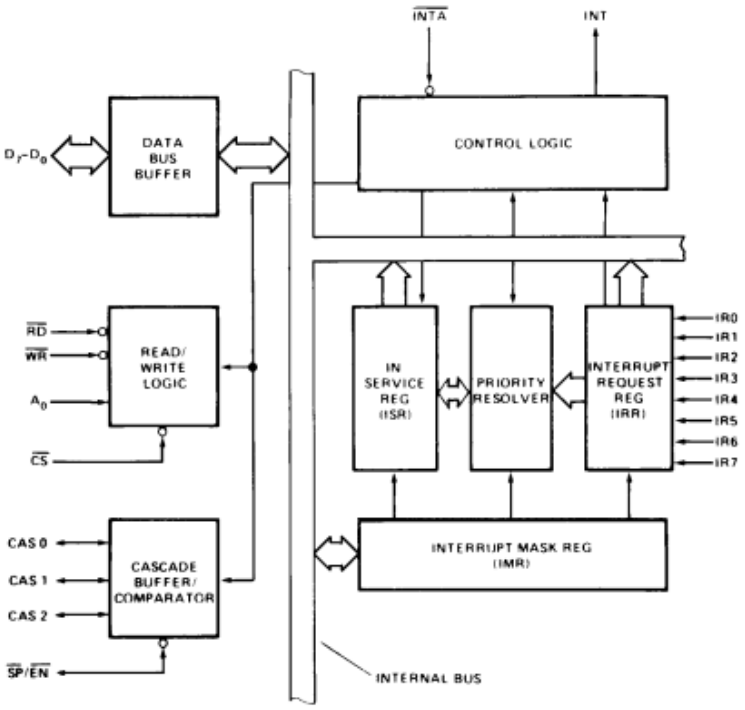


Figure 1. Block Diagram

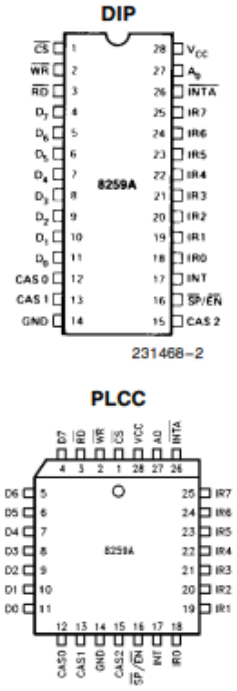


Figure 2. Pin Configurations

20.) TIDA-0447 : Texas Instruments Brushless DC Motor

TI Designs

24-V DC, 100-W/30-W Dual Sensorless Brushless DC Motor Drive Reference Design

TEXAS INSTRUMENTS

TI Designs

The TIDA-0447 is a 24-V, dual brushless motor drive platform to be used in dishwashers to drive the water circulation pump and drain pump. The drive stage for circulation pump is designed for 100-W continuous operation, and the drain pump drive stage is designed for 30-W continuous operation. The design is tested for full load operation, overcurrent, and motor stall protection.

Design Resources

TIDA-00447	Design Folder
MSP430G2744	Product Folder
CSD88539ND	Product Folder
DRV8303	Product Folder
DRV10983	Product Folder
TPD4S009	Product Folder
LMT84	Product Folder
TLV803S	Product Folder
CSD17304Q3	Product Folder
ISO7421D	Product Folder

TI E2E™ Community

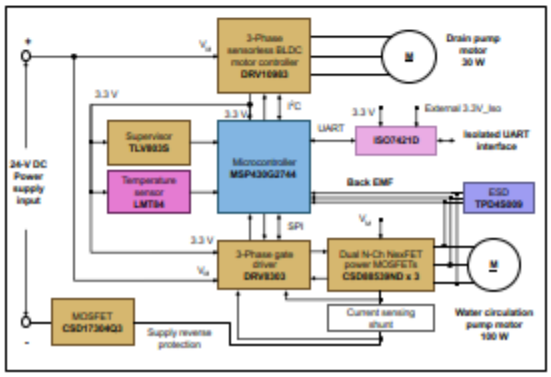
ASK Our E2E Experts
WEBENCH® Calculator Tools

Design Features

- Enables Safer, Noiseless Operation and Small Form Factor
- Circulation Pump Drive Designed for up to 100-W Continuous Operation Using Discrete Approach Having an MCU, External MOSFET Driver With Built-in Protections and Current Sensing Amplifier, and External Power MOSFETs
- MCU Software Implements InstaSPIN-BLDC, Sensorless Trapezoidal Control of BLDC Motor Using Back-EMF (BEMF) Integration Method Offering Robust Low Speed Operation, and Finer Control Over Entire Speed Range
- Drain Pump Designed for up to 30-W Continuous Operation Based on a Single-Chip, 3-Phase Motor Driver With Integrated Power MOSFETs
  - Offers Proprietary Sensorless Control Scheme to Provide Continuous Sinusoidal Drive
  - Integrates 5-V/3.3-V Buck/Linear Converter and Protection Functions Such as Overcurrent, Voltage Surge Protection, UVLO Protection, and Motor Lock Detection
- Designed to Operate at Ambient Temperatures of –20°C to 55°C

Featured Applications

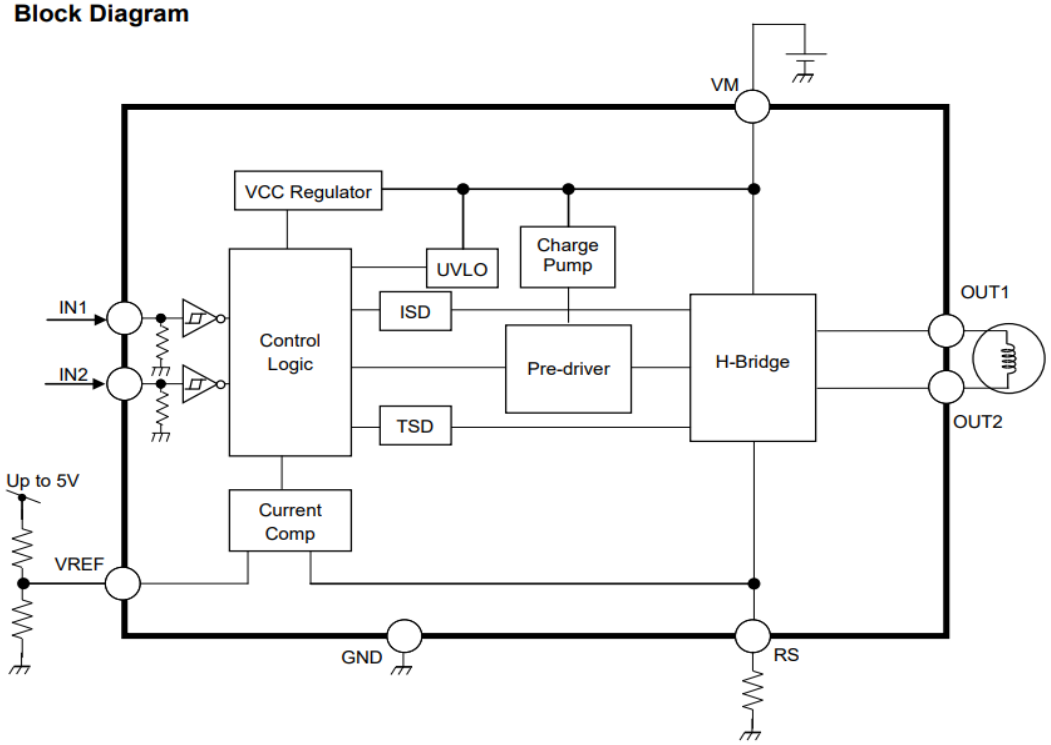
- Dishwashers
- Appliances With 24-V DC Pumps or Fans

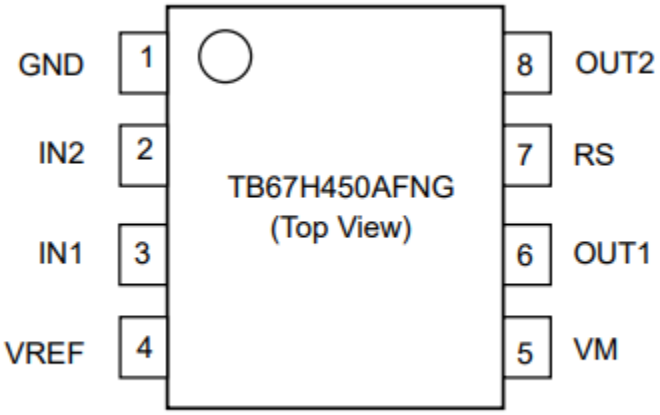


https://www.ti.com/lit/ug/tidua50b/tidua50b.pdf?ts=1681989974294&ref_url=https%253A%252F%252Fwww.google.com%252F

21.)TB67H450AFN - H bridge

Block Diagram





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23.) FEM3500 - Electromagnetic lock

FEM3500/FEM3500D/FEM3500M/FEM3500DM
Electromagnetic Lock

Electro-Magnetic Lock Description:

The FEM3500 is an unmonitored single magnetic lock and FEM3500D is an unmonitored double magnetic lock with dual 12 or 24 volt settings. There are no Lock or Door status sensors on these units. For wiring instruction refer to figure 2.

The FEM3500M is a monitored single magnetic lock and the FEM3500DM is a monitored double magnetic lock with 12 or 24 volt settings. Each magnetic lock has a built-in Hall crystal for remote monitoring of Lock status (open or closed) through relay contacts rated at 24 VDC, 1.0 A max on visible high luminosity backlight indicator position on the aluminum housing and a Door Status Sensors (DSS) for remote monitoring of Door status through reed switch contact. For wiring instruction refer to Figure 1.

Backlight Indicator OFF	Relay De-energized,	No Power on Magnetic Lock
Backlight Indicator RED	Relay De-energized,	Power on Magnetic Lock and Door is Open.
Backlight Indicator GREEN	Relay Energized,	Power on Magnetic Lock and Door Locked.

Power setting and Input

Power Input	FEM3500/ FEM3500M	FEM3500D/ FEM3500DM
12 VDC	0.50 A	2 x 0.50 A
24 VDC	0.25 A	2 × 0.25 A

The (+) lead of the power source is connected to Pins 1 (VDC +) of the terminal block and the (-) lead is connected to Pin 2 (-). The operating switch or controlling contacts must be installed between the power source and the magnetic lock to reduce operating time of the magnetic lock to a minimum. The electromagnetic lock requires a filtered and regulated DC Power Source for optimal performance.

Remove the wiring cavity cover plate and check the position of the two shunts located on the PCB. A single shunt across pins 2 and 3 will set the operating voltage to 24 volts. A shunt between pins 1 to 2 and a shunt between pins 3 to 4 sets the operating voltage to 12 volts.

These voltage shunts must be set correctly before 12 VDC or 24 VDC power is supplied to the Electromagnetic Lock to prevent damage to the unit.

Wiring connections:

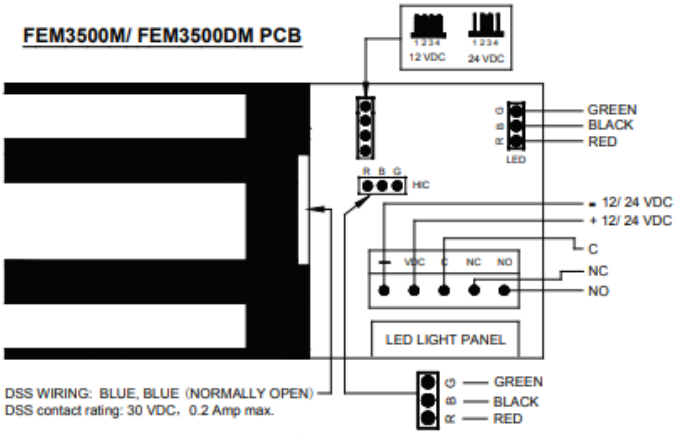


Figure 1

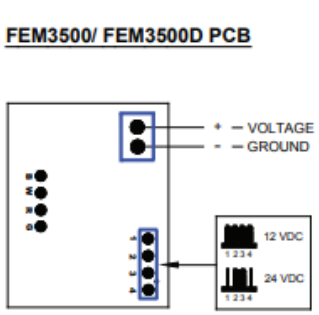


Figure 2

24.) Optical relay - TLP222G

TOSHIBA TLP222G,TLP222G-2

TOSHIBA Photocoupler Photorelay

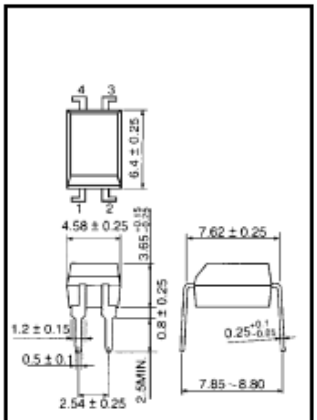
TLP222G, TLP222G-2

Cordless Telephones
PBX
Modems

The Toshiba TLP222G series consist of a gallium arsenide infrared emitting diode optically coupled to a photo-MOSFET in a DIP package.
The TLP222G series are a bi-directional switch, which can replace mechanical relays in many applications.

- TLP222G: 4-pin DIP (DIP4), 1-channel type (1-form-A)
- TLP222G-2: 8-pin DIP (DIP8), 2-channel type (2-form-A)
- Peak Off-state voltage: 350 V (min)
- Trigger LED current: 3 mA (max)
- On-state current: 120 mA (max)
- On-state resistance: 35 Ω (max, t < 1 s)
- On-state resistance: 50 Ω (max, continuous)
- Isolation voltage: 2500 Vrms (min)

Unit: mm

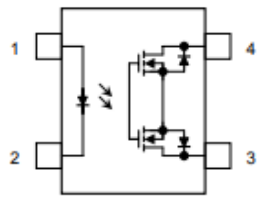


JEDEC	—
JEITA	—
TOSHIBA	11-5B2

Weight: 0.26 g (typ.)

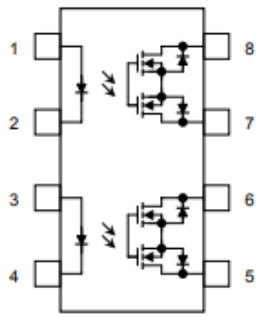
Pin Configuration (top view)

TLP222G

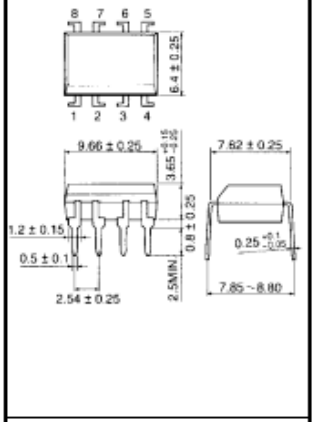


1: Anode
2: Cathode
3: Drain
4: Drain

TLP222G-2



1, 3 : Anode
2, 4 : Cathode
5 : Drain D1
6 : Drain D2
7 : Drain D3
8 : Drain D4



JEDEC	—
JEITA	—
TOSHIBA	11-10C4

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24.) Optical Relay - G3VM-21LR

G3VM-21LR

MOS FET Relays

World's Smallest* SSOP Package MOS FET Relays with Low Output Capacitance and ON Resistance (C × R = 5 pF • Ω) in a 20-V Load Voltage Model.

- **Output capacitance of 1 pF (typical) allows high-frequency applications.**

* As of March 2011 Survey by OMRON

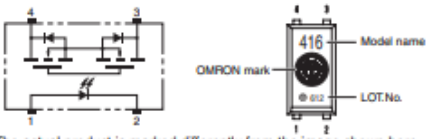
RoHS compliant

Note: The actual product is marked differently from the image shown here.

■ Application Examples

- **Semiconductor test equipment**
- **Test & Measurement equipment**
- **Communication equipment**
- **Data loggers**

■ Terminal Arrangement/Internal Connections



Note: The actual product is marked differently from the image shown here.

■ List of Models

Package type	Contact form	Terminals	Load voltage (peak value) *	Model	Minimum package quantity
					Number per tape and reel
SSOP4	1a (SPST-NO)	Surface-mounting Terminals	20 V	G3VM-21LR	-
				G3VM-21LR (TR05)	500
				G3VM-21LR (TR10)	1,000
				G3VM-21LR (TR)	1,500

Note: Ask your OMRON representative for orders under 1,500 pcs, 1,000 pcs, or 500 pcs. We can supply products with the tape already cut. Tape-cut SSOPs are packaged without humidity resistance. Use manual soldering to mount them. Refer to common precautions.

* The AC peak and DC value are given for the load voltage.

■ Absolute Maximum Ratings (Ta = 25 °C)

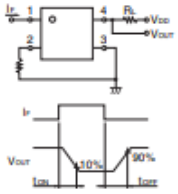
	Item	Symbol	Rating	Unit	Measurement conditions
Input	LED forward current	I_F	50	mA	
	LED forward current reduction rate	ΔI_F/°C	−0.5	mA/°C	Ta ≥ 25 °C
	LED reverse voltage	V_R	5	V	
	Connection temperature	T_J	125	°C	
Output	Load voltage (AC peak/DC)	V_{OFF}	20	V	
	Continuous load current (AC peak/DC)	I_O	160	mA	
	ON current reduction rate	ΔI_O/°C	−1.6	mA/°C	Ta ≥ 25 °C
	Connection temperature	T_J	125	°C	
Dielectric strength between I/O (See note 1.)		V_{I-O}	1500	Vrms	AC for 1 min
Ambient operating temperature		Ta	−20 to +85	°C	With no icing or condensation
Ambient storage temperature		Tstg	−40 to +125	°C	With no icing or condensation
Soldering temperature		-	260	°C	10 s

Note: 1. The dielectric strength between the input and output was checked by applying voltage between all pins as a group on the LED side and all pins as a group on the light-receiving side.

■ Electrical Characteristics (Ta = 25 °C)

	Item	Symbol	Minimum	Typical	Maximum	Unit	Measurement conditions
Input	LED forward voltage	V_F	1.0	1.15	1.3	V	I_F = 10 mA
	Reverse current	I_R	-	-	10	μA	V_R = 5 V
	Capacity between terminals	C_T	-	15	-	pF	V = 0, f = 1 MHz
	Trigger LED forward current	I_{FT}	-	-	4	mA	I_O = 100 mA
Output	Maximum resistance with output ON	R_{ON}	-	5	8	Ω	I_F = 5 mA, I_O = 160 mA, t = 10 ms
	Current leakage when the relay is open	I_{LEAK}	-	-	1.0	nA	V_{OFF} = 20 V, Ta = 50 °C
	Capacity between terminals	C_{OFF}	-	1	2.5	pF	V = 0, f = 100 MHz, t < 1 s
Capacity between I/O terminals		C_{I-O}	-	0.8	-	pF	f = 1 MHz, Vs = 0 V
Insulation resistance between I/O terminals		R_{I-O}	1000	-	-	MΩ	V_{I-O} = 500 VDC, RoH ≤ 60 %
Turn-ON time		t_{ON}	-	0.06	0.5	ms	I_F = 5 mA, R_L = 200 Ω, V_{DD} = 10 V (See note 2.)
Turn-OFF time		t_{OFF}	-	0.12	0.5	ms	

Note: 2. Turn-ON and Turn-OFF Times



https://omronfs.omron.com/en_US/ecb/products/pdf/en-g3vm_21lr.pdf