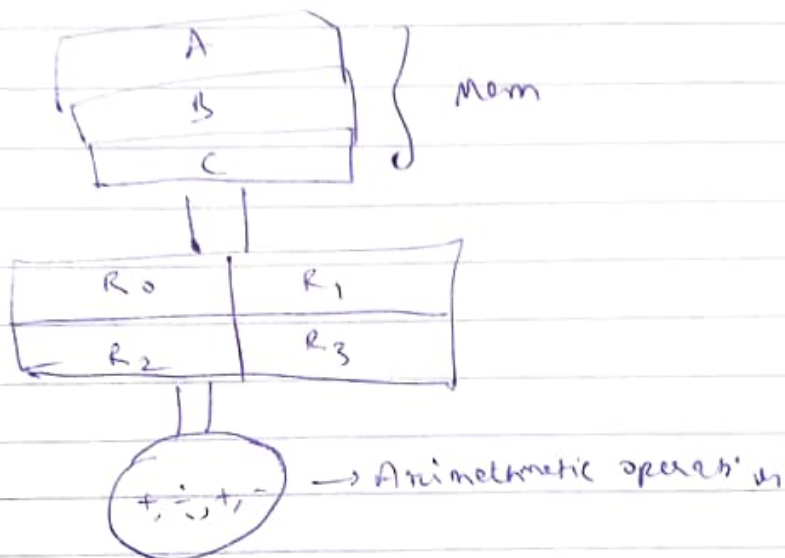


↳ Register → Register Architecture



CISC :-

MUL A, B

RISC (only register [no memory])

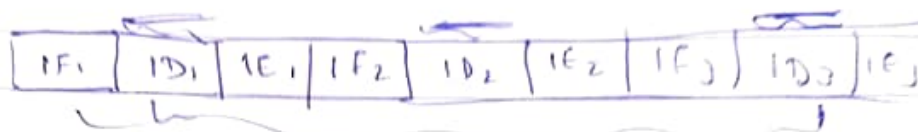
LDA R0, A

LDA R1, B

MUL R0, R1

STR A, R0

- Basic Parallel Techniques (instead of 1 using 2 components)
(to speed up the operation)
 - Pipelining
 - Replication



Instruction

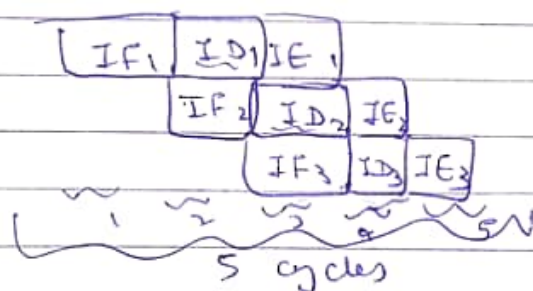
9 cycles

→ Fetch

→ Decode

→ Execute

Pipeline Hazards



ADD R2, R1, R3

SB R2, R3, R2

STR R2, b

Evolution of μp

Name	Date	Transistors	clock speed	Data width
8080	1974	6K	2MHz	8
8086	1978	29K	5MHz	16
80286	1982	134K	12	16
80386	1985	275K	10-33	32
80486	1989	1.2M	20-100	32
Pentium	1993	3.1M	60-200	32/64
Pentium II	1997	7.5M	233-450	32/64
Pentium III	1999	9.5M	450-933MHz	32/64
Pentium 4	2000	42M	1.5GHz	32/64