RISC-V Based Custom Processor with Configurable Pipeline Depth

RISC-V is an open-source and modular instruction set architecture that is widely used in processor design and academic research. Most existing RISC-V processors use a **fixed pipeline structure**, which limits flexibility in studying different pipeline configurations. This project focuses on the **design and simulation of a RISC-V based custom processor with configurable pipeline depth**.

The proposed processor supports both **3-stage and 5-stage pipeline configurations**, selectable using a configuration parameter. The processor is divided into modular pipeline stages including Instruction Fetch, Instruction Decode, Execute, Memory, and Write Back. Hazard detection and forwarding logic are implemented to ensure correct instruction execution in both pipeline modes.

Instead of using Synopsys VCS, the entire processor is **implemented and simulated using Xilinx Vivado 2018.2**. The RISC-V processor is described using **Verilog/SystemVerilog HDL**, and functional verification is performed using **Vivado's built-in simulation environment**. Instruction memory is initialized through testbench files, and pipeline behavior, hazards, and data forwarding are analyzed using waveform simulation in Vivado.

The project is **purely simulation-based** and does not involve physical hardware implementation. This approach allows students to study pipeline behavior, execution flow, and performance trade-offs using FPGA-oriented tools. The project provides practical exposure to **RISC-V architecture, pipelined processor design, and FPGA-based simulation using Xilinx Vivado.**

Workflow for Configurable RISC-V Processor Simulation

Comparison of Using **Xilinx Vivado 2018.2** vs **Synopsys VCS**