📊 RESULTS AND ANALYSIS (FINAL FORMAT)

1️⃣ Functional Simulation Results

Result:

The functional simulation of the RO-PUF design was performed using Vivado 2018.2. The simulation waveform shows proper clock operation and successful generation of PUF response bits.

Analysis:

The output puf response generates a non-zero binary value (e.g., 0010), confirming that the paired ring oscillators exhibit measurable delay differences. This validates that the design successfully exploits intrinsic process variations to generate unique PUF responses.

📌 **Key Observation:**

- Clock toggles correctly
- Reset initializes the design
- PUF output changes after enable signal

2️⃣ Resource Utilization Analysis (Area)

Result:

The FPGA resource utilization report indicates the following usage:

- Slice LUTs: **125**
- Slice Registers: **216**
- Bonded IOBs: **7**
- BUFGCTRL: **1**

Analysis:

The low utilization of LUTs and registers demonstrates that the RO-PUF design has minimal area overhead. This makes the design suitable for lightweight security applications where hardware resources are constrained.

📌 **Inference:**

- Efficient area usage
- Scalable for larger PUF instances

3️⃣ Timing Analysis (Delay)

Result:

The timing summary report shows:

- Worst Negative Slack (WNS): **∞**
- Total Negative Slack (TNS): **0.000 ns**
- Number of failing endpoints: **0**

Analysis:

The absence of setup and hold timing violations confirms that the design meets all timing requirements. Since no explicit timing constraints were applied, infinite slack values are acceptable for a simulation-only project.

📌 **Inference:**

- Design is timing-safe
- Suitable for synchronous operation

4️⃣ Power Analysis

Result:

The power analysis report indicates:

- Total On-Chip Power: **4.645 W**
- Dynamic Power: **≈ 98%**
- Static Power: **≈ 2%**

Dynamic power breakdown:

- Signals: **1.55 W**
- Logic: **1.24 W**
- I/O: **1.77 W**

Analysis:

Dynamic power dominates the overall power consumption due to continuous switching activity of the ring oscillators. Static power remains low, indicating minimal leakage. This behavior is expected in RO-based PUF architectures.

📌 **Inference:**

- Power-efficient in idle state
- Higher dynamic power during active oscillation

5️⃣ Thermal Analysis

Result:

- Junction Temperature: **≈ 48°C**
- Thermal Margin: **≈ 36°C**

Analysis:

The junction temperature remains well within safe operating limits, indicating reliable thermal performance of the design.

📌 **Inference:**

- No thermal risk
- Design is stable under estimated operating conditions

RESULTS SUMMARY

The RO-PUF design was successfully simulated and synthesized using Vivado 2018.2. Functional simulation confirmed correct PUF response generation. Resource utilization analysis showed low area overhead, timing analysis confirmed zero violations, and power analysis indicated dominant dynamic power due to oscillator activity with low static power consumption. Thermal results remained within safe limits, demonstrating the feasibility of the design for FPGA-based security applications.