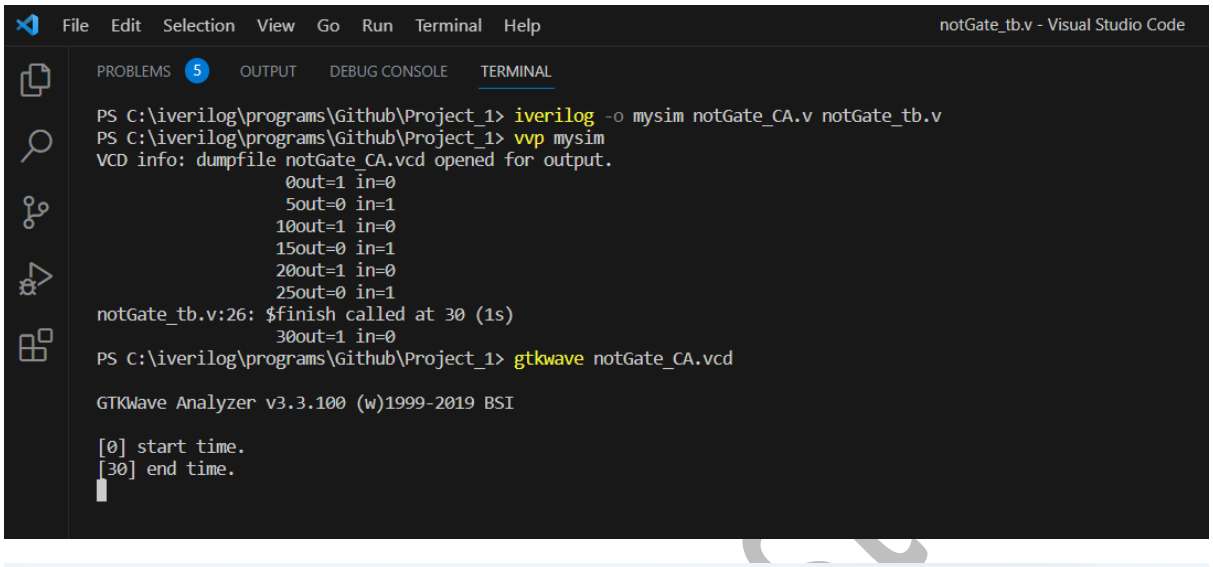
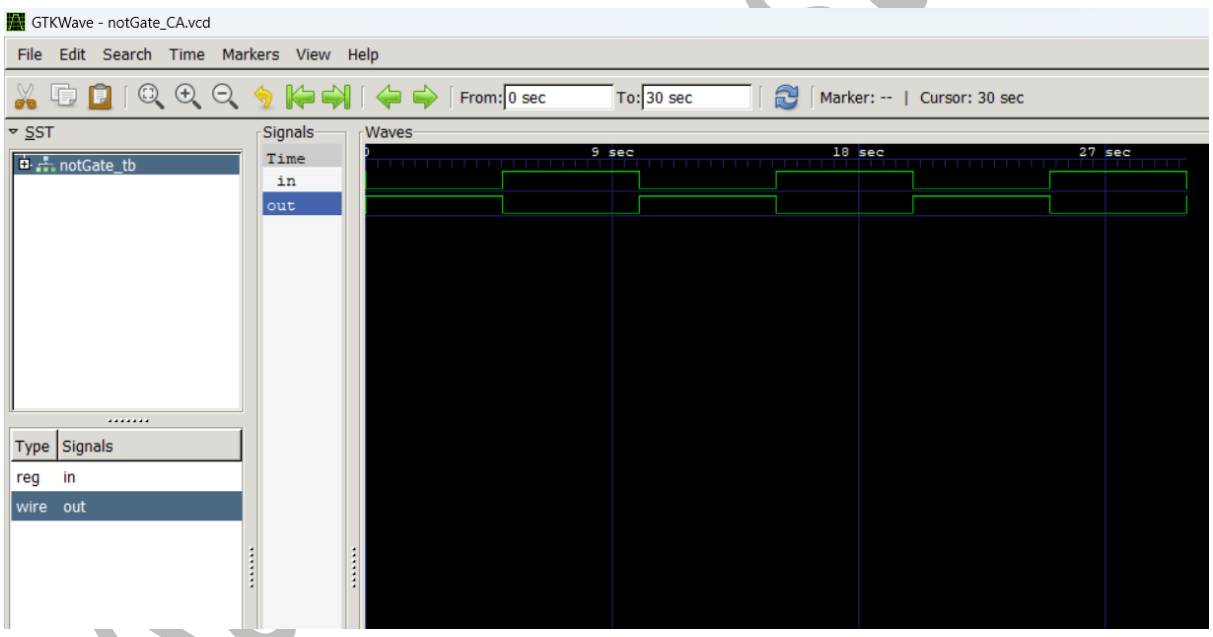
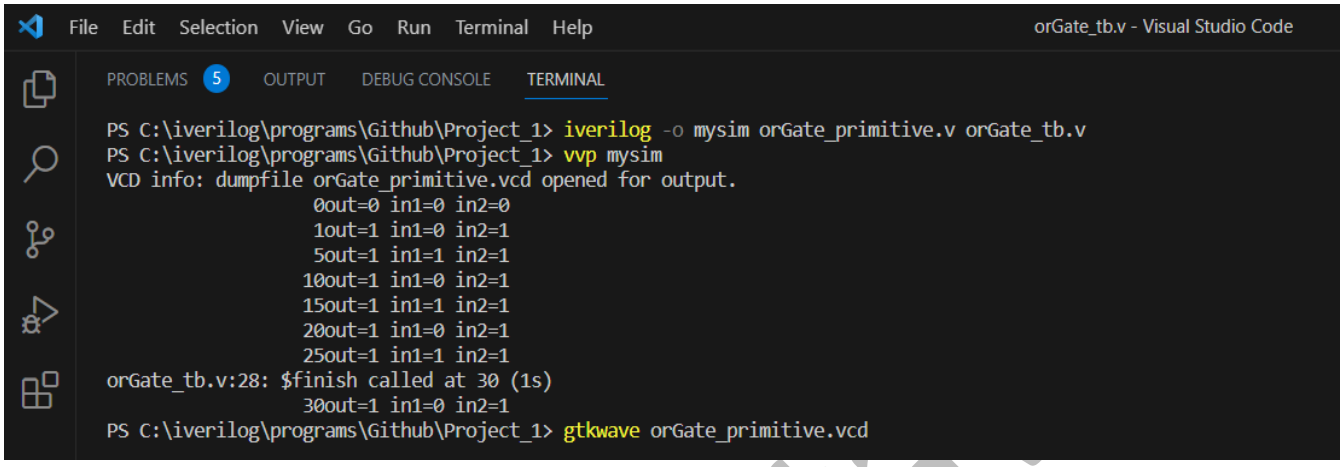
OUTPUTS:

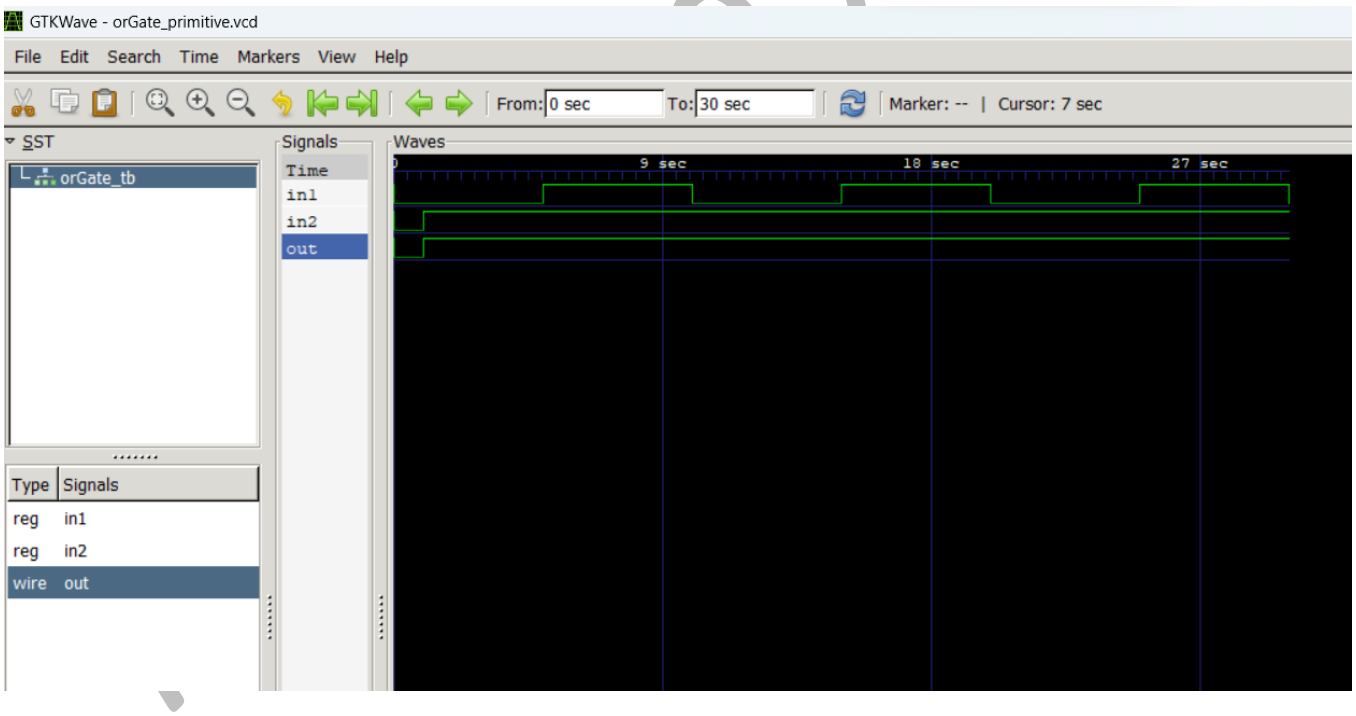
1. NOT GATE



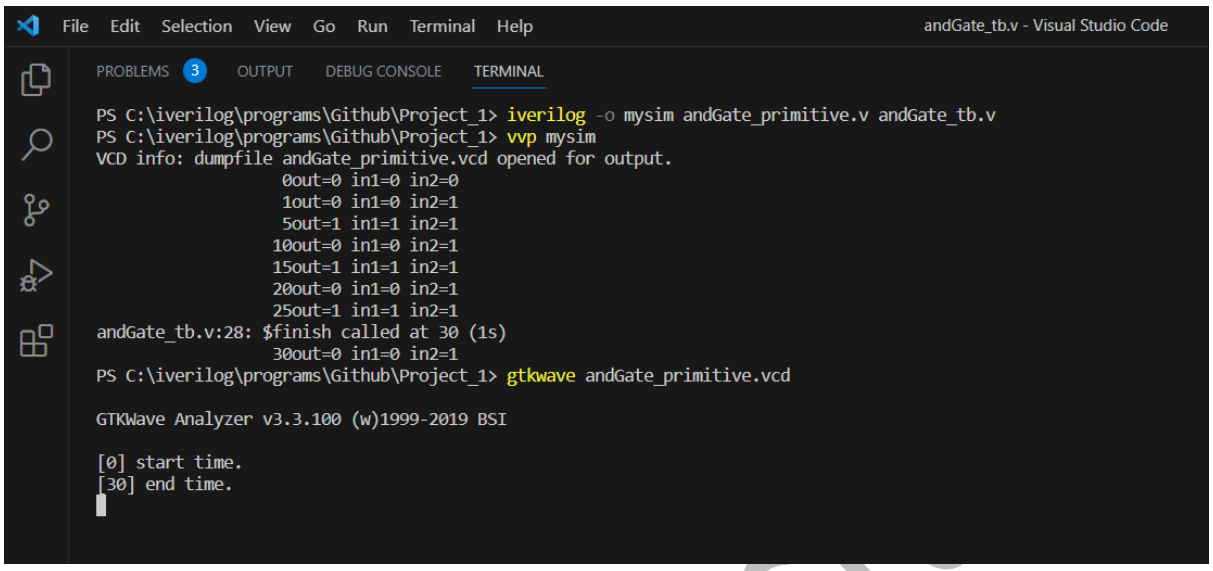


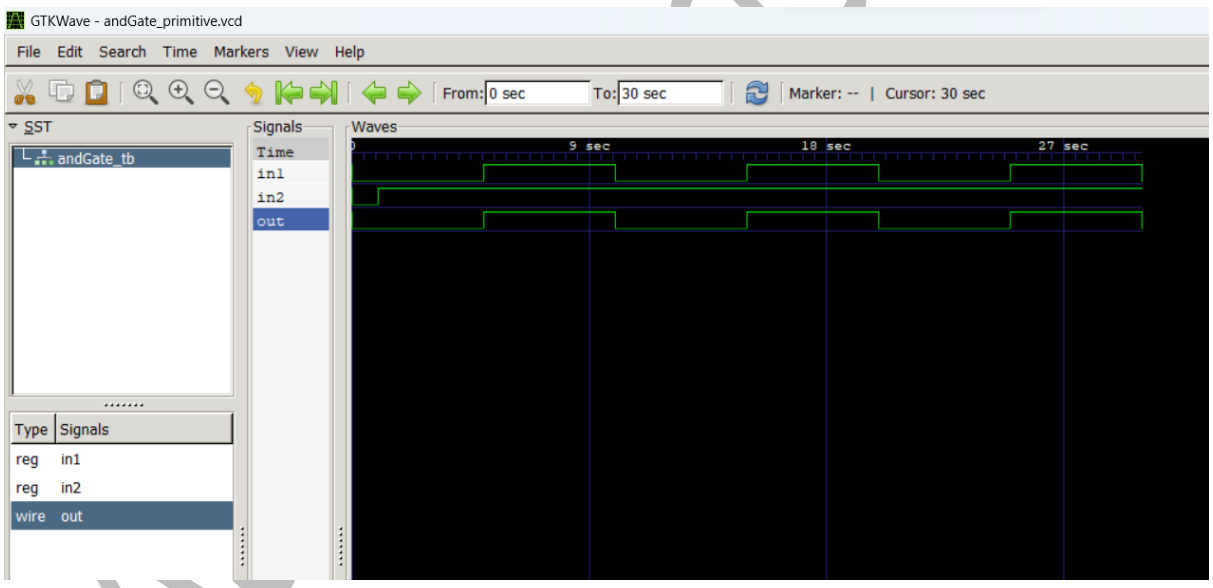
2. OR GATE


File Edit Selection View Go Run Terminal Help
orGate_tb.v - Visual Studio Code
PROBLEMS 5 OUTPUT DEBUG CONSOLE TERMINAL
PS C:\iverilog\programs\Github\Project_1> iverilog -o mysim orGate_primitive.v orGate_tb.v
PS C:\iverilog\programs\Github\Project_1> vvp mysim
VCD info: dumpfile orGate_primitive.vcd opened for output.
0out=0 in1=0 in2=0
1out=1 in1=0 in2=1
5out=1 in1=1 in2=1
10out=1 in1=0 in2=1
15out=1 in1=1 in2=1
20out=1 in1=0 in2=1
25out=1 in1=1 in2=1
orGate_tb.v:28: $finish called at 30 (1s)
30out=1 in1=0 in2=1
PS C:\iverilog\programs\Github\Project_1> gtkwave orGate_primitive.vcd

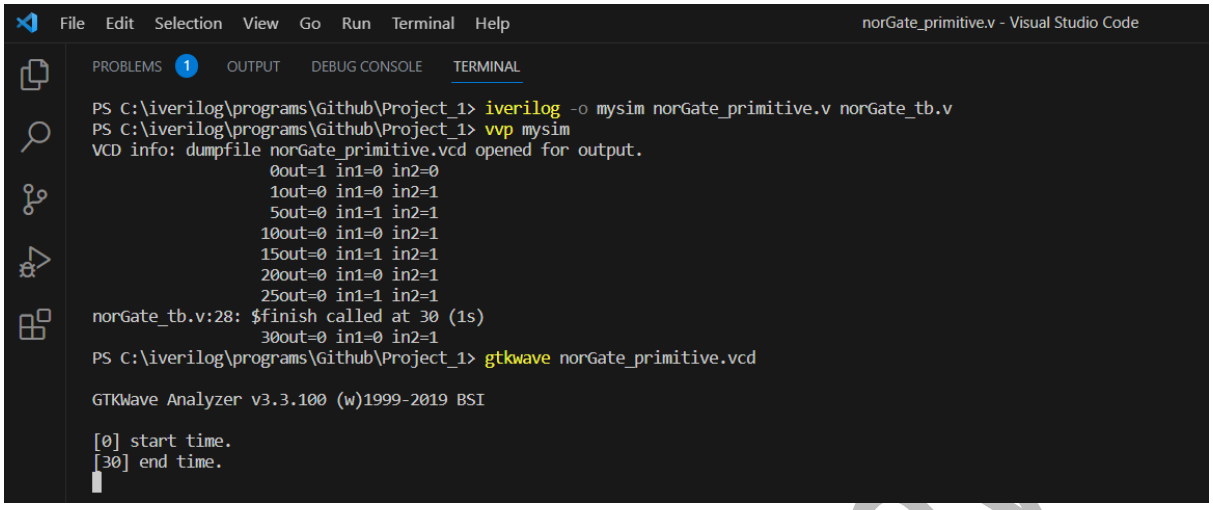

GTKWave - orGate_primitive.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 30 sec
Marker: -- | Cursor: 7 sec
SST
orGate_tb
Signals
Time
in1
in2
out
Waves
9 sec
18 sec
27 sec
Type Signals
reg in1
reg in2
wire out

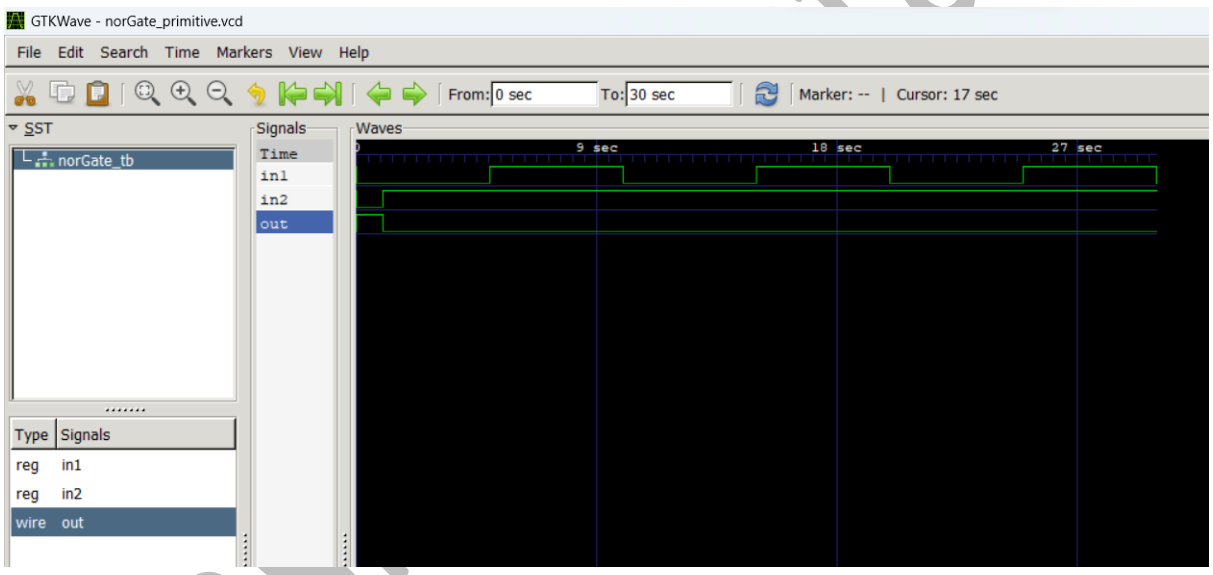
3. AND GATE


File Edit Selection View Go Run Terminal Help
andGate_tb.v - Visual Studio Code
PROBLEMS 3 OUTPUT DEBUG CONSOLE TERMINAL
PS C:\iverilog\programs\Github\Project_1> iverilog -o mysim andGate_primitive.v andGate_tb.v
PS C:\iverilog\programs\Github\Project_1> vvp mysim
VCD info: dumpfile andGate_primitive.vcd opened for output.
0out=0 in1=0 in2=0
1out=0 in1=0 in2=1
5out=1 in1=1 in2=1
10out=0 in1=0 in2=1
15out=1 in1=1 in2=1
20out=0 in1=0 in2=1
25out=1 in1=1 in2=1
andGate_tb.v:28: $finish called at 30 (1s)
30out=0 in1=0 in2=1
PS C:\iverilog\programs\Github\Project_1> gtkwave andGate_primitive.vcd
GTKWave Analyzer v3.3.100 (w)1999-2019 BSI
[0] start time.
[30] end time.

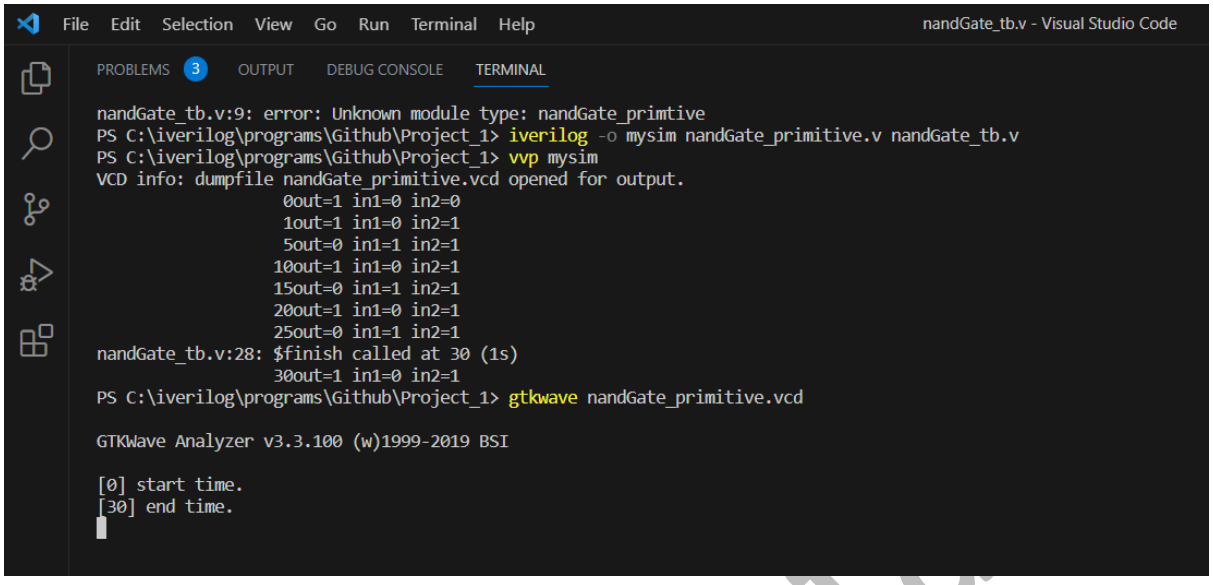

GTKWave - andGate_primitive.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 30 sec
Marker: -- | Cursor: 30 sec
SST
andGate_tb
Type Signals
reg in1
reg in2
wire out
Signals
Time
in1
in2
out
Waves
9 sec
18 sec
27 sec

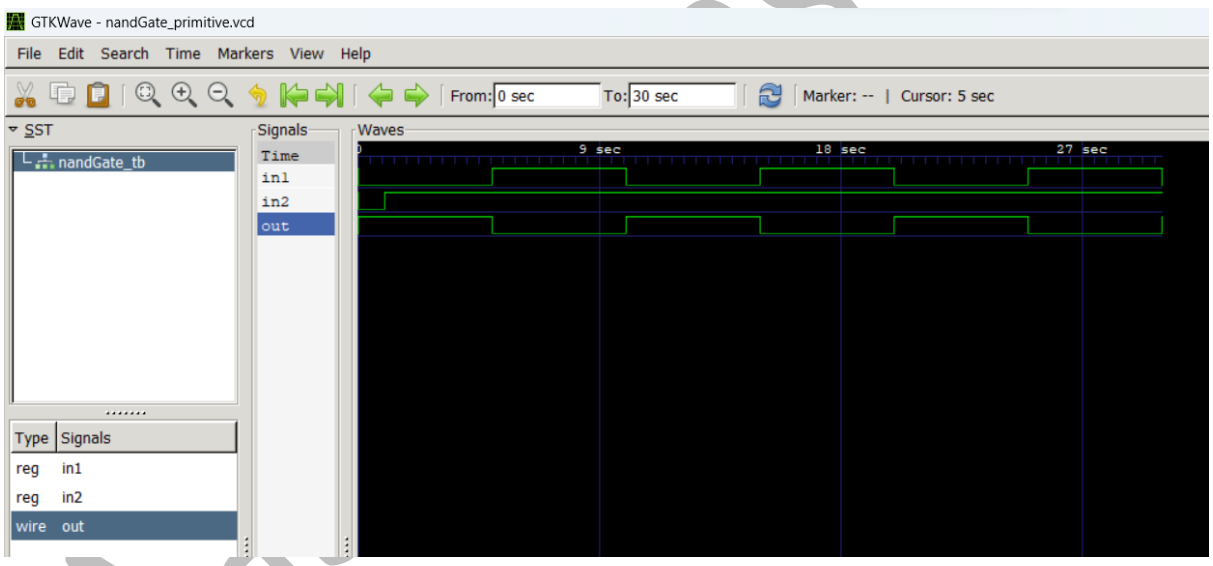
4. NOR GATE


File Edit Selection View Go Run Terminal Help
norGate_primitive.v - Visual Studio Code
PROBLEMS 1 OUTPUT DEBUG CONSOLE TERMINAL
PS C:\iverilog\programs\Github\Project_1> iverilog -o mysim norGate_primitive.v norGate_tb.v
PS C:\iverilog\programs\Github\Project_1> vvp mysim
VCD info: dumpfile norGate_primitive.vcd opened for output.
0out=1 in1=0 in2=0
1out=0 in1=0 in2=1
5out=0 in1=1 in2=1
10out=0 in1=0 in2=1
15out=0 in1=1 in2=1
20out=0 in1=0 in2=1
25out=0 in1=1 in2=1
norGate_tb.v:28: $finish called at 30 (1s)
30out=0 in1=0 in2=1
PS C:\iverilog\programs\Github\Project_1> gtkwave norGate_primitive.vcd
GTKWave Analyzer v3.3.100 (w)1999-2019 BSI
[0] start time.
[30] end time.

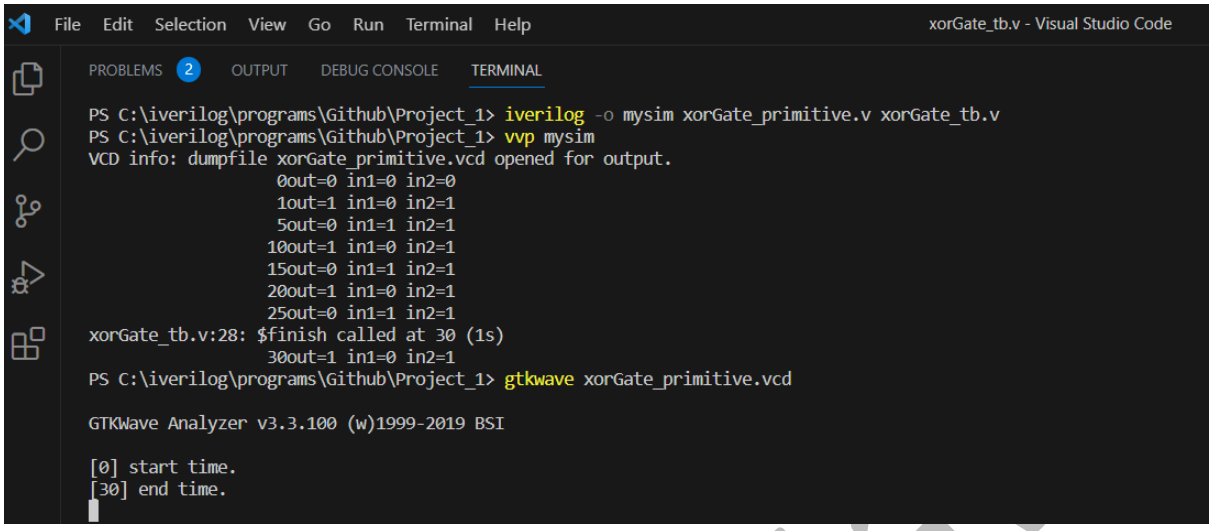

GTKWave - norGate_primitive.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 30 sec
Marker: -- | Cursor: 17 sec
SST
norGate_tb
Type Signals
reg in1
reg in2
wire out
Signals
Time
in1
in2
out
Waves
9 sec
18 sec
27 sec

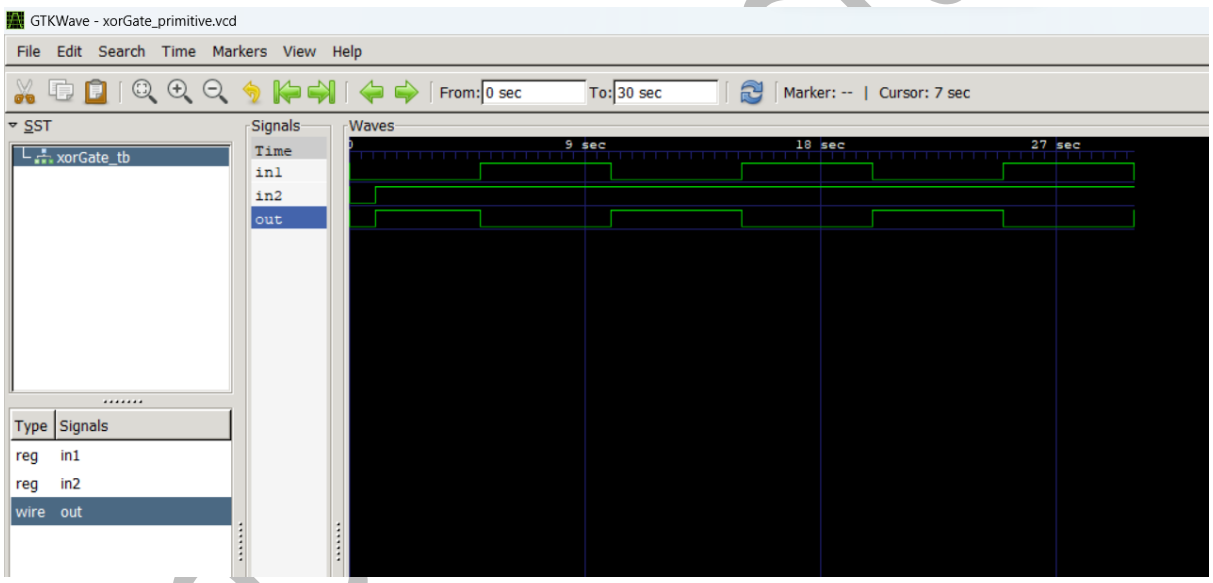
5. NAND GATE


File Edit Selection View Go Run Terminal Help
nandGate_tb.v - Visual Studio Code
PROBLEMS 3
OUTPUT
DEBUG CONSOLE
TERMINAL
nandGate_tb.v:9: error: Unknown module type: nandGate_primtive
PS C:\iverilog\programs\Github\Project_1> iverilog -o mysim nandGate_primitive.v nandGate_tb.v
PS C:\iverilog\programs\Github\Project_1> vvp mysim
VCD info: dumpfile nandGate_primitive.vcd opened for output.
0out=1 in1=0 in2=0
1out=1 in1=0 in2=1
5out=0 in1=1 in2=1
10out=1 in1=0 in2=1
15out=0 in1=1 in2=1
20out=1 in1=0 in2=1
25out=0 in1=1 in2=1
nandGate_tb.v:28: $finish called at 30 (1s)
30out=1 in1=0 in2=1
PS C:\iverilog\programs\Github\Project_1> gtkwave nandGate_primitive.vcd
GTKWave Analyzer v3.3.100 (w)1999-2019 BSI
[0] start time.
[30] end time.

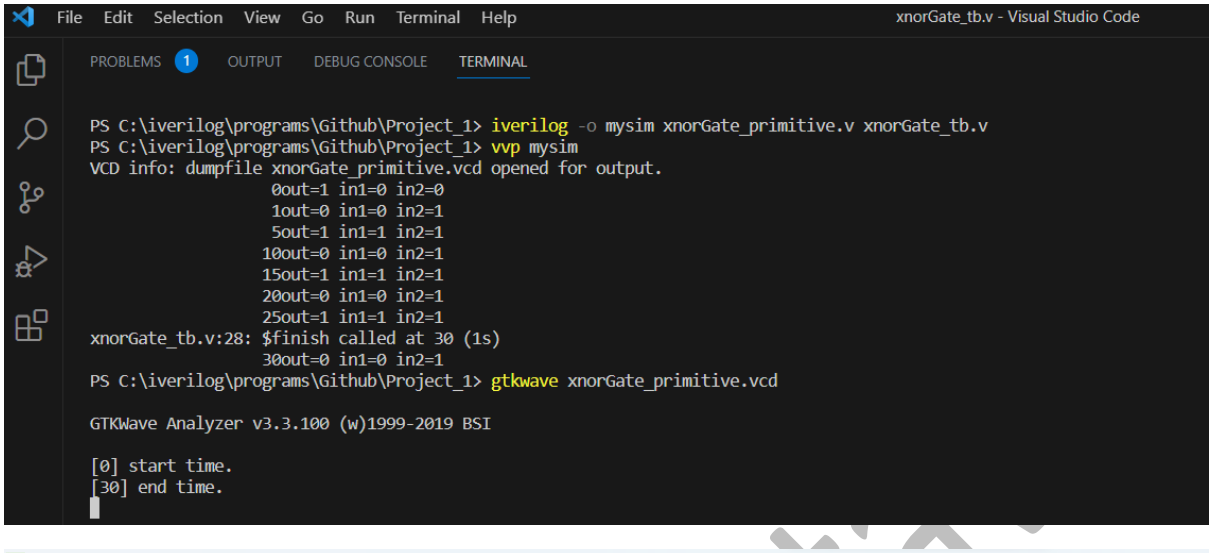

GTKWave - nandGate_primitive.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 30 sec
Marker: -- | Cursor: 5 sec
SST
nandGate_tb
Signals
Time
in1
in2
out
Waves
9 sec
18 sec
27 sec
Type Signals
reg in1
reg in2
wire out

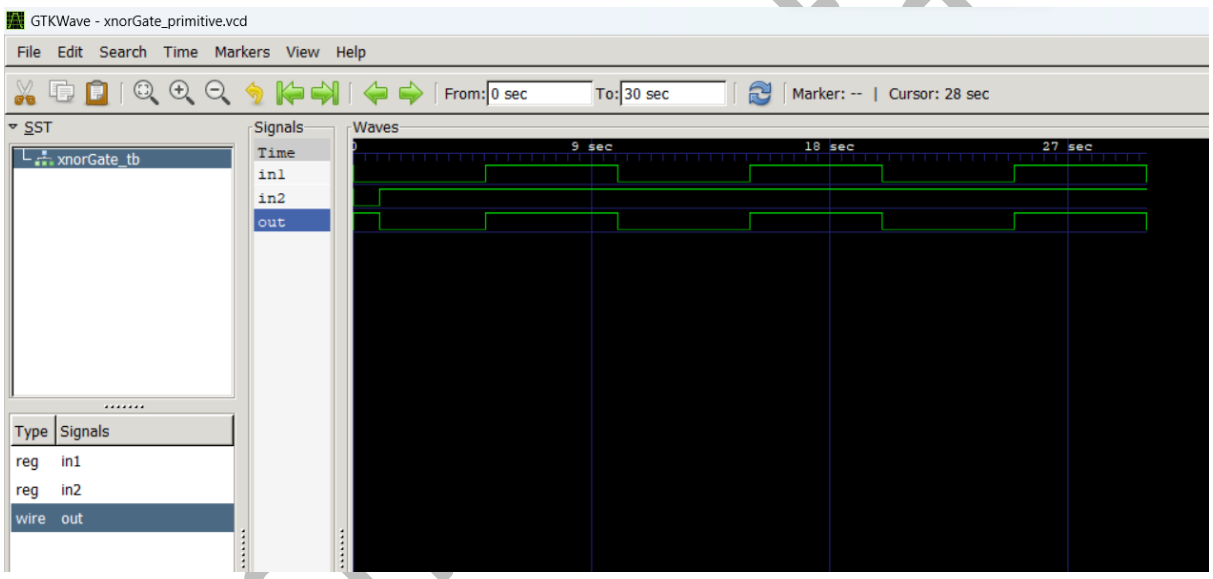
6. XOR GATE


File Edit Selection View Go Run Terminal Help
xorGate_tb.v - Visual Studio Code
PROBLEMS 2 OUTPUT DEBUG CONSOLE TERMINAL
PS C:\iverilog\programs\Github\Project_1> iverilog -o mysim xorGate_primitive.v xorGate_tb.v
PS C:\iverilog\programs\Github\Project_1> vvp mysim
VCD info: dumpfile xorGate_primitive.vcd opened for output.
0out=0 in1=0 in2=0
1out=1 in1=0 in2=1
5out=0 in1=1 in2=1
10out=1 in1=0 in2=1
15out=0 in1=1 in2=1
20out=1 in1=0 in2=1
25out=0 in1=1 in2=1
xorGate_tb.v:28: $finish called at 30 (1s)
30out=1 in1=0 in2=1
PS C:\iverilog\programs\Github\Project_1> gtkwave xorGate_primitive.vcd
GTKWave Analyzer v3.3.100 (w)1999-2019 BSI
[0] start time.
[30] end time.


GTKWave - xorGate_primitive.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 30 sec
Marker: -- | Cursor: 7 sec
SST
xorGate_tb
Signals
Time
in1
in2
out
Waves
9 sec
18 sec
27 sec
Type Signals
reg in1
reg in2
wire out

7. XNOR GATE


File Edit Selection View Go Run Terminal Help
xnorGate_tb.v - Visual Studio Code
PROBLEMS 1
OUTPUT
DEBUG CONSOLE
TERMINAL
PS C:\iverilog\programs\Github\Project_1> iverilog -o mysim xnorGate_primitive.v xnorGate_tb.v
PS C:\iverilog\programs\Github\Project_1> vvp mysim
VCD info: dumpfile xnorGate_primitive.vcd opened for output.
0out=1 in1=0 in2=0
1out=0 in1=0 in2=1
5out=1 in1=1 in2=1
10out=0 in1=0 in2=1
15out=1 in1=1 in2=1
20out=0 in1=0 in2=1
25out=1 in1=1 in2=1
xnorGate_tb.v:28: $finish called at 30 (1s)
30out=0 in1=0 in2=1
PS C:\iverilog\programs\Github\Project_1> gtkwave xnorGate_primitive.vcd
GTKWave Analyzer v3.3.100 (w)1999-2019 BSI
[0] start time.
[30] end time.


GTKWave - xnorGate_primitive.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 30 sec
Marker: -- | Cursor: 28 sec
SST
xnorGate_tb
Type Signals
reg in1
reg in2
wire out
Signals
Time
in1
in2
out
Waves
9 sec
18 sec
27 sec