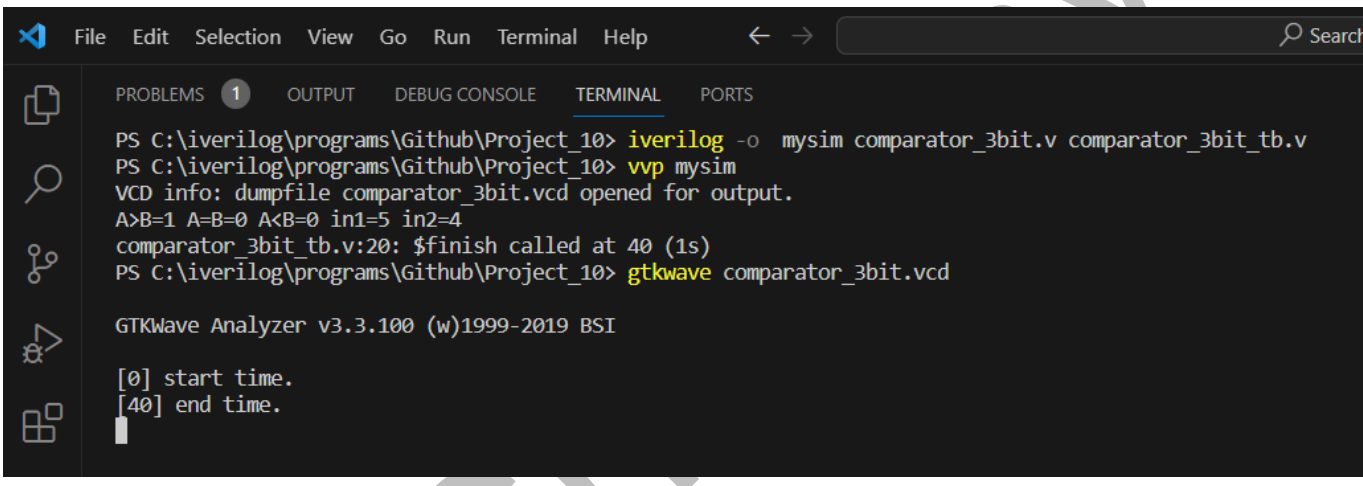
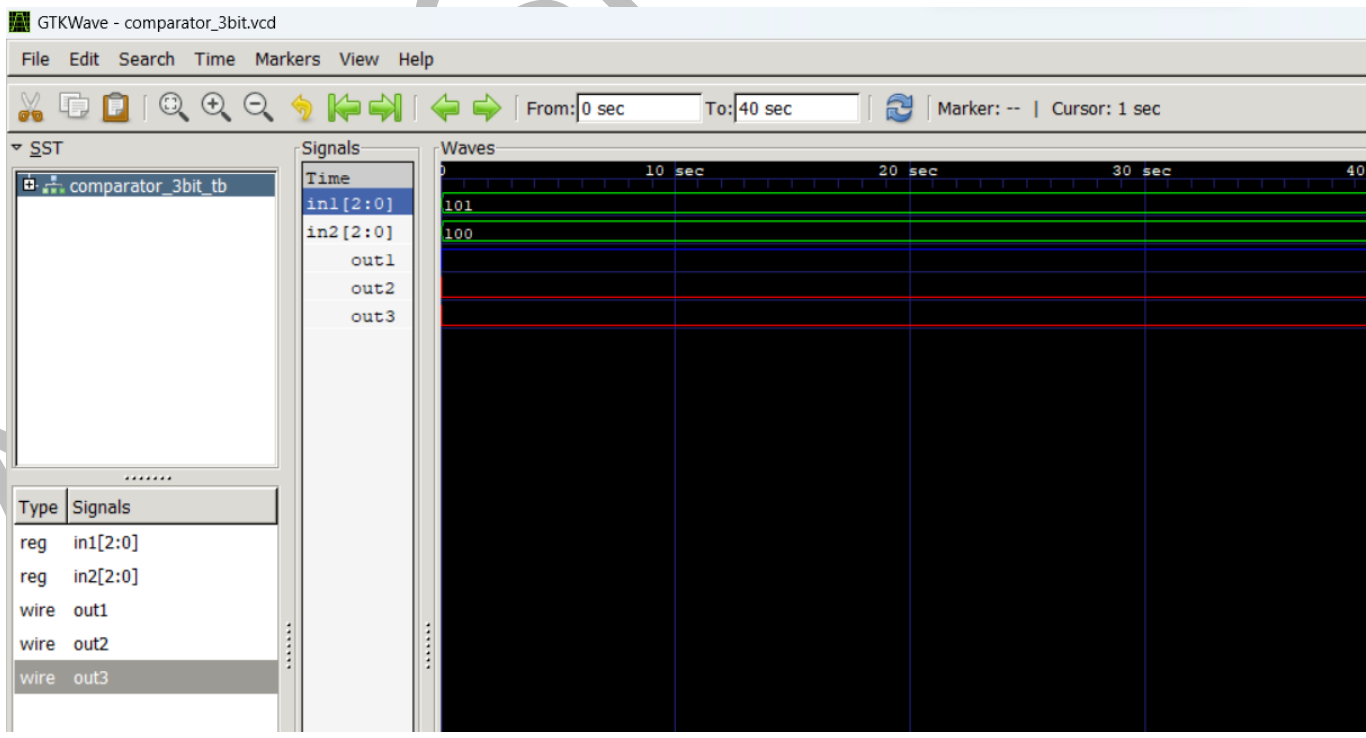
PROJECT-10
OUTPUT

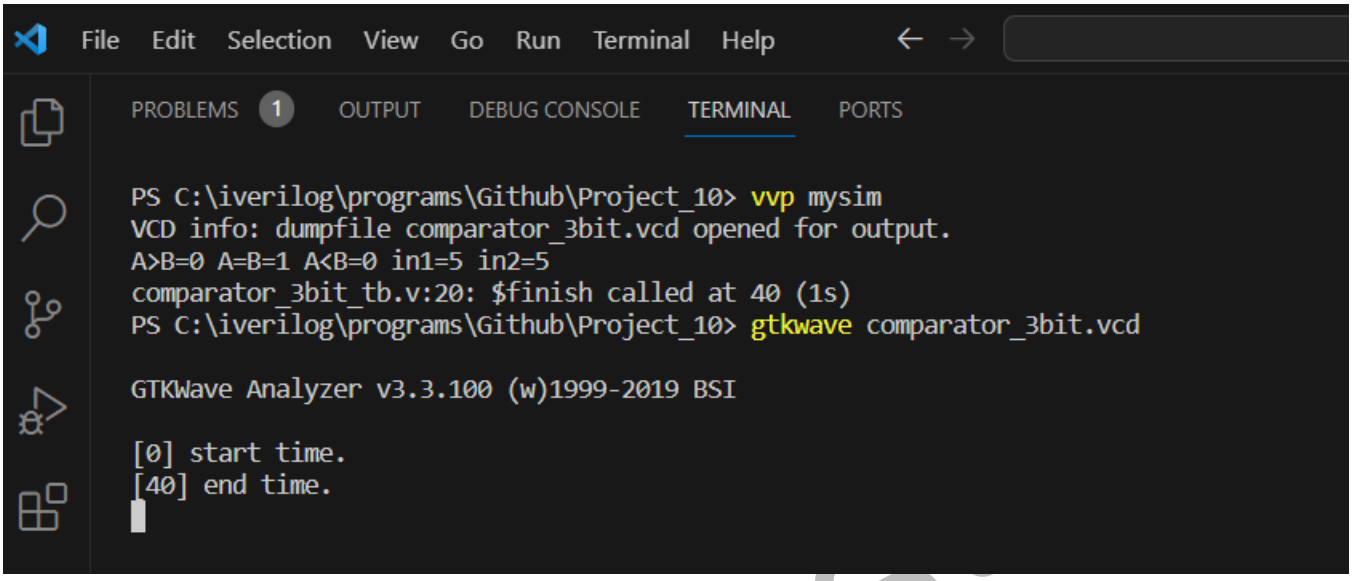
Made by: Aashi Srivastava
National Institute of Technology, Warangal

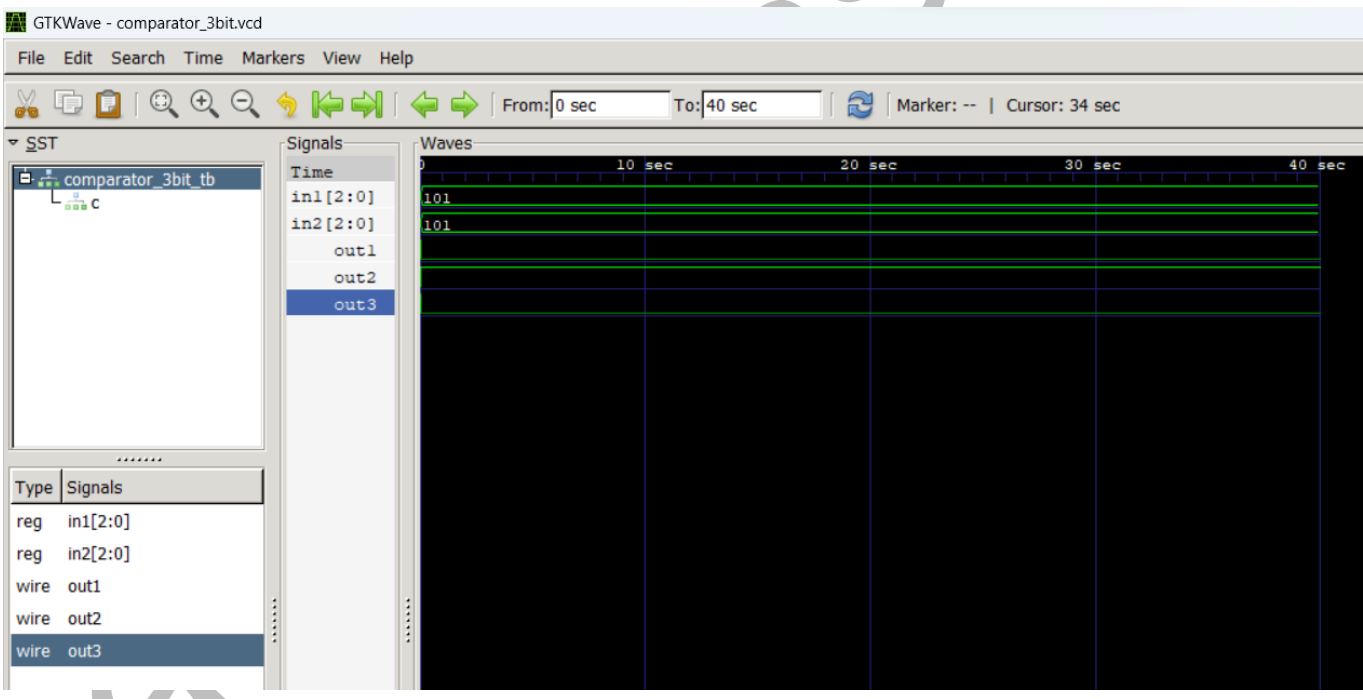
1. A>B



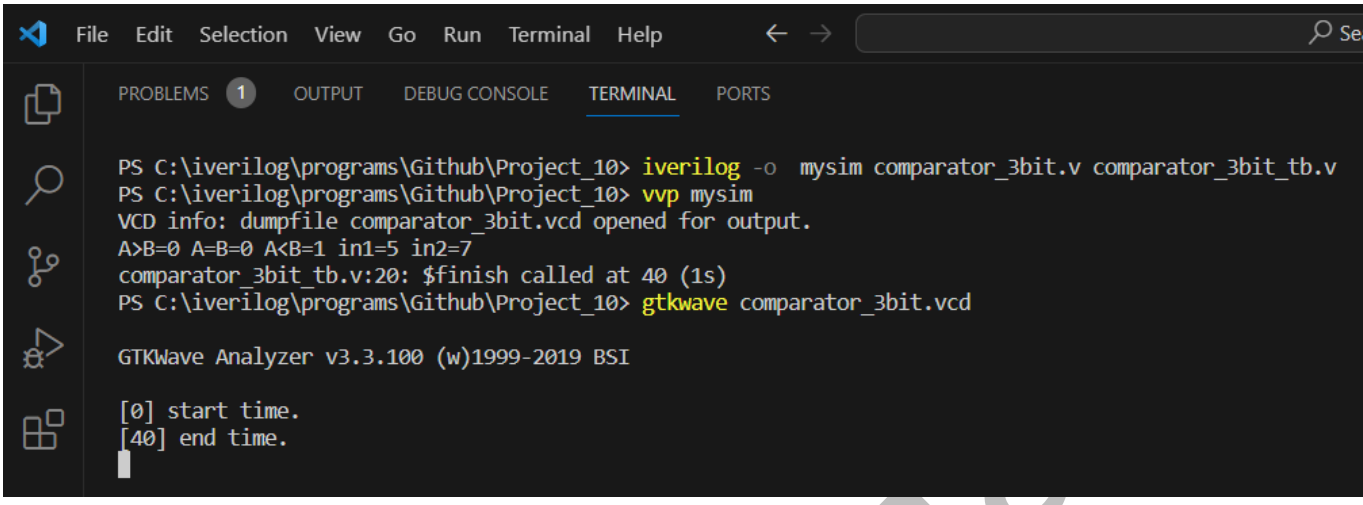


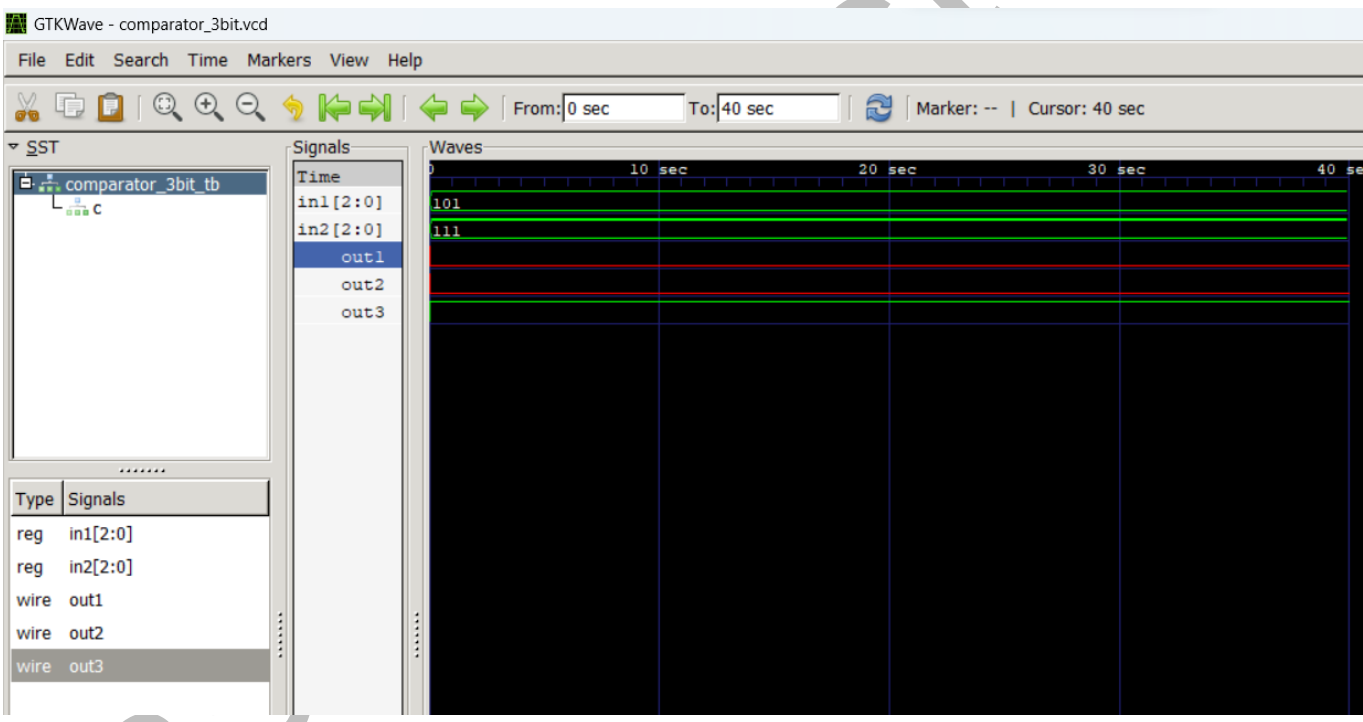
2. A=B


File Edit Selection View Go Run Terminal Help
PROBLEMS 1 OUTPUT DEBUG CONSOLE TERMINAL PORTS
PS C:\iverilog\programs\Github\Project_10> vvp mysim
VCD info: dumpfile comparator_3bit.vcd opened for output.
A>B=0 A=B=1 A<B=0 in1=5 in2=5
comparator_3bit_tb.v:20: $finish called at 40 (1s)
PS C:\iverilog\programs\Github\Project_10> gtkwave comparator_3bit.vcd
GTKWave Analyzer v3.3.100 (w)1999-2019 BSI
[0] start time.
[40] end time.


GTKWave - comparator_3bit.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 40 sec
Marker: -- | Cursor: 34 sec
SST
comparator_3bit_tb
c
Signals
Time
in1[2:0]
in2[2:0]
out1
out2
out3
Waves
10 sec
20 sec
30 sec
40 sec
101
101
Type Signals
reg in1[2:0]
reg in2[2:0]
wire out1
wire out2
wire out3

3. A<B


File Edit Selection View Go Run Terminal Help
PROBLEMS 1 OUTPUT DEBUG CONSOLE TERMINAL PORTS
PS C:\iverilog\programs\Github\Project_10> iverilog -o mysim comparator_3bit.v comparator_3bit_tb.v
PS C:\iverilog\programs\Github\Project_10> vvp mysim
VCD info: dumpfile comparator_3bit.vcd opened for output.
A>B=0 A=B=0 A<B=1 in1=5 in2=7
comparator_3bit_tb.v:20: $finish called at 40 (1s)
PS C:\iverilog\programs\Github\Project_10> gtkwave comparator_3bit.vcd
GTKWave Analyzer v3.3.100 (w)1999-2019 BSI
[0] start time.
[40] end time.


GTKWave - comparator_3bit.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 40 sec
Marker: -- | Cursor: 40 sec
SST
comparator_3bit_tb
c
Type Signals
reg in1[2:0]
reg in2[2:0]
wire out1
wire out2
wire out3
Signals
Time
in1[2:0]
in2[2:0]
out1
out2
out3
Waves
10 sec
20 sec
30 sec
101
111