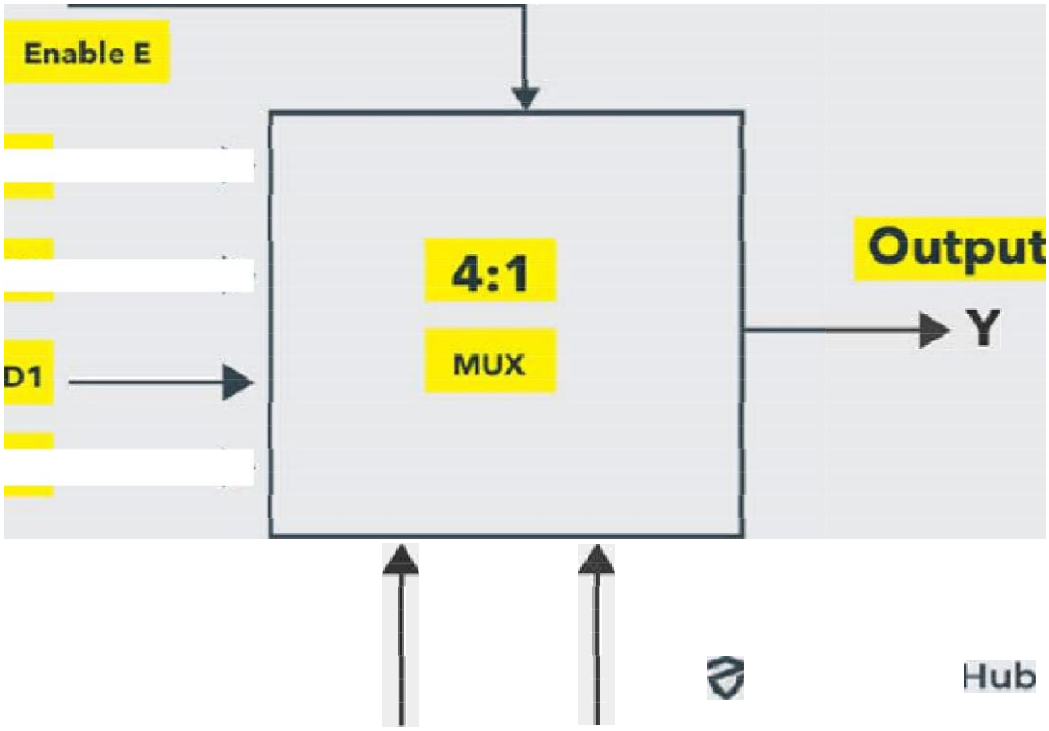
# PROJECT NO. – 11(b)

AIM : To construct 4X1 multiplexer .

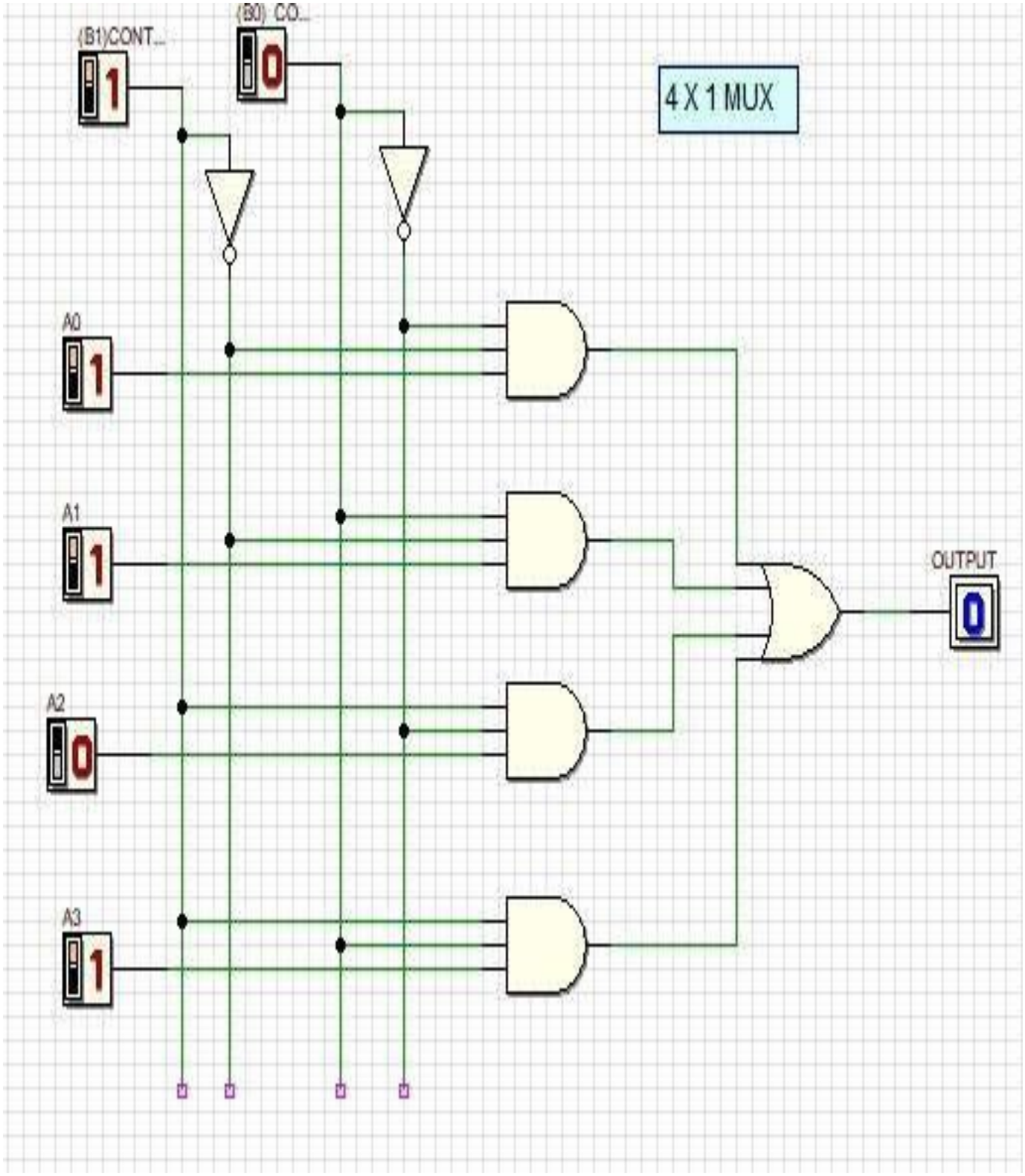
APPARATUS : input and output switch ; NOT,AND,and OR gate

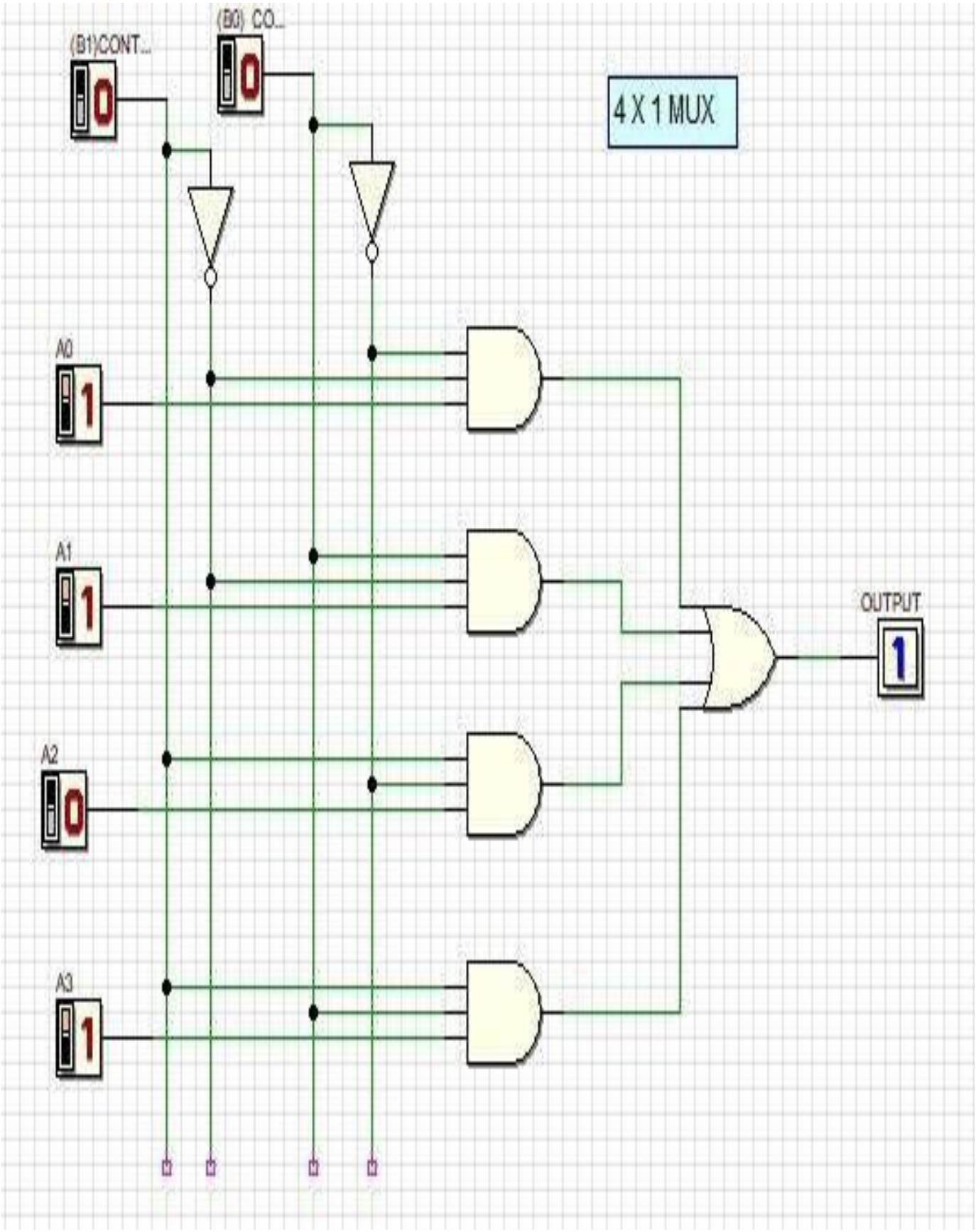
BLOCK DIAGRAM OF 4X1 MULTIPLEXER :

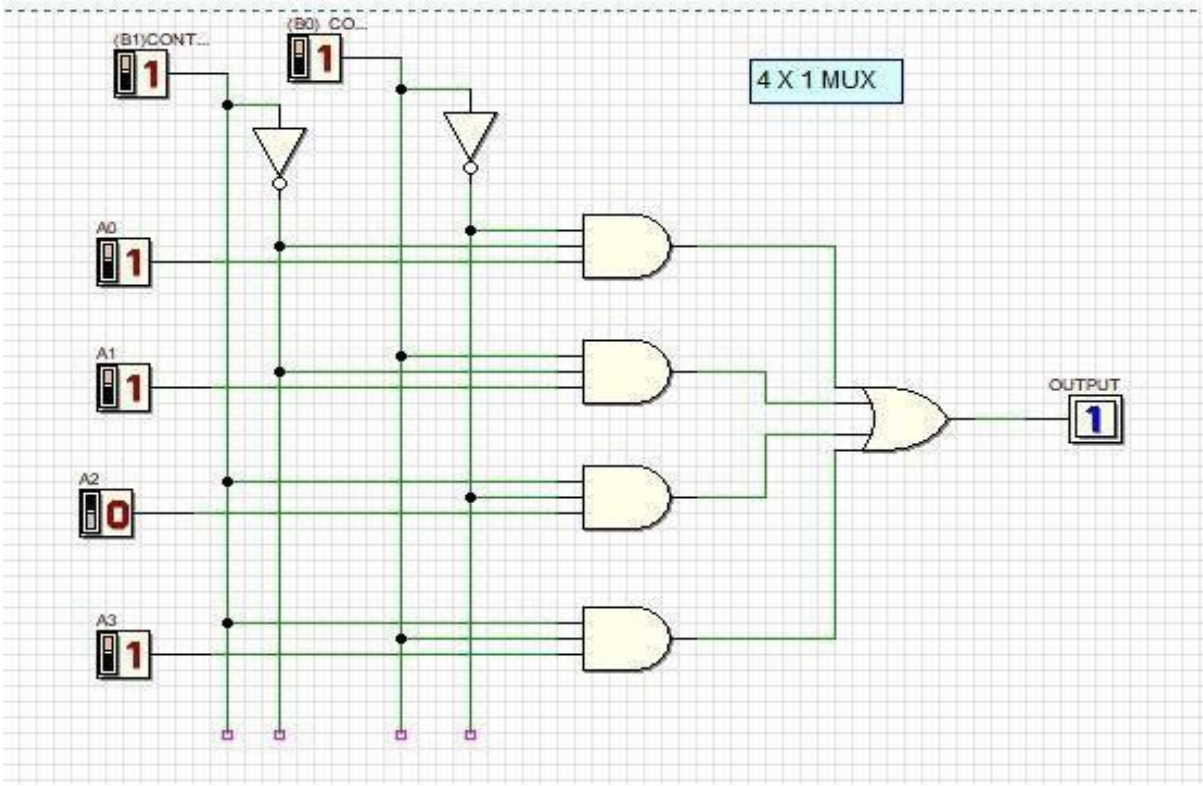
Block Diagram Of 4-To-1 Multiplexer



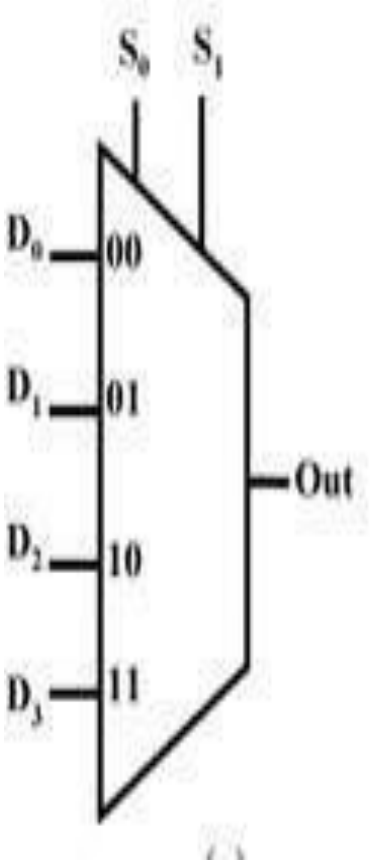
## CIRCUIT DIAGRAM OF 4X1 MUX :




(B1)CONT...
0
(B0) CO...
0
4 X 1 MUX
A0
1
A1
1
A2
0
A3
1
OUTPUT
1




## TRUTH TABLE FORN 4X1 MUX :




| $S_0$ | $S_1$ | Out |
|---|---|---|
| 0 | 0 | $D_0$ |
| 0 | 1 | $D_1$ |
| 1 | 0 | $D_2$ |
| 1 | 1 | $D_3$ |

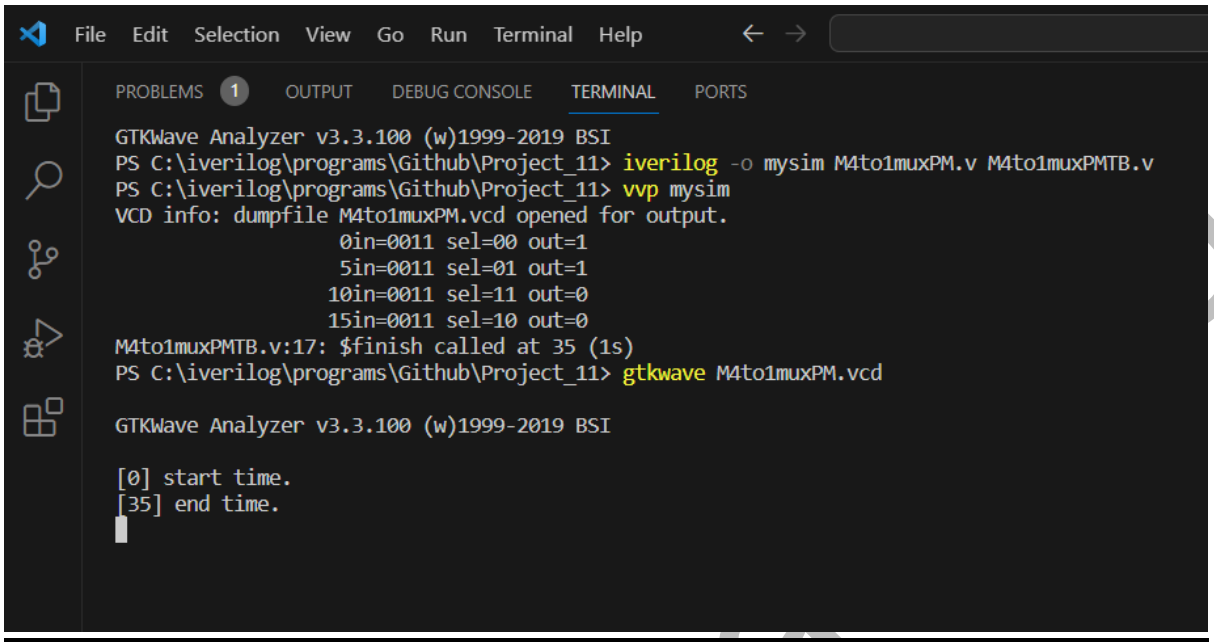
## Verilog Code:

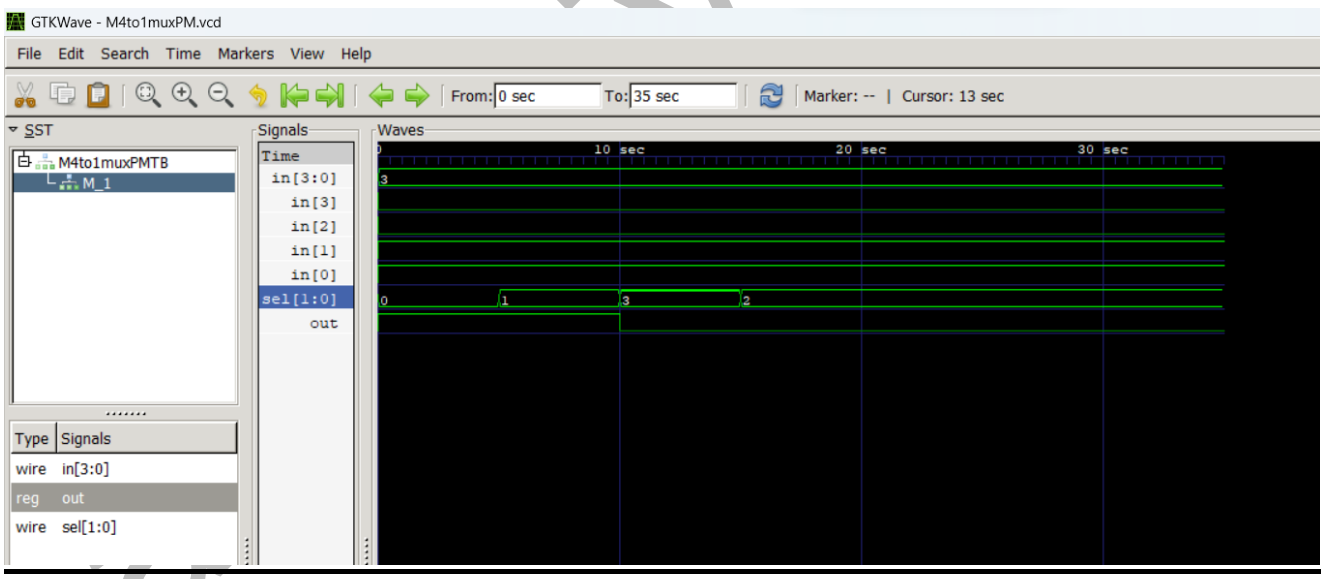
```
//Developed by: Aashi Srivastava
// TITLE:4 to 1 mux
// Date: 15.10.23, 09.53 IST
module M4to1muxPM (
    in, sel, out
);
    input [3:0] in;
    input [1:0 ]sel;
    output reg out;

    always @(*)
    begin
        if (sel==2'b00)
        out=in[0];
        else if (sel==2'b01)
        out=in[1];
        else if (sel==2'b10)
        out=in[2];
        else
        out=in[3];
    end

endmodule
```

## Test-Bench:

```
//Developed by: Aashi Srivastava
// TITLE: 4 to 1 mux test bench
// Date: 15.10.23, 09.53 IST
module M4to1muxPMTB (

);
    reg [3:0]in;
    reg [1:0]sel;
    wire out;

   M4to1muxPM M_1(in,sel,out);
   initial begin
    $dumpfile("M4to1muxPM.vcd");
    $dumpvars(0,M4to1muxPMTB);
    $monitor($time, "in=%b sel=%b out=%b", in, sel, out);
    in=4'b0011; sel=2'b00;
    #5 in=4'b0011; sel=2'b01;
     #5 in=4'b0011; sel=2'b11;
     #5 in=4'b0011; sel=2'b10;
    #20 $finish;
   end


endmodule
```

# OUTPUT:


File Edit Selection View Go Run Terminal Help
PROBLEMS 1 OUTPUT DEBUG CONSOLE TERMINAL PORTS
GTKWave Analyzer v3.3.100 (w)1999-2019 BSI
PS C:\iverilog\programs\Github\Project_11> iverilog -o mysim M4to1muxPM.v M4to1muxPMTB.v
PS C:\iverilog\programs\Github\Project_11> vvp mysim
VCD info: dumpfile M4to1muxPM.vcd opened for output.
0in=0011 sel=00 out=1
5in=0011 sel=01 out=1
10in=0011 sel=11 out=0
15in=0011 sel=10 out=0
M4to1muxPMTB.v:17: $finish called at 35 (1s)
PS C:\iverilog\programs\Github\Project_11> gtkwave M4to1muxPM.vcd
GTKWave Analyzer v3.3.100 (w)1999-2019 BSI
[0] start time.
[35] end time.


GTKWave - M4to1muxPM.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 35 sec
Marker: -- | Cursor: 13 sec
SST
M4to1muxPMTB
M_1
Type Signals
wire in[3:0]
reg out
wire sel[1:0]
Signals
Time
in[3:0]
in[3]
in[2]
in[1]
in[0]
sel[1:0]
out
Waves
10 sec
20 sec
30 sec