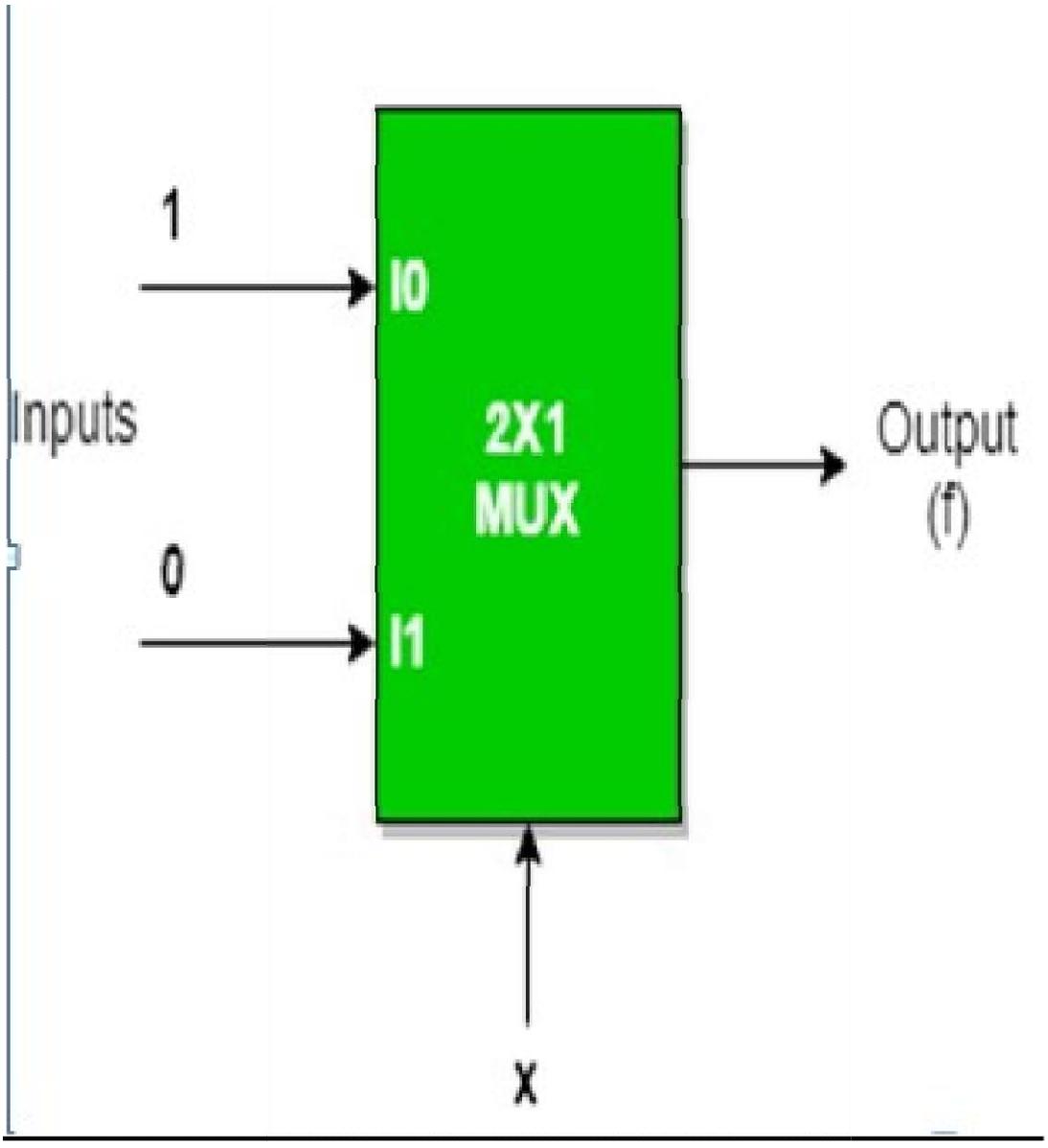
PROJECT NO. – 11(a)

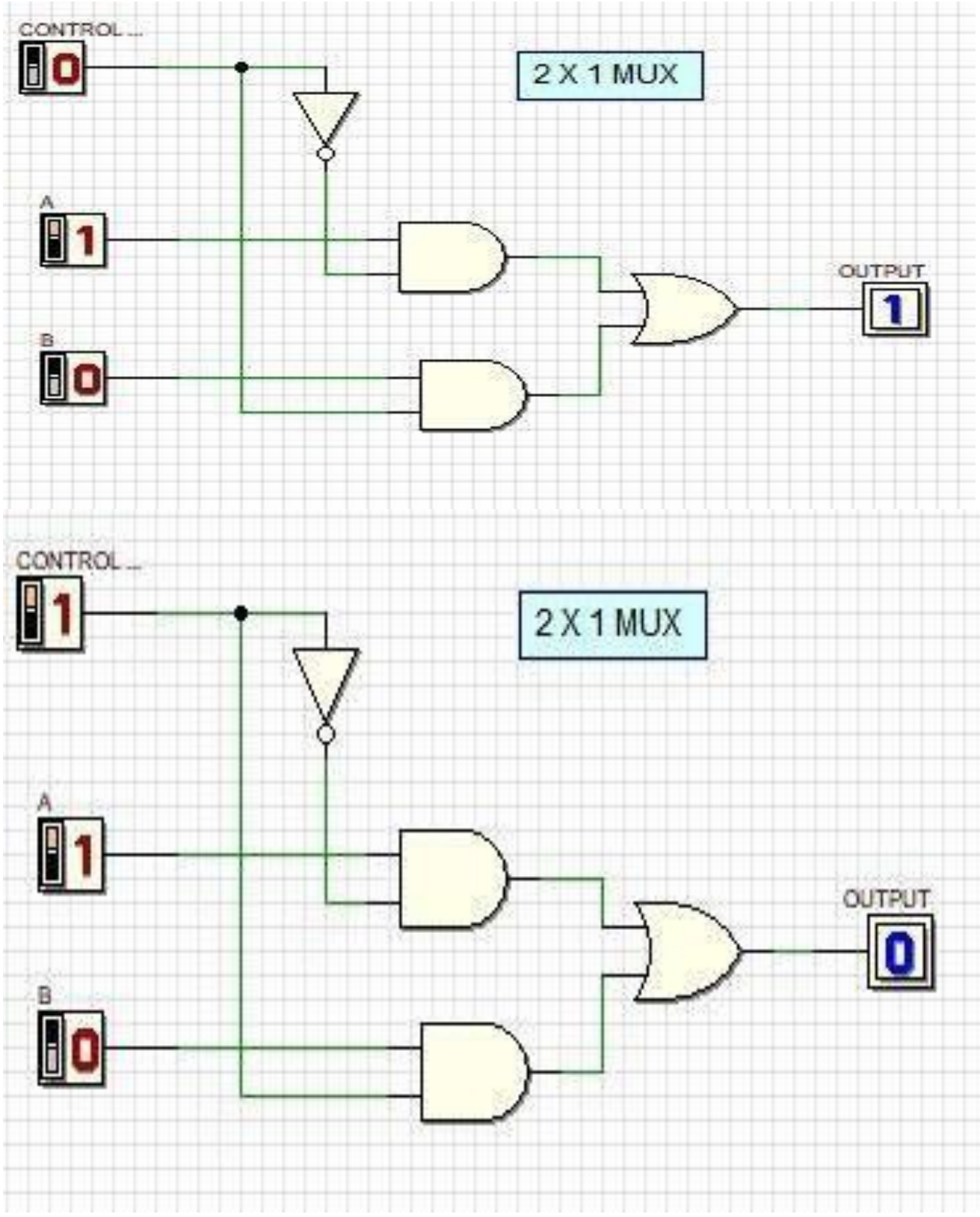
AIM : To construct 2X1multiplexer .

APPARATUS : input and output switch ; NOT,AND,and OR gate

BLOCK DIAGRAM OF 2X1 MULTIPLEXER :



CIRCUIT DIAGRAM OF 2X1 MUX :



TRUTH TABLE FORN 2X1 MUX :

	INPUT SELECT LINE	OUTPUT
1.	0	D0
2.	1	D1

Verilog Code:

```
//Developed by: Aashi Srivastava
// TITLE:2 to 1 multiplexer
// Date: 15.10.23, 09.53 IST
module M2to1mux (
    in, sel, out
);
    input [1:0] in;
    input sel;
    output out;

    assign out=in[sel];
endmodule
```

Test-Bench:

```
//Developed by: Aashi Srivastava
// TITLE: 2 to 1 multiplexer test bench
// Date: 15.10.23, 09.53 IST
module M2to1muxtest (

);
   reg [1:0]in;
   reg sel;
   wire out;

   M2to1mux M_1(.in(in),.sel(sel),.out(out));
   initial begin
    $dumpfile("M2to1mux.vcd");
    $dumpvars(0,M2to1muxtest);
    $monitor($time, "in=%b sel=%b out=%b", in, sel, out);
     in=2'b01; sel=1'b1;
     #5 in=2'b01; sel=1'b0;
     #10 $finish;
   end


endmodule
```

OUTPUT: