# PROJECT-2

# OUTPUTS

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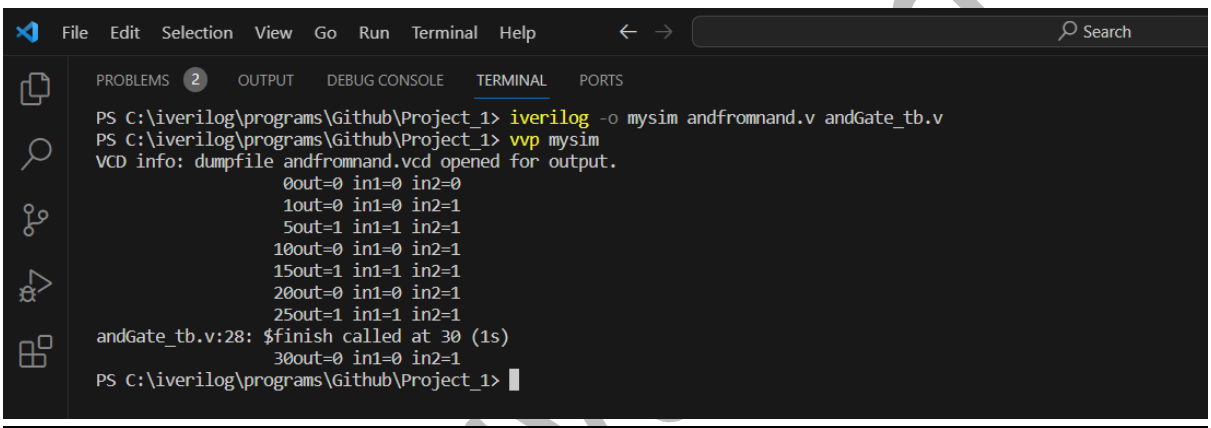
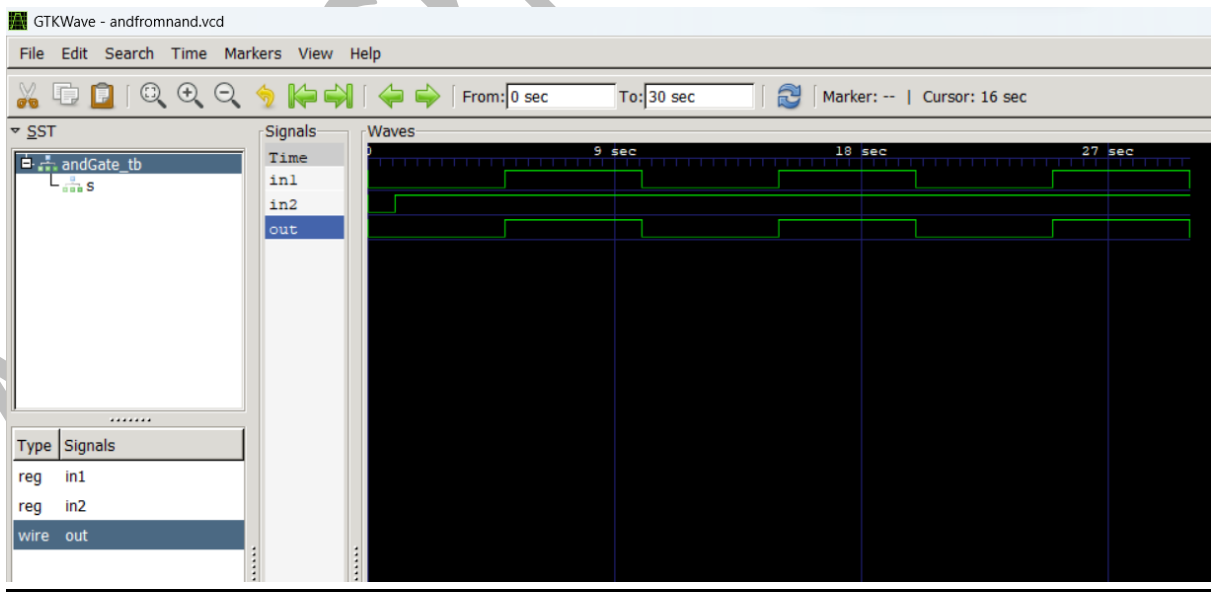
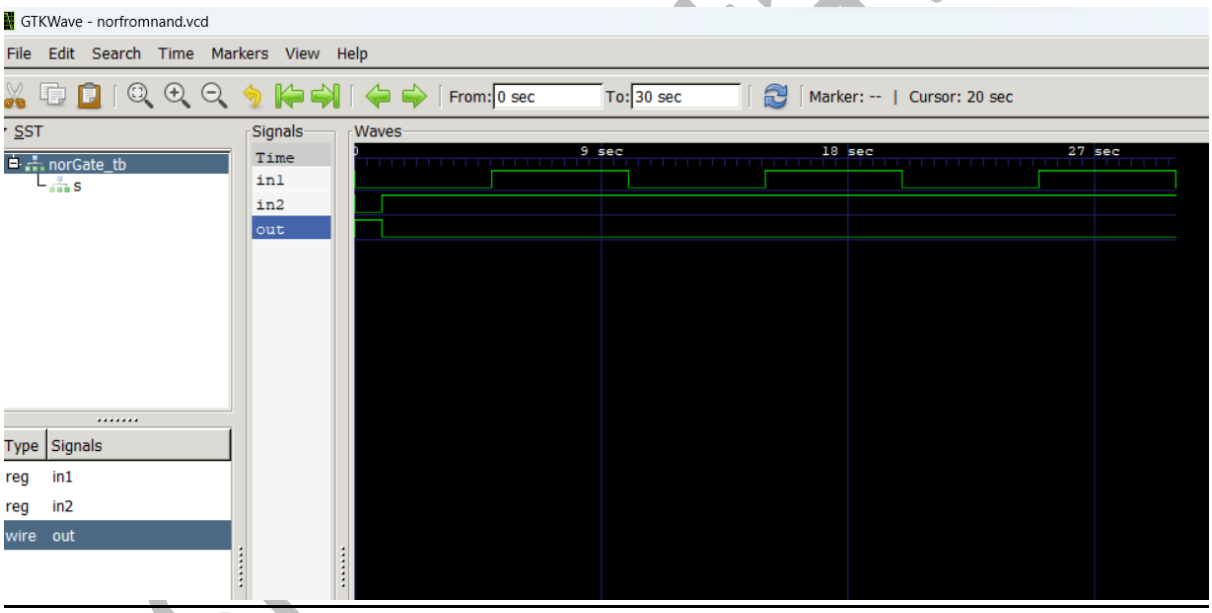
## 1. AND FROM NAND



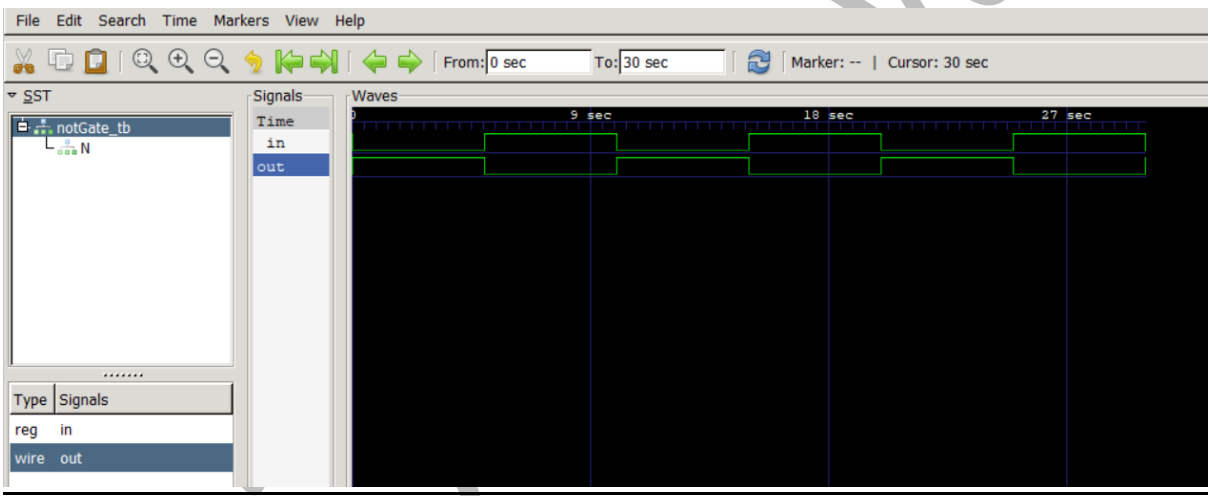
## 2. NOR FROM NAND

```
PS C:\iverilog\programs\Github\Project_1> iverilog -o mysim norfromnand.v norGate_tb.v
PS C:\iverilog\programs\Github\Project_1> vvp mysim
VCD info: dumpfile norfromnand.vcd opened for output.
                   0out=1 in1=0 in2=0
                   1out=0 in1=0 in2=1
                   5out=0 in1=1 in2=1
                  10out=0 in1=0 in2=1
                  15out=0 in1=1 in2=1
                  20out=0 in1=0 in2=1
                  25out=0 in1=1 in2=1
norGate_tb.v:28: $finish called at 30 (1s)
                  30out=0 in1=0 in2=1
PS C:\iverilog\programs\Github\Project_1>
```



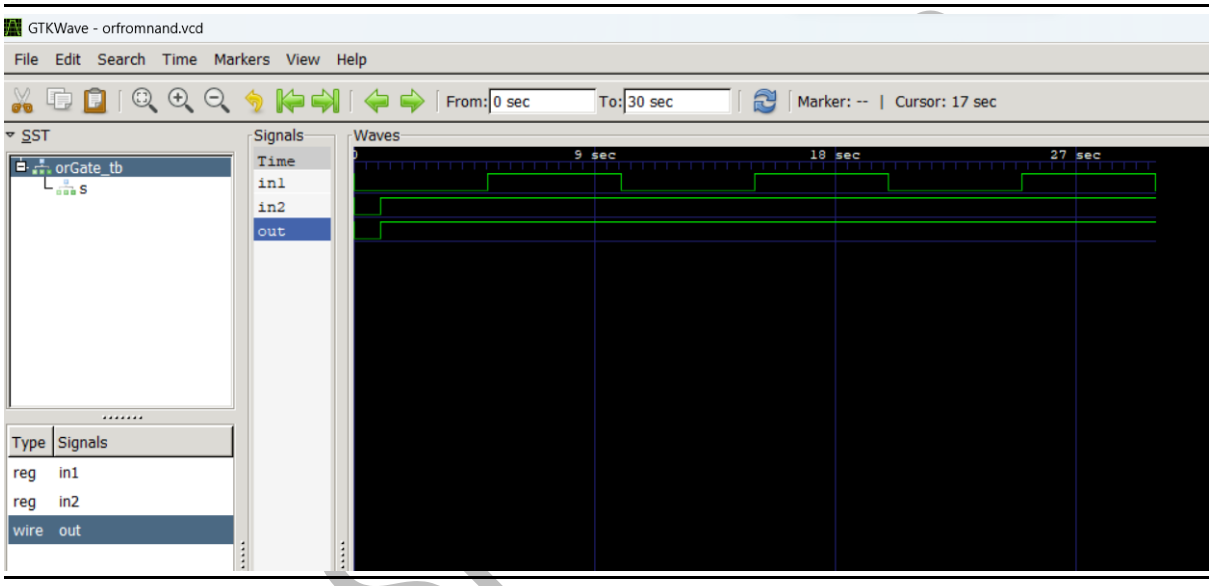
## 3. NOT FROM NAND

```
PS C:\iverilog\programs\Github\Project_1> iverilog -o mysim notfromnand.v notGate_tb.v
PS C:\iverilog\programs\Github\Project_1> vvp mysim
VCD info: dumpfile notfromnand.vcd opened for output.
                   0out=1 in=0
                   5out=0 in=1
                  10out=1 in=0
                  15out=0 in=1
                  20out=1 in=0
                  25out=0 in=1
notGate_tb.v:26: $finish called at 30 (1s)
                  30out=1 in=0
PS C:\iverilog\programs\Github\Project_1>
```



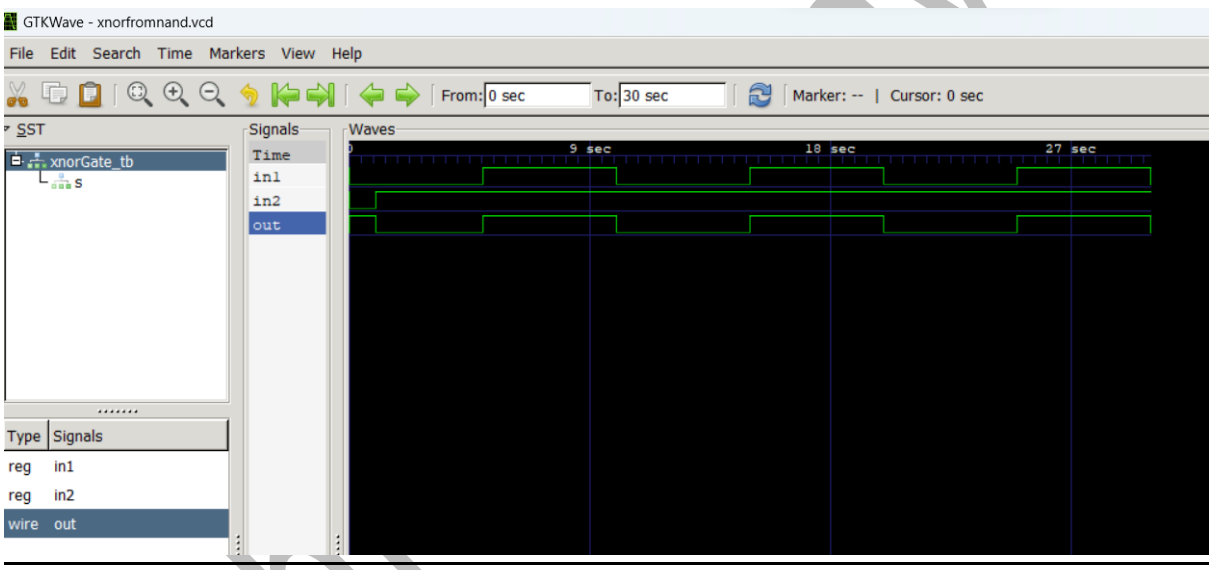
# 4. OR FROM NAND

```
PS C:\iverilog\programs\Github\Project_1> iverilog -o mysim orfromnand.v orGate_tb.v
PS C:\iverilog\programs\Github\Project_1> vvp mysim
VCD info: dumpfile orfromnand.vcd opened for output.
                   0out=0 in1=0 in2=0
                   1out=1 in1=0 in2=1
                   5out=1 in1=1 in2=1
                  10out=1 in1=0 in2=1
                  15out=1 in1=1 in2=1
                  20out=1 in1=0 in2=1
                  25out=1 in1=1 in2=1
orGate_tb.v:28: $finish called at 30 (1s)
```



## 5. XNOR FROM NAND

```
[0] start time.
PS C:\iverilog\programs\Github\Project_1> iverilog -o mysim xnorfromnand.v xnorGate_tb.v
PS C:\iverilog\programs\Github\Project_1> vvp mysim
VCD info: dumpfile xnorfromnand.vcd opened for output.
                   0out=1 in1=0 in2=0
                   1out=0 in1=0 in2=1
                   5out=1 in1=1 in2=1
                  10out=0 in1=0 in2=1
                  15out=1 in1=1 in2=1
                  20out=0 in1=0 in2=1
                  25out=1 in1=1 in2=1
xnorGate_tb.v:27: $finish called at 30 (1s)
                  30out=0 in1=0 in2=1
PS C:\iverilog\programs\Github\Project_1>
```



# 6. XOR FROM NAND

```
PS C:\iverilog\programs\Github\Project_1> iverilog -o mysim xorfromnand.v xorGate_tb.v
PS C:\iverilog\programs\Github\Project_1> vvp mysim
VCD info: dumpfile xorfromnand.vcd opened for output.
                   0out=0 in1=0 in2=0
                   1out=1 in1=0 in2=1
                   5out=0 in1=1 in2=1
                  10out=1 in1=0 in2=1
                  15out=0 in1=1 in2=1
                  20out=1 in1=0 in2=1
                  25out=0 in1=1 in2=1
xorGate_tb.v:28: $finish called at 30 (1s)
                  30out=1 in1=0 in2=1
PS C:\iverilog\programs\Github\Project_1>
```