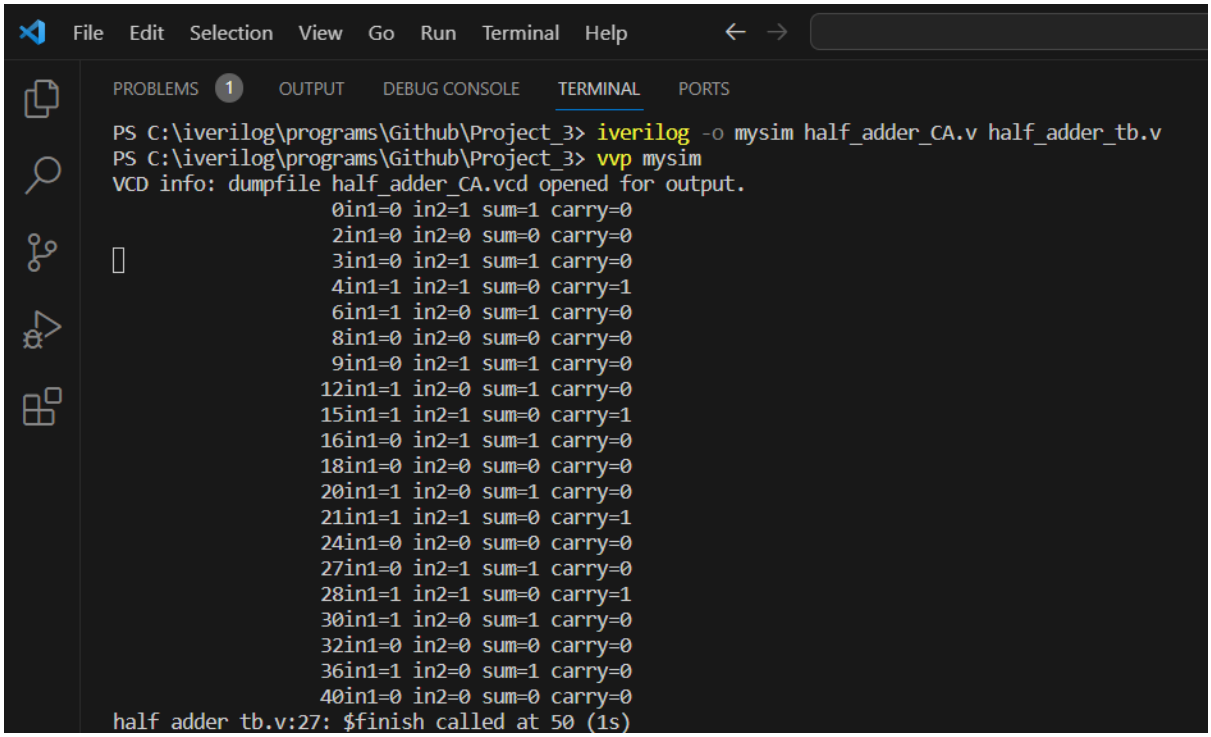
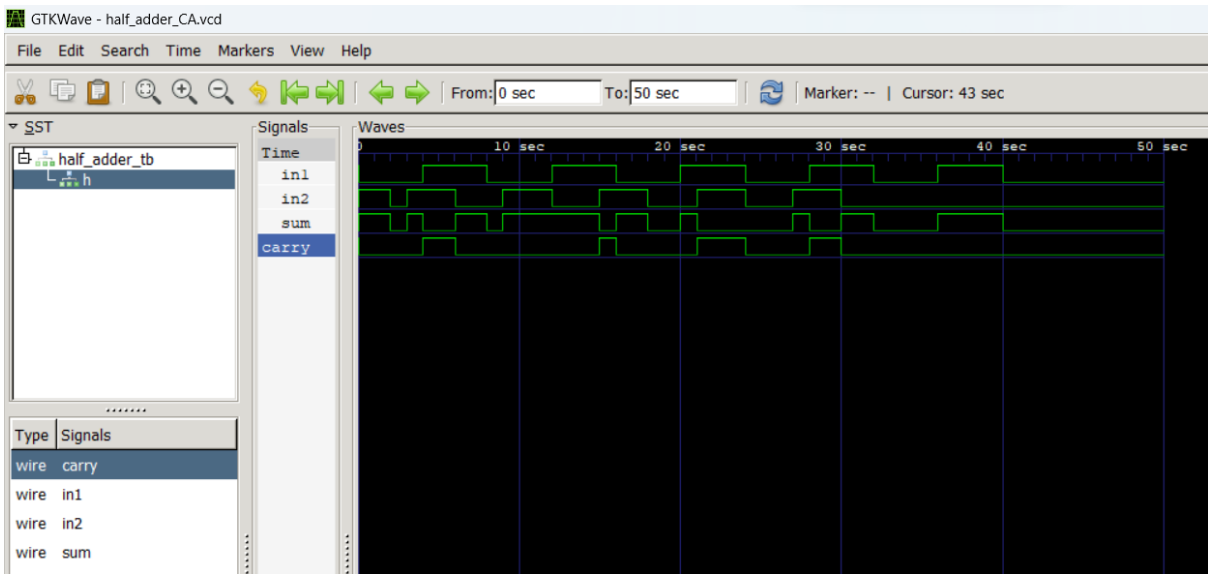
PROJECT-3 OUTPUTS

Developed by: Aashi Srivastava

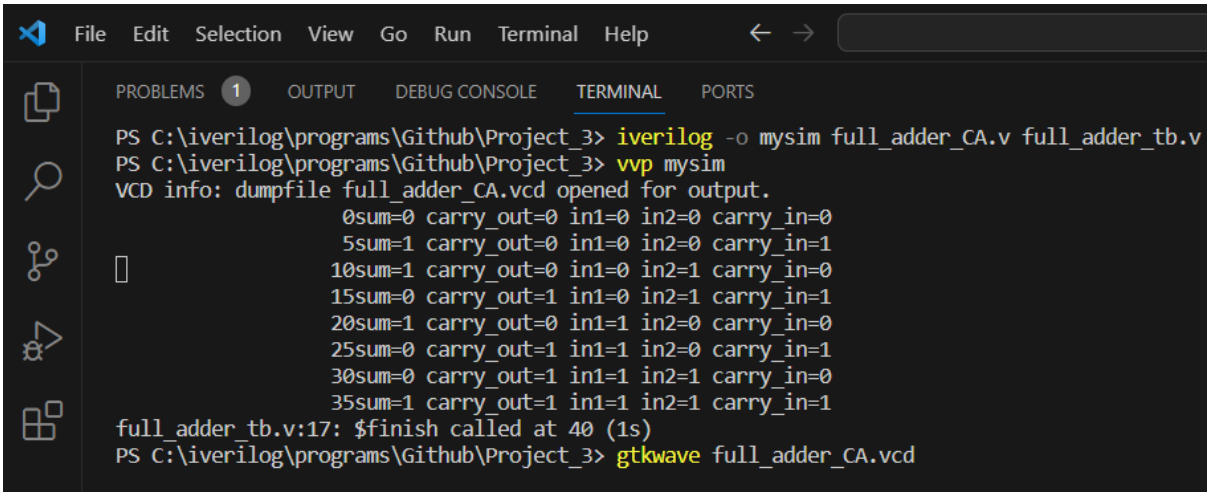
National Institute of Technology, Warangal

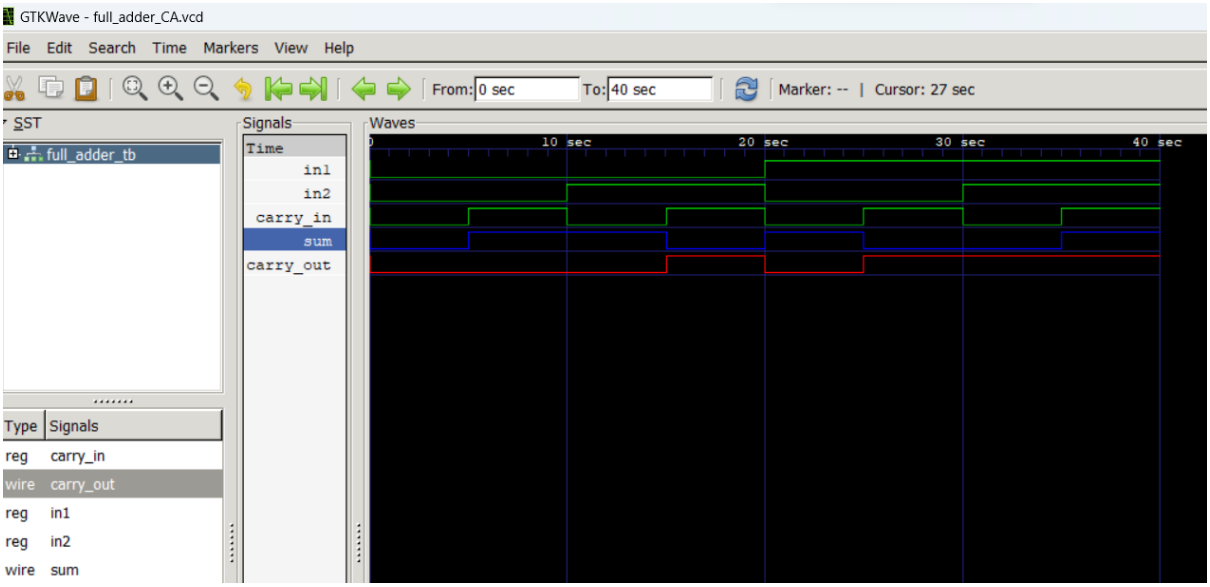
1. Half Adder





2. Full- Adder


File Edit Selection View Go Run Terminal Help
PROBLEMS 1 OUTPUT DEBUG CONSOLE TERMINAL PORTS
PS C:\iverilog\programs\Github\Project_3> iverilog -o mysim full_adder_CA.v full_adder_tb.v
PS C:\iverilog\programs\Github\Project_3> vvp mysim
VCD info: dumpfile full_adder_CA.vcd opened for output.
0sum=0 carry_out=0 in1=0 in2=0 carry_in=0
5sum=1 carry_out=0 in1=0 in2=0 carry_in=1
10sum=1 carry_out=0 in1=0 in2=1 carry_in=0
15sum=0 carry_out=1 in1=0 in2=1 carry_in=1
20sum=1 carry_out=0 in1=1 in2=0 carry_in=0
25sum=0 carry_out=1 in1=1 in2=0 carry_in=1
30sum=0 carry_out=1 in1=1 in2=1 carry_in=0
35sum=1 carry_out=1 in1=1 in2=1 carry_in=1
full_adder_tb.v:17: $finish called at 40 (1s)
PS C:\iverilog\programs\Github\Project_3> gtkwave full_adder_CA.vcd


GTKWave - full_adder_CA.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 40 sec
Marker: -- | Cursor: 27 sec
SST
full_adder_tb
Signals
Time
in1
in2
carry_in
sum
carry_out
Waves
10 sec
20 sec
30 sec
40 sec
Type Signals
reg carry_in
wire carry_out
reg in1
reg in2
wire sum