PROJECT NO. – 4

AIM : To design a full adder using half adder.

APPARATUS : Input and output switches ; wires for connection ; OR ,AND, NOR Gates; DEEDS simulator

TRUTH TABLE FOR FULL ADDER

INPUT			OUTPUT	
A	B	C	SUM (A+B+C)	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1

1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

KMAP FOR FULL ADDER (SUM)

		B'*(C)'	B'*(C)	B*(C)	B*(C)'	
A'		0	1	0	1	
A		1	0	1	0	

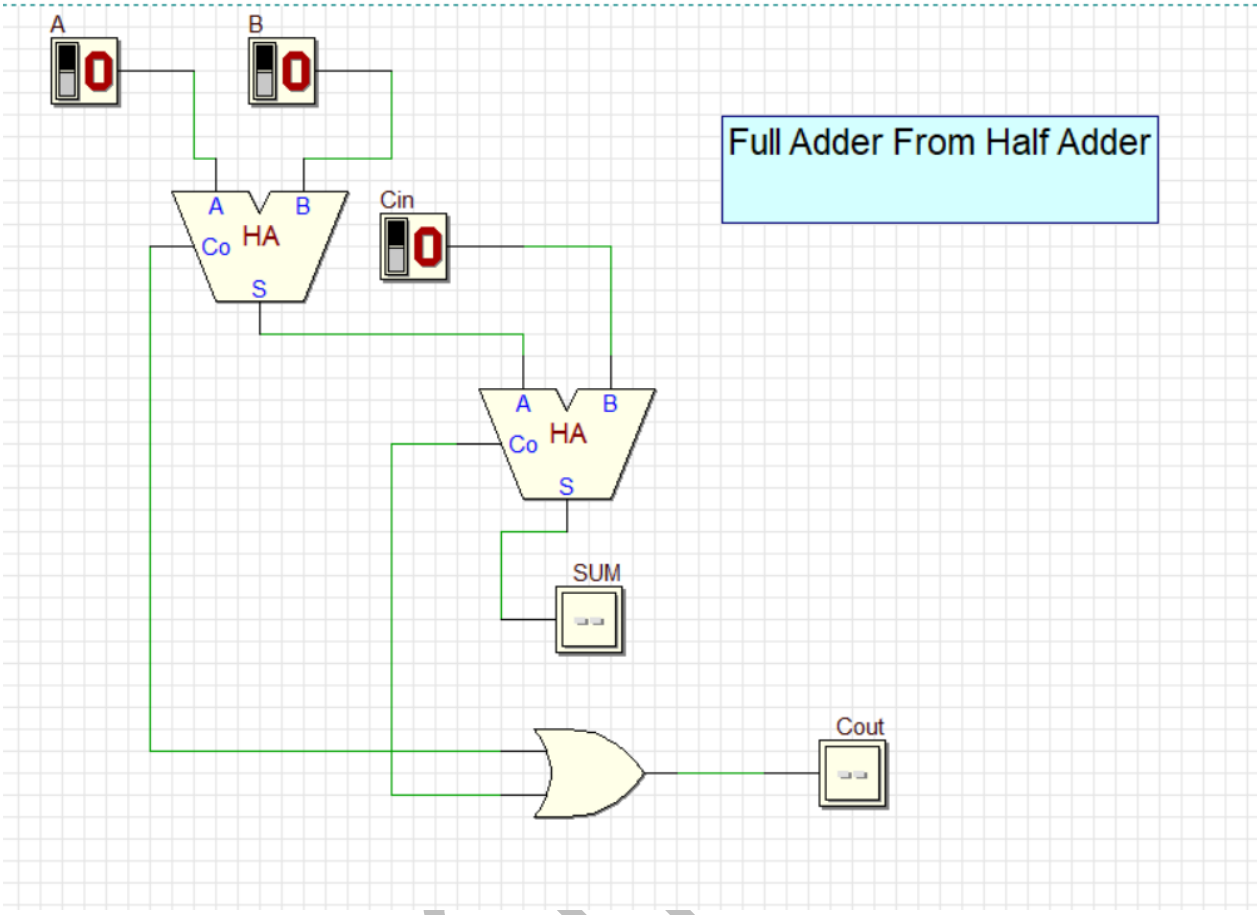
SIMPLIFING K MAP

SUM = (A ')*(B'*(C)+ B*(C)') + A*(B'*(C)'+ B*(C)) .

=A⊕ B⊕C

KMAP FOR FULL ADDER (CARRY)

		B'*(C)'	B'*C	B*C	B*(C)'	
A'		0	0	1	0	
A		0	1	1	1	



Verilog Code:

Full adder from Half Adder

```
//Developed by: Aashi Srivastava
// TITLE: Full adder from Half Adder
// Date: 10.10.23, 9:44 IST
module full_from_half (sum,carry_out,in1,in2,carry_in);
    input in1,in2,carry_in;
    output sum,carry_out;
    wire wire1,wire2,wire3;

    half_adder_CA h1(wire1,wire2,in1,in2);
    half_adder_CA h2(sum,wire3,wire1,carry_in);
    or o1(carry_out,wire2,wire3);

endmodule
module half_adder_CA(
    sum,carry,in1,in2
);
input in1,in2;
output sum, carry;

assign sum=in1^in2; //Sum of half adder is given by xor of the two inputs
assign carry=in1 & in2; // carry of the two half adder is given by the and of
the two inputs
endmodule
```

Test-Bench:

```
//Developed by: Aashi Srivastava
// TITLE: Full adder test bench
// Date: 10.10.23, 9:44 IST

module full_adder_tb (

);
    reg in1,in2,carry_in;
    wire sum,carry_out;

    full_from_half s(sum,carry_out,in1,in2,carry_in);

    initial begin
        $dumpfile("full_from_half.vcd");
        $dumpvars(0,full_adder_tb);
        $monitor($time, "sum=%b carry_out=%b in1=%b in2=%b
carry_in=%b",sum,carry_out,in1,in2,carry_in);
        #40 $finish;
    end
    initial begin
        in1=0;
        #20 in1=~in1;
    end
    initial begin
        in2=0;
        repeat(3)
        #10 in2=~in2;
    end
    initial begin
        carry_in=0;
        repeat(7)
        #5 carry_in=~carry_in;
    end

endmodule
```