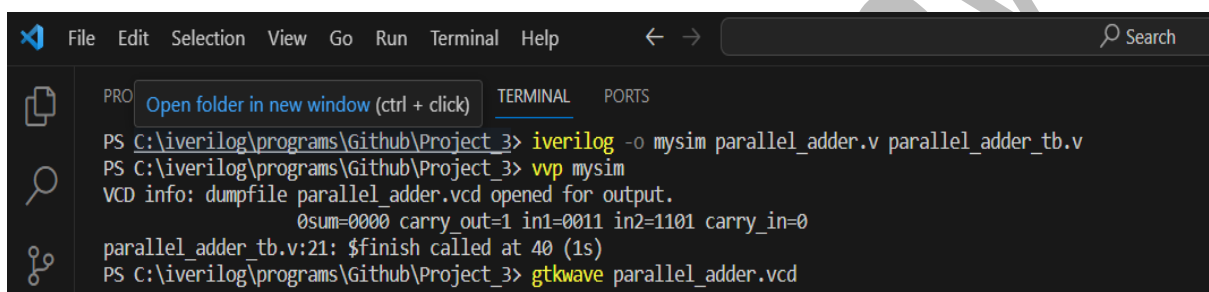


# PROJECT-5 OUTPUTS

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## 4-bit Parallel Adder



```
PS C:\iverilog\programs\Github\Project_3> iverilog -o mysim parallel_adder.v parallel_adder_tb.v
PS C:\iverilog\programs\Github\Project_3> vvp mysim
VCD info: dumpfile parallel_adder.vcd opened for output.
0sum=0000 carry_out=1 in1=0011 in2=1101 carry_in=0
parallel_adder_tb.v:21: $finish called at 40 (1s)
PS C:\iverilog\programs\Github\Project_3> gtkwave parallel_adder.vcd
```

