

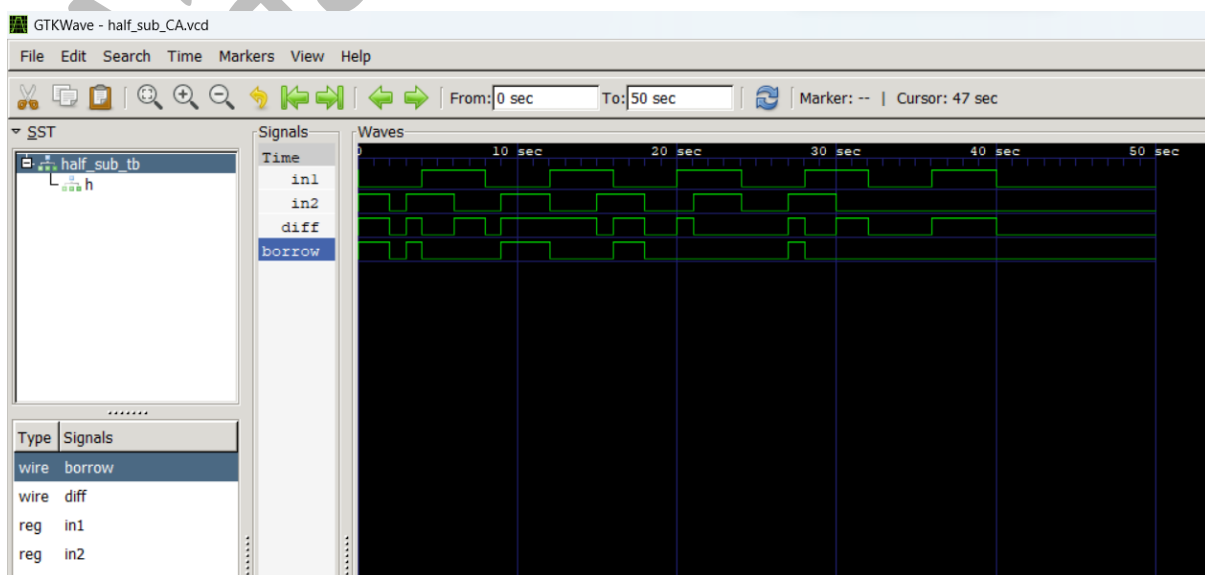
PROJECT-6 OUTPUTS

Developed by: Aashi Srivastava

National Institute of Technology, Warangal

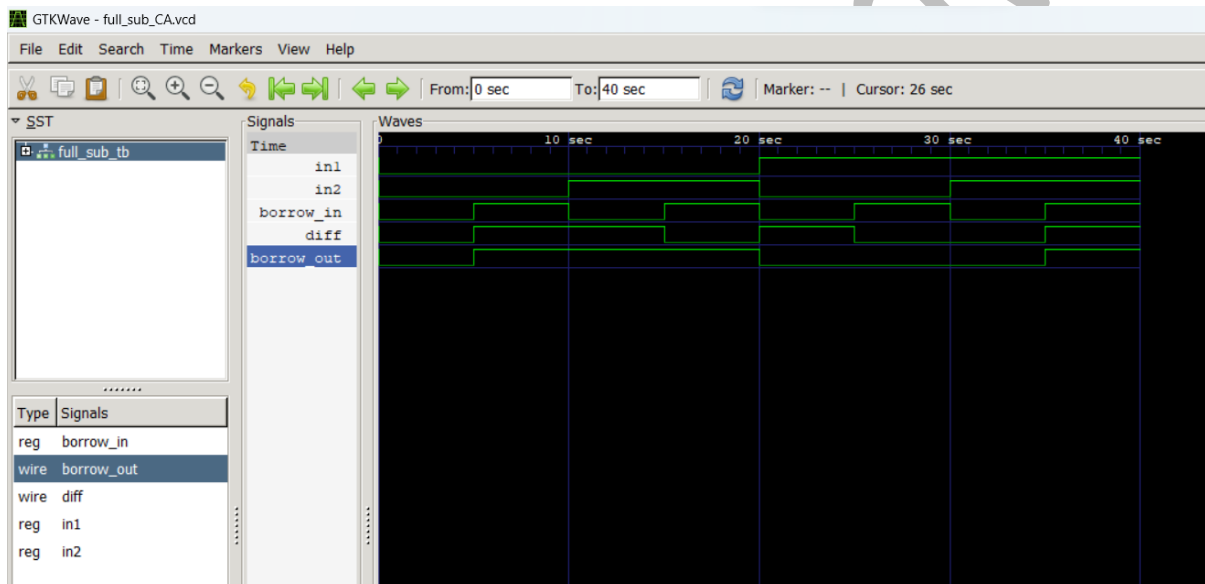
Half Subtractor:

```
PS C:\Users\AASHI SRIVASTAVA>
PS C:\Users\AASHI SRIVASTAVA> cd C:\iverilog\programs\Github\Project_6
PS C:\iverilog\programs\Github\Project_6> iverilog -o mysim half_sub_CA.v half_sub_tb.v
PS C:\iverilog\programs\Github\Project_6> vvp mysim
VCD info: dumpfile half_sub_CA.vcd opened for output.
0in1=0 in2=1 diff=1 borrow=1
2in1=0 in2=0 diff=0 borrow=0
3in1=0 in2=1 diff=1 borrow=1
4in1=1 in2=1 diff=0 borrow=0
6in1=1 in2=0 diff=1 borrow=0
8in1=0 in2=0 diff=0 borrow=0
9in1=0 in2=1 diff=1 borrow=1
12in1=1 in2=0 diff=1 borrow=0
15in1=1 in2=1 diff=0 borrow=0
16in1=0 in2=1 diff=1 borrow=1
18in1=0 in2=0 diff=0 borrow=0
20in1=1 in2=0 diff=1 borrow=0
21in1=1 in2=1 diff=0 borrow=0
24in1=0 in2=0 diff=0 borrow=0
27in1=0 in2=1 diff=1 borrow=1
28in1=1 in2=1 diff=0 borrow=0
30in1=1 in2=0 diff=1 borrow=0
32in1=0 in2=0 diff=0 borrow=0
36in1=1 in2=0 diff=1 borrow=0
40in1=0 in2=0 diff=0 borrow=0
half_sub_tb.v:27: $finish called at 50 (1s)
PS C:\iverilog\programs\Github\Project_6> gtkwave half_sub_CA.vcd
```



Full Subtractor:

```
PS C:\iverilog\programs\Github\Project_6> iverilog -o mysim full_sub_CA.v full_sub_tb.v
PS C:\iverilog\programs\Github\Project_6> vvp mysim
VCD info: dumpfile full_sub_CA.vcd opened for output.
    0diff=0 borrow_out=0 in1=0 in2=0 borrow_in=0
    5diff=1 borrow_out=1 in1=0 in2=0 borrow_in=1
   10diff=1 borrow_out=1 in1=0 in2=1 borrow_in=0
   15diff=0 borrow_out=1 in1=0 in2=1 borrow_in=1
   20diff=1 borrow_out=0 in1=1 in2=0 borrow_in=0
   25diff=0 borrow_out=0 in1=1 in2=0 borrow_in=1
   30diff=0 borrow_out=0 in1=1 in2=1 borrow_in=0
   35diff=1 borrow_out=1 in1=1 in2=1 borrow_in=1
full_sub_tb.v:18: $finish called at 40 (1s)
PS C:\iverilog\programs\Github\Project_6> gtkwave full_sub_CA.vcd
```



Parallel Subtractor:

```
File Edit Selection View Go Run Terminal Help

PROBLEMS 1 OUTPUT DEBUG CONSOLE TERMINAL PORTS

PS C:\iverilog\programs\Github\Project_6> iverilog -o mysim Parallel_sub.v Parallel_sub_tb.v
PS C:\iverilog\programs\Github\Project_6> vvp mysim
VCD info: dumpfile Parallel_sub.vcd opened for output.
          0diff=0111 borrow_out=1 in1=1010 in2=0011
Parallel_sub_tb.v:21: $finish called at 40 (1s)
PS C:\iverilog\programs\Github\Project_6> gtkwave Parallel_sub.vcd

GTKWave Analyzer v3.3.100 (w)1999-2019 BSI

[0] start time.
[40] end time.
```

