

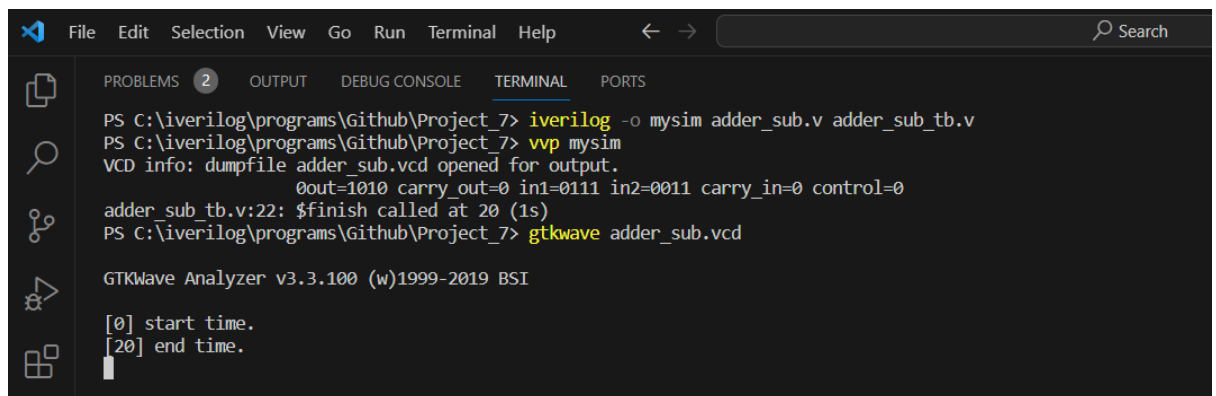
PROJECT-7 OUTPUTS

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1. Adder-Subtractor-

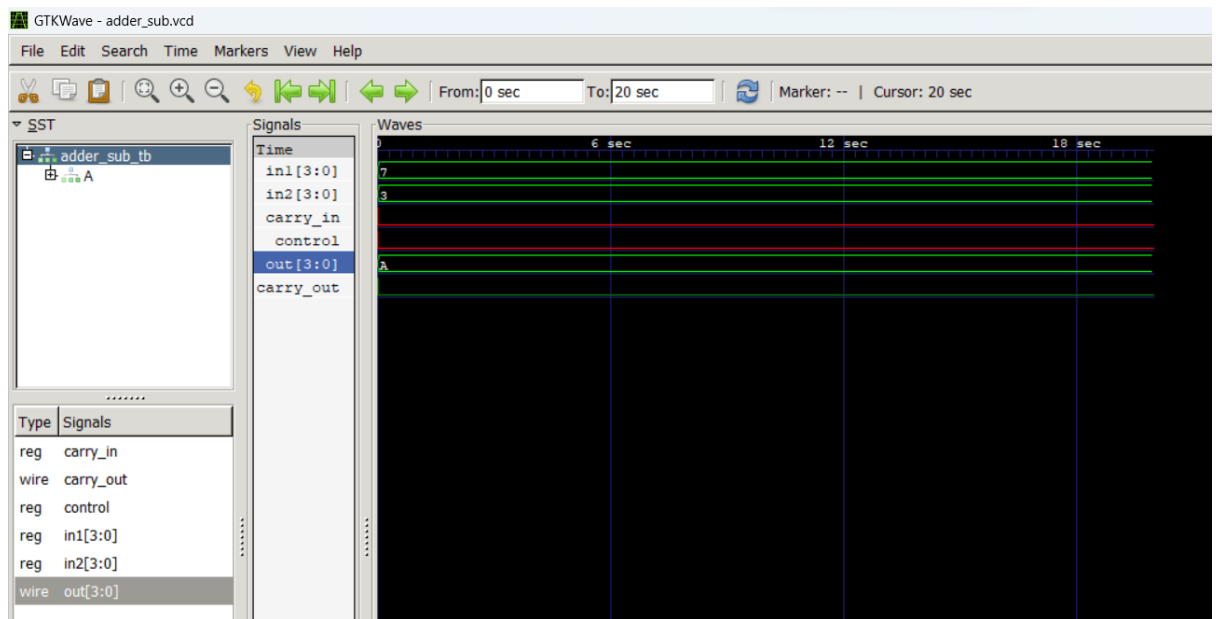
When control=0



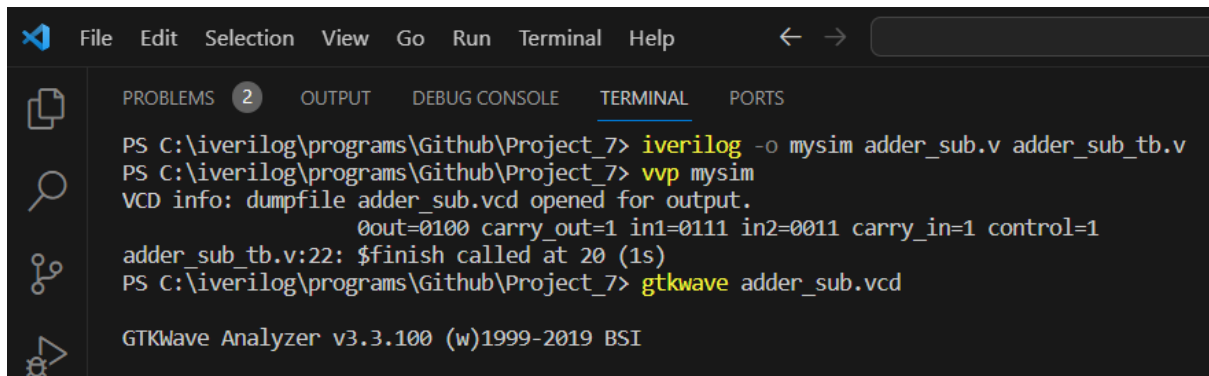
```
PS C:\iverilog\programs\Github\Project_7> iverilog -o mysim adder_sub.v adder_sub_tb.v
PS C:\iverilog\programs\Github\Project_7> vvp mysim
VCD info: dumpfile adder_sub.vcd opened for output.
          0out=1010 carry_out=0 in1=0111 in2=0011 carry_in=0 control=0
adder_sub_tb.v:22: $finish called at 20 (1s)
PS C:\iverilog\programs\Github\Project_7> gtkwave adder_sub.vcd

GTKWave Analyzer v3.3.100 (w)1999-2019 BSI

[0] start time.
[20] end time.
```



When control=1



```
PS C:\iverilog\programs\Github\Project_7> iverilog -o mysim adder_sub.v adder_sub_tb.v
PS C:\iverilog\programs\Github\Project_7> vvp mysim
VCD info: dumpfile adder_sub.vcd opened for output.
0out=0100 carry_out=1 in1=0111 in2=0011 carry_in=1 control=1
adder_sub_tb.v:22: $finish called at 20 (1s)
PS C:\iverilog\programs\Github\Project_7> gtkwave adder_sub.vcd

GTKWave Analyzer v3.3.100 (w)1999-2019 BSI
```

