PROJECT NO. – 7

AIM : To design a parallel adder and subtractor circuit .

APPARATUS : Input and output switches ; wires for connection ; full adders; XOR ,NOT Gate ; DEEDS simulator .

(COMBINED) :

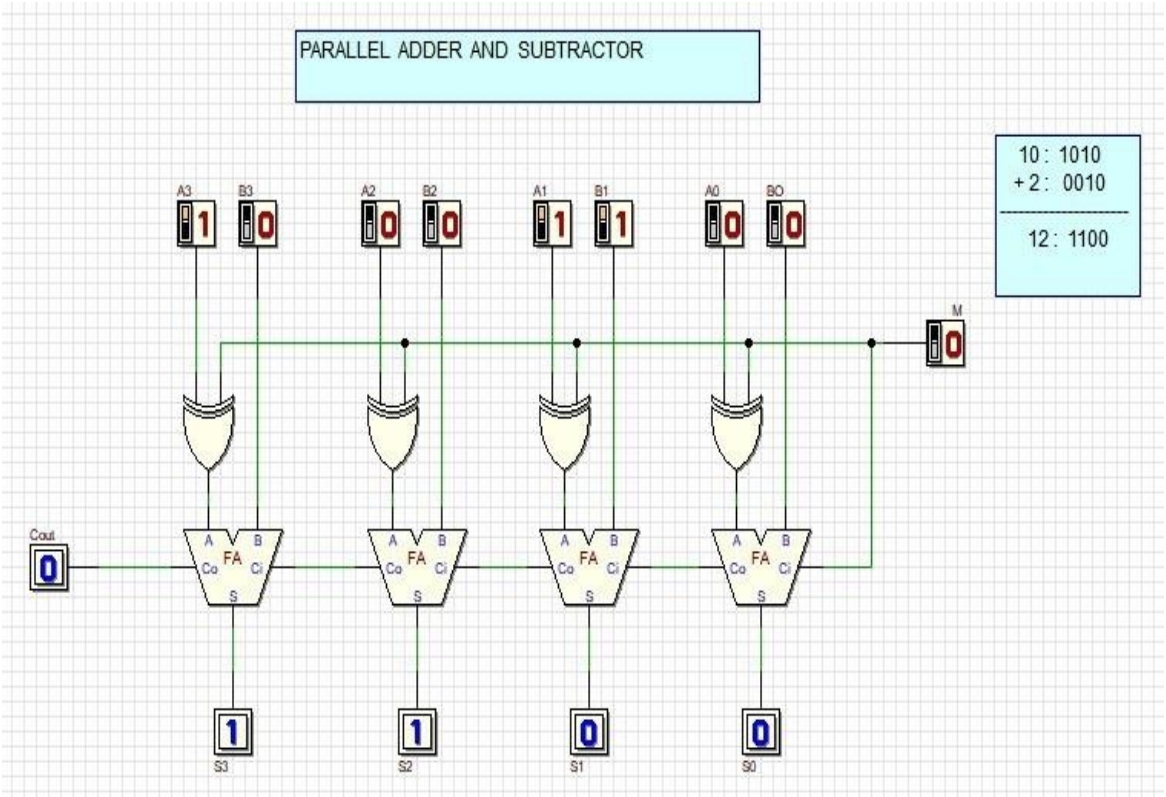
XOR gate input = A*M' + (A')*M

A : When M = 0

XOR gate input = A

So the full adder would add A and B input .

The circuit hence act as a PARALLE ADDER when M = 0



B: When M = 1

XOR gate input = A’

So the full adder would add A’ and B and a initial carry input 1 .

Taking A’ + 1 gives as the 2’s complement of A .

The circuit hence act as a PARALLE SUBTRACTOR when M = 1 .

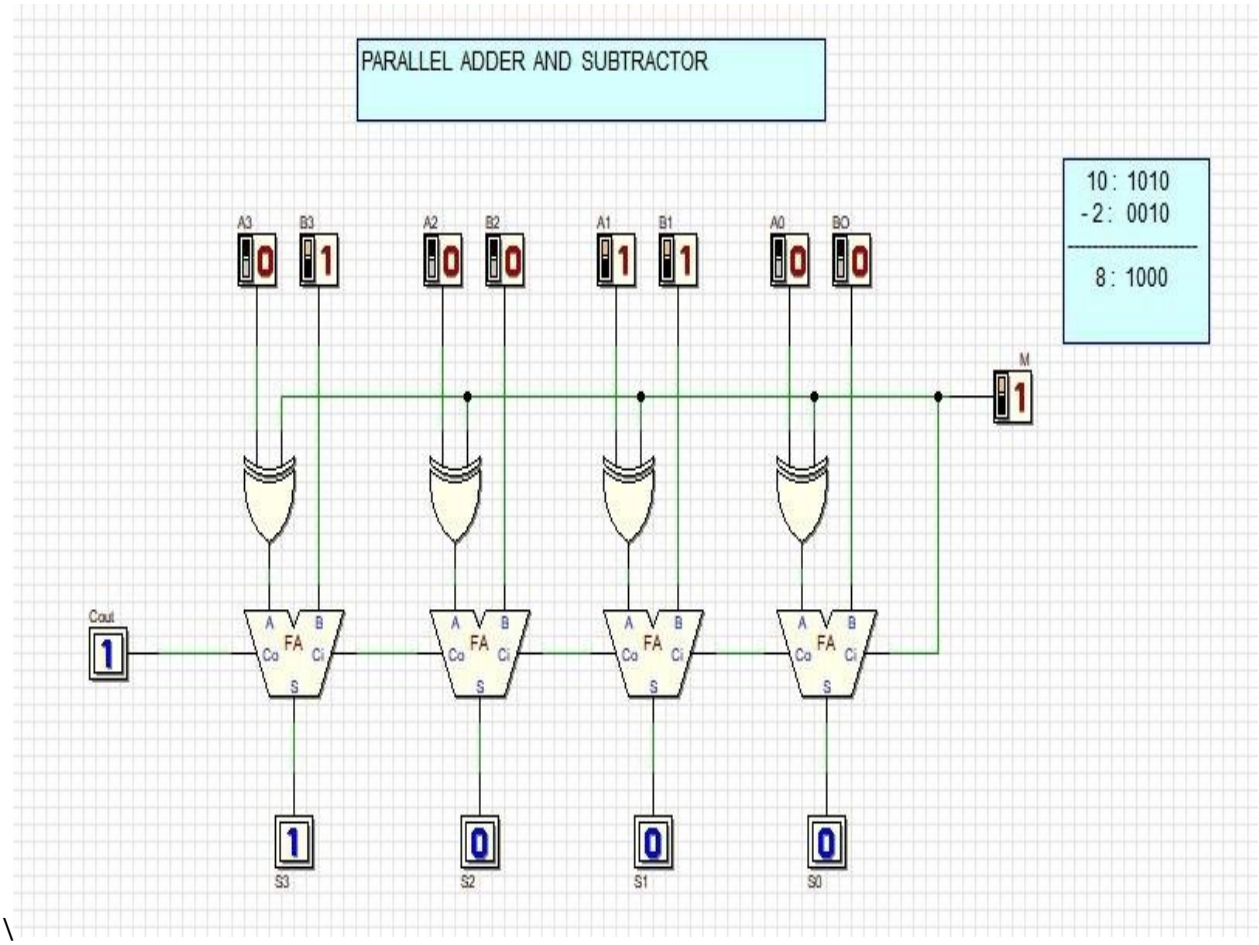
Verilog Code:

Adder-Subtractor

```
//Developed by: Aashi Srivastava
// TITLE:adder_subtractor combined
// Date: 12.10.23, 14:36 IST
module adder_sub (
    out,carry_out,in1,in2,carry_in,control
);
    input [3:0] in1,in2;

    output [3:0] out;
    input control;
    input carry_in;
    output carry_out;

    wire [3:1] wire1;

    adder_sub1 a1(out[0], wire1[1],in1[0],in2[0],carry_in,control);

    adder_sub1 a2(out[1], wire1[2],in1[1],in2[1],wire1[1],control);

    adder_sub1 a3(out[2], wire1[3],in1[2],in2[2],wire1[2],control);

    adder_sub1 a4(out[3], carry_out,in1[3],in2[3],wire1[3],control);

endmodule

module   adder_sub1 (out, carry_out,in1,in2, carry_in ,control);
    input in1,in2;
    output out,carry_out;
    input control, carry_in ;
    wire wire1;

    xor n1(wire1,in2,control);
    assign out=in1^wire1^carry_in;
    assign carry_out= (in1 & wire1) | (wire1 & carry_in) |(carry_in & in1);

endmodule
```

Test-Bench:

```
//Developed by: Aashi Srivastava
// TITLE:adder_subtractor combined test bench
// Date: 12.10.23, 14:36 IST
module adder_sub_tb (

);
    reg [3:0] in1,in2;

    wire [3:0] out;
    reg control;
    reg carry_in;
    wire carry_out;

    adder_sub A(out,carry_out,in1,in2,carry_in,control);

    initial begin
        $dumpfile ("adder_sub.vcd");
        $dumpvars(0,adder_sub_tb);
         $monitor($time, "out=%b carry_out=%b in1=%b in2=%b carry_in=%b
control=%b",out,carry_out,in1,in2, carry_in, control);
         carry_in= 1'b1; control=1'b1;
         in1=4'b0111; in2=4'b0011;
        #20 $finish;

    end

endmodule
```


PARALLEL ADDER AND SUBTRACTOR
10 : 1010
-2 : 0010
8 : 1000
A3
B3
A2
B2
A1
B1
A0
BO
M
Cout
FA
Co
Ci
S
S3
S2
S1
S0

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