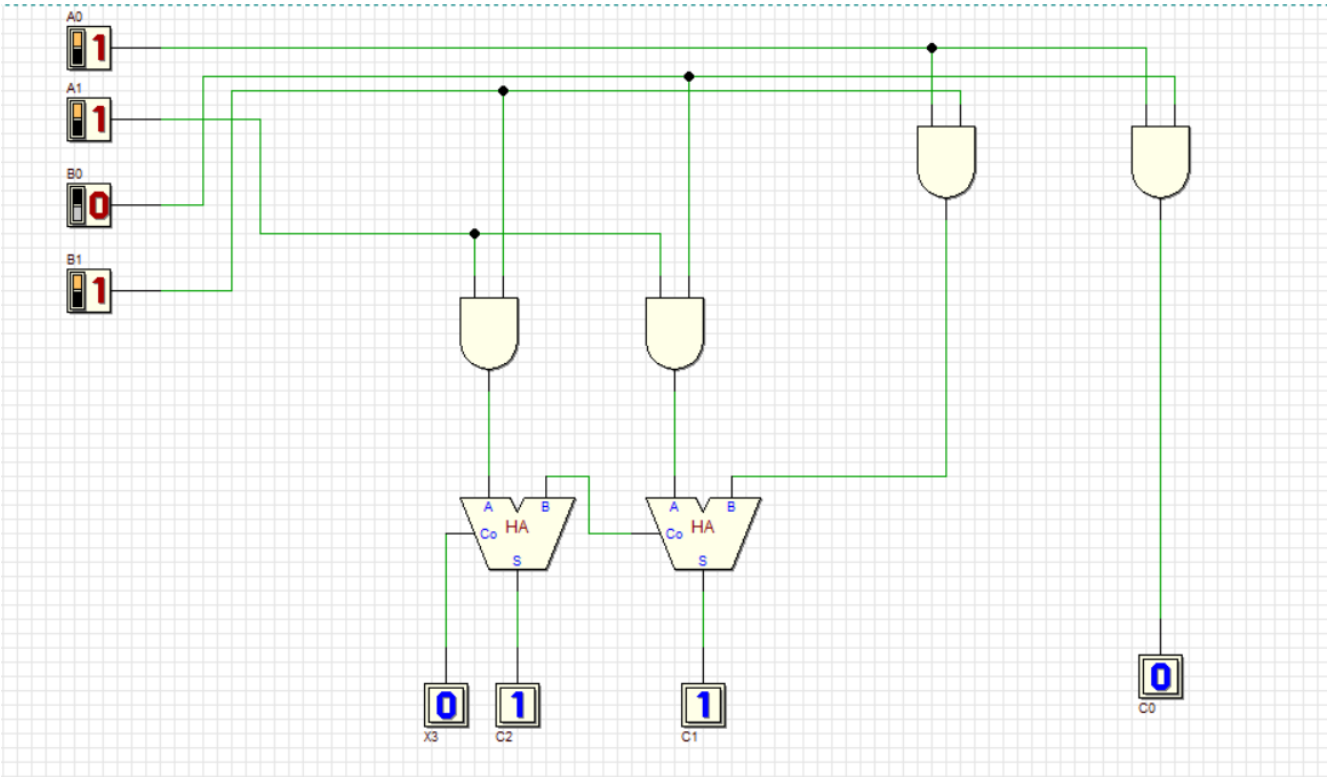
PROJECT NO. – 8(a)

AIM : To design a 2-bit Multiplier circuit.

APPARATUS : Input and output switches ; wires for connection ; full adders; XOR ,NOT Gate ; DEEDS simulator.



Verilog Code:

2-bit Multiplier

```
//Developed by: Aashi Srivastava
// TITLE:2-bit multiplier
// Date: 15.10.23, 09.53 IST
module multiplier_2bit (in1,in2,p);
input [1:0] in1,in2; //2-bit inputs
output [3:0] p ; //p here is the product
wire wire1,wire2,wire3,wire4;

and a1 (p[0], in1[0], in2[0]);
and a2 (wire1, in1[1],in2[0]);
and a3(wire2, in1[0], in2[1]);
and a4(wire3, in1[1], in2[1]);
half_adder h1 (p[1], wire4,wire1,wire2);
half_adder h2(p[2],p[3],wire3,wire4);
endmodule

module half_adder (
    sum,carry,in1,in2
);
    input in1,in2;
    output sum,carry;
    assign sum= in1^in2;
    assign carry = in1&in2;
endmodule
```

Test-Bench:

```
//Developed by: Aashi Srivastava
// TITLE:2-bit multiplier test bench
// Date: 15.10.23, 09.53 IST
module multiplier_2bit_tb (

);
    reg [1:0] in1,in2;
    wire [3:0] p;

    multiplier_2bit p1(in1,in2,p);

    initial begin
        $dumpfile("multiplier_2bit.vcd");
        $dumpvars(0,multiplier_2bit_tb);
        $monitor($time, "in1=%b in2=%b p=%b", in1,in2,p);
        in1=2'b11; in2=2'b10;
        #50 $finish();
    end

endmodule
```

OUTPUT:

```
[0] start time.
PS C:\iverilog\programs\Github\Project_8> iverilog -o mysim multiplier_2bit.v multiplier_2bit_tb.v
PS C:\iverilog\programs\Github\Project_8> vvp mysim
VCD info: dumpfile multiplier_2bit.vcd opened for output.
                  0in1=11 in2=10 p=0110
multiplier_2bit_tb.v:14: $finish called at 50 (1s)
PS C:\iverilog\programs\Github\Project_8> gtkwave multiplier_2bit.vcd

GTKWave Analyzer v3.3.100 (w)1999-2019 BSI

[0] start time.
[50] end time.
```