PROJECT-9 OUTPUTS

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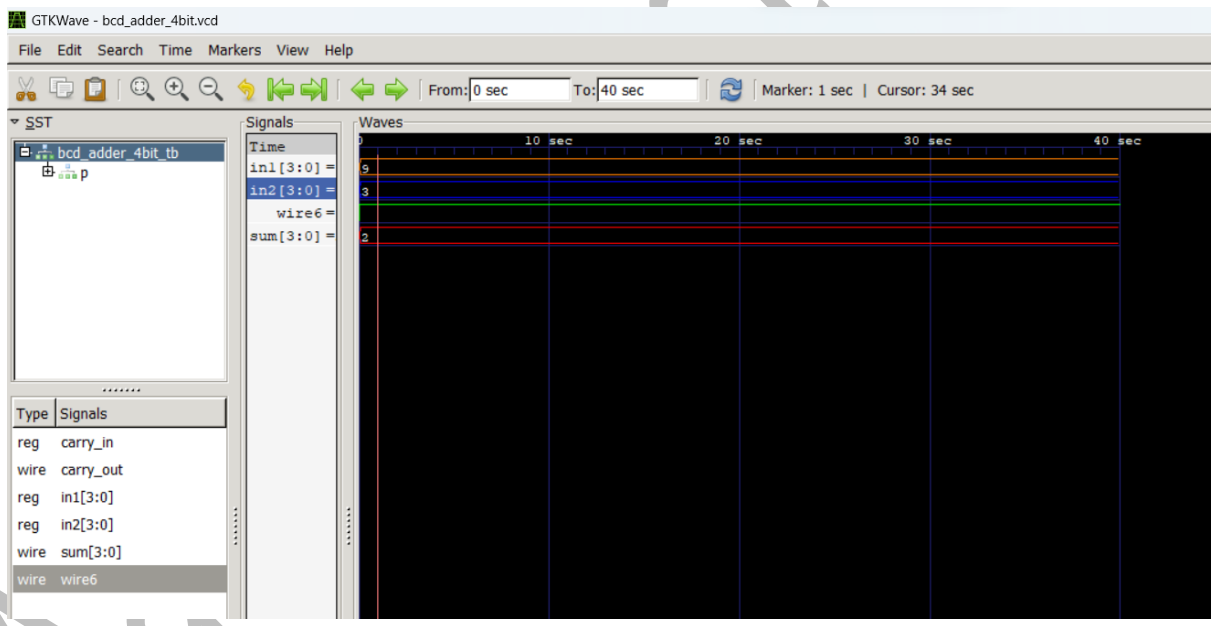
1. 4 bit, BCD Adder

```
PS C:\iverilog\programs\Github\Project_9> iverilog -o mysim bcd_adder_4bit.v bcd_adder_4bit_tb.v
PS C:\iverilog\programs\Github\Project_9> vvp mysim
VCD info: dumpfile bcd_adder_4bit.vcd opened for output.
 sum=12 in1=9 in2=3
bcd_adder_4bit_tb.v:18: $finish called at 40 (1s)
PS C:\iverilog\programs\Github\Project_9> gtkwave bcd_adder_4bit.vcd

GTKWave Analyzer v3.3.100 (w)1999-2019 BSI
```



2. 8 bit, BCD Adder

```
PS C:\iverilog\programs\Github\Project_9> iverilog -o mysim bcd_adder_8bit.v bcd_adder_8bit_tb.v
PS C:\iverilog\programs\Github\Project_9> vvp mysim
VCD info: dumpfile bcd_adder_8bit.vcd opened for output.
 sum=198 in1=99 in2=99
bcd_adder_8bit_tb.v:23: $finish called at 40 (1s)
PS C:\iverilog\programs\Github\Project_9> gtkwave bcd_adder_8bit.vcd
```