UART 16550 Transmitter (TX) Logic

1. Baud Rate Generation with 16-Bit Oversampling

The UART 16550 TX logic incorporates a baud rate generator that produces clock pulses to achieve the desired data transmission rate. The introduction of 16-bit oversampling is a technique where 16 samples are taken per bit period, significantly improving the accuracy of baud rate detection. This oversampling method helps in better identifying the transitions between bits and enhances the robustness of the communication link.

2. Data Formatting

Data formatting in the transmitter logic involves the configuration of start bits, data bits (typically 8 bits, but can be configured using the LCR), optional parity bits, and stop bits. The Line Control Register (LCR) is a key component in this process, providing a set of control bits to configure the data format. The LCR allows users to specify the word length, select the number of stop bits, and enable or disable parity.

3. Transmit Data Buffer

The transmit data buffer serves as a temporary storage location for the data to be transmitted. The TX logic efficiently manages the transfer of data from this buffer to the serial output line. The buffer is essential for handling varying data rates and ensuring smooth communication.

4. Flow Control

To prevent data overrun issues, the UART 16550 TX logic may implement flow control mechanisms. Flow control ensures that the transmitter does not send data at a rate faster than the receiver can handle. This prevents data loss and ensures reliable communication in scenarios where the receiver might be temporarily unable to process incoming data.

Bit Assignments in Line Control Register (LCR)

In a typical UART configuration, the Line Control Register consists of multiple bits that control various aspects of the communication format. The exact bit assignments may vary slightly depending on the UART model or manufacturer. Here is a common set of bit assignments:

Word Length (Bits 1 and 0):

00: 5 bits

01: 6 bits

10: 7 bits

11: 8 bits

Word length determines the number of data bits in each frame. It is essential for both the transmitter and receiver to agree on the word length for successful communication.

Number of Stop Bits (Bit 2):

0: 1 stop bit

1: 1.5 or 2 stop bits (depending on the configuration)

Stop bits indicate the end of a data frame. The number of stop bits can be set to 1, 1.5, or 2, depending on the desired configuration.

Parity Enable (Bit 3):

0: No parity

1: Parity bit is enabled

Parity is an error-checking mechanism. If enabled, an additional bit (parity bit) is transmitted after the data bits to make the total number of bits even or odd, based on the selected parity mode.

Even/Odd Parity (Bit 4):

0: Odd parity

1: Even parity (if Parity Enable is set)

This bit determines whether the parity bit should make the total number of set bits (including the parity bit) odd or even.

Stick Parity (Bit 5):

0: Stick parity is disabled

1: Stick parity is enabled

Stick parity is a mechanism where the parity bit is forced to be a specific value (1 or 0). This is useful in certain applications for creating a fixed parity condition.

Break Control (Bit 6):

0: Normal operation

1: Forces a break condition (continuous low level on the line)

The break control bit is used to transmit a continuous low-level condition on the communication line, indicating the start of a new transmission.

Divisor Latch Access (Bit 7):

0: Divisor latch is not accessed

1: Divisor latch is accessed

The Divisor Latch Access bit is used to access the divisor latch register for setting the baud rate.

UART 16550 Receiver (RX) Logic

1. Baud Rate Detection with 16-Bit Oversampling

Similar to the TX logic, the RX logic employs a baud rate detector with 16-bit oversampling to synchronize with the incoming data stream. The use of 16 samples per bit improves the accuracy of detecting bit transitions, enhancing the ability to receive data reliably at different baud rates.

2. Data Reception

The RX logic receives framed data, including start bits, data bits, optional parity bits, and stop bits. The Line Control Register (LCR) plays a crucial role in configuring the data format on the receiver side. It ensures that the receiver is set up to interpret incoming data correctly based on the configuration specified by the transmitter.

3. Parity Checking

If configured, the UART 16550 RX logic performs parity checking on received data. The LCR is used to set the desired parity option (even, odd, or none). Parity checking helps detect errors introduced during data transmission, providing a mechanism for ensuring data integrity.

4. Error Handling

The RX logic includes error detection and handling mechanisms, such as framing errors, parity errors, and buffer overrun conditions. Proper error handling is crucial for identifying and addressing issues that may occur during data reception. Error flags can be monitored, and appropriate actions can be taken to maintain reliable communication.

5. Interrupts

The UART 16550 RX logic supports interrupts to notify the system when data is available in the receive buffer or when specific events, such as errors, occur during data reception. Interrupts provide a mechanism for the system to respond promptly to incoming data or error conditions, enhancing the overall efficiency of the communication system.

Conclusion

The inclusion of 16-bit oversampling and the Line Control Register (LCR) in the UART 16550 TX and RX logic adds significant value to the overall functionality of the communication interface. These features contribute to accurate and reliable data transmission, making the UART 16550 suitable for a wide range of embedded systems and applications. The ability to configure data format settings and leverage oversampling techniques enhances the versatility and compatibility of the UART 16550 in diverse communication scenarios. Understanding and utilizing these features is essential for optimizing the performance of UART communication in embedded systems.