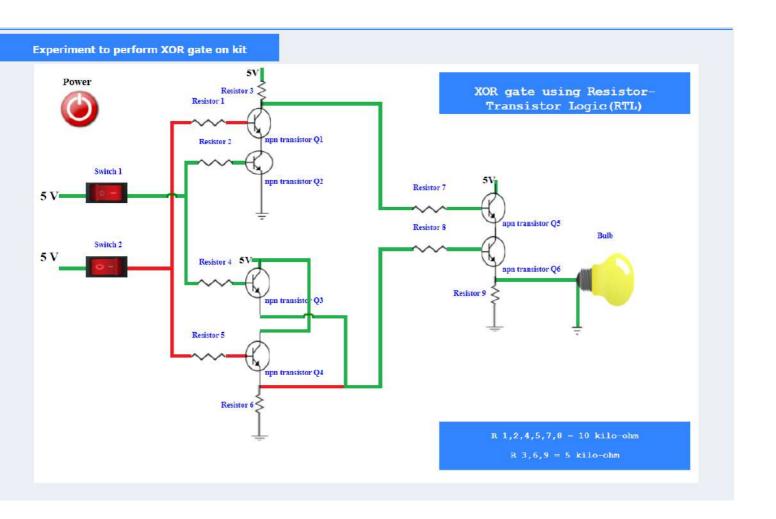


Name: Aashish Kumar

Roll 44 **No:**



Resistor 3 Resistor 1 Switch 2 Resistor 2 Input transistor Q1 Input transistor Q1 Input transistor Q2 Input

NAND gate using Resistor Transistor Logic (RTL) Switch 1 Resistor 3 H Connected!!

Experiment to perform NAND gate on kit

Switch 3

npn transistor Q1

npn transistor Q2

Resistor 2

Transistor as a NOT gate Switch 1 Resistor 1

Battery

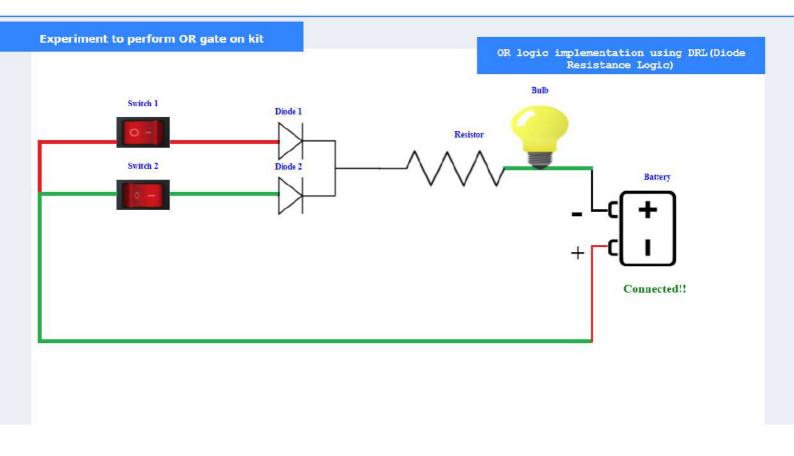
Connected!!

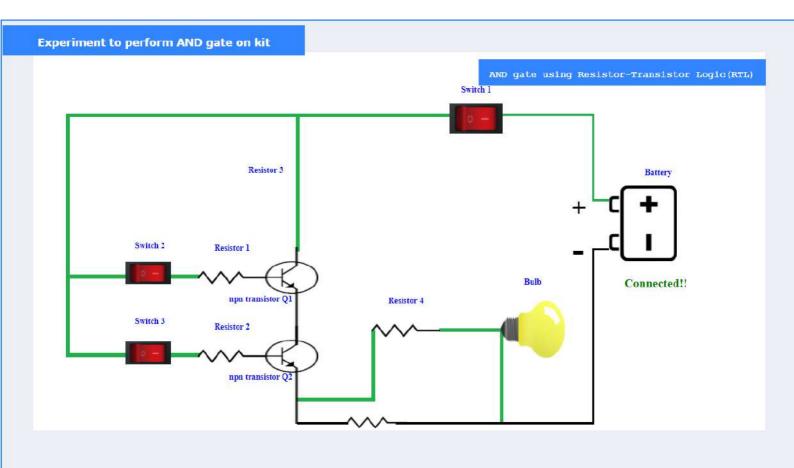
Experiment to perform NOT gate on kit

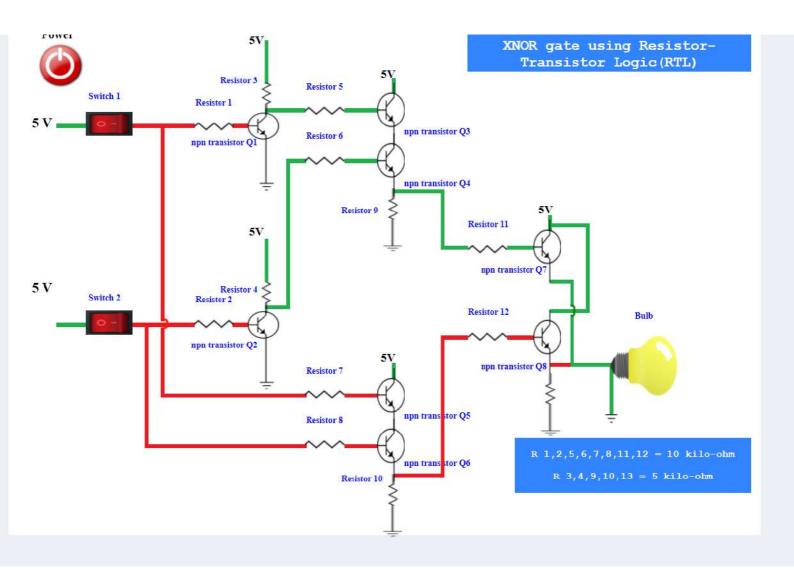
Resistor 2

npn transistor

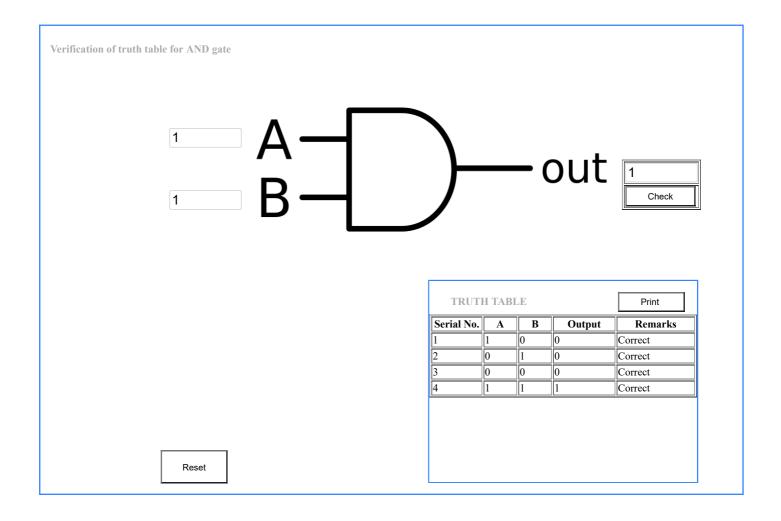
Switch 2



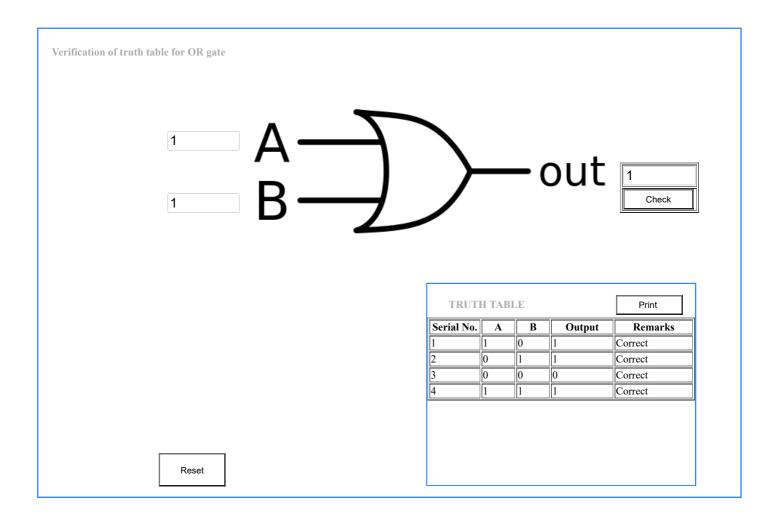




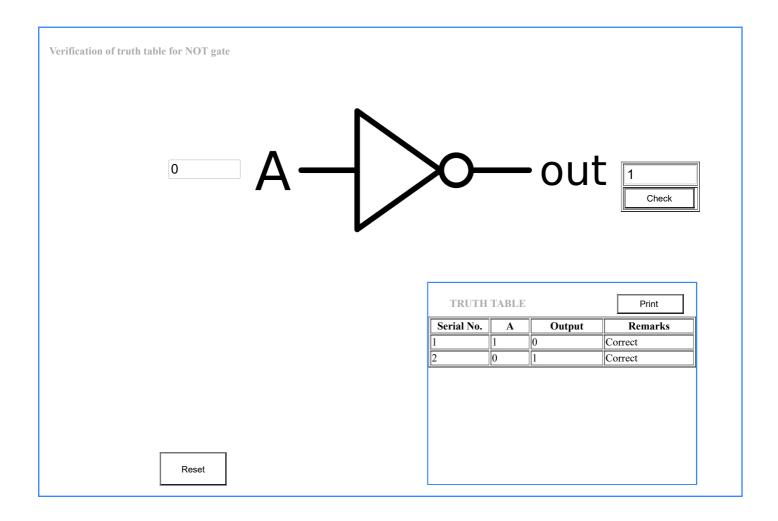
9/20/21, 3:01 PM AND Gate



9/20/21, 3:02 PM **OR Gate**

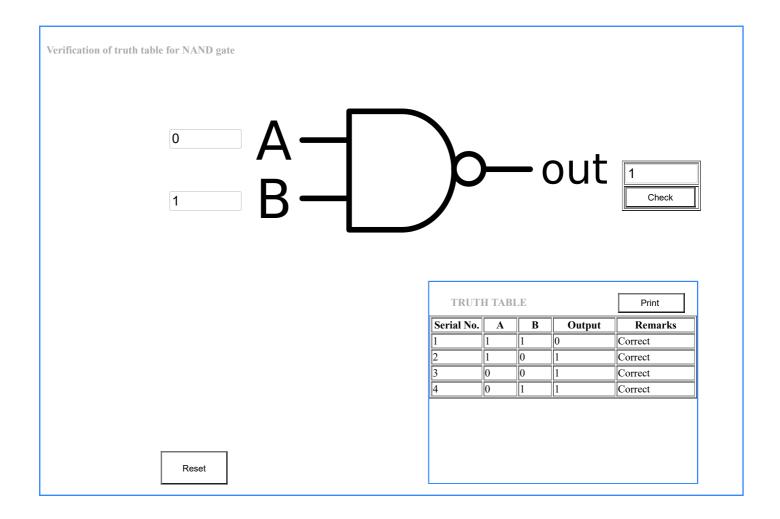


9/20/21, 3:02 PM **NOT Gate**

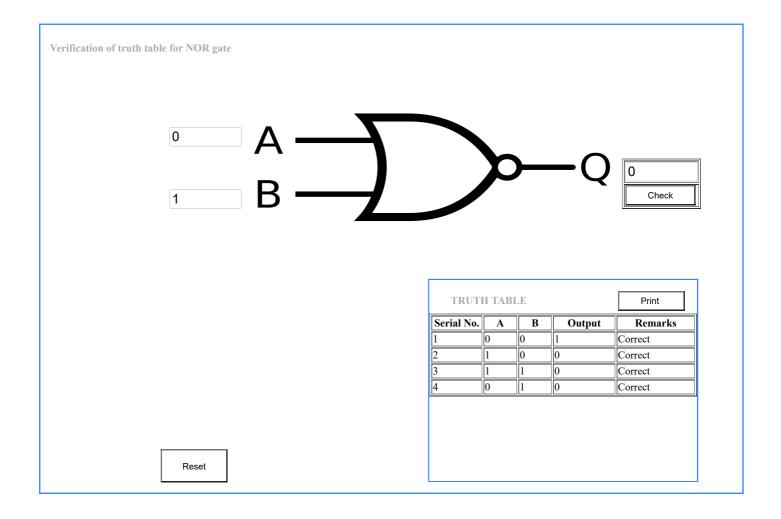


9/20/21, 3:04 PM NAND Gate

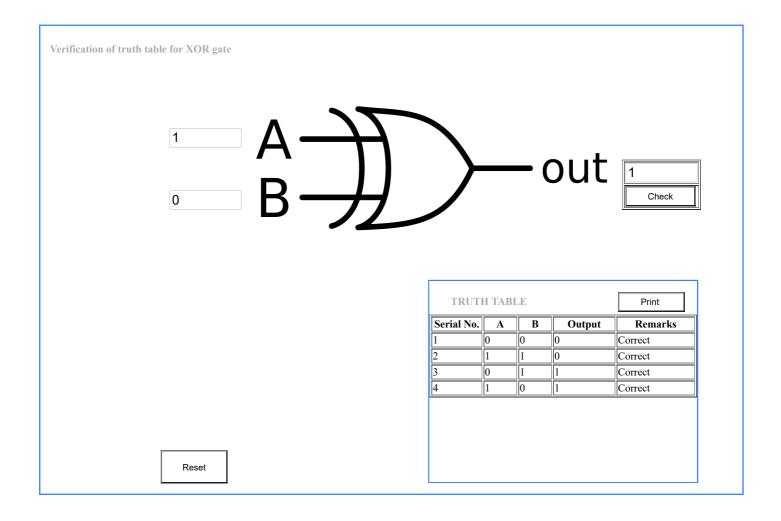
Instructions



9/20/21, 3:05 PM NOR Gate



9/20/21, 3:06 PM XOR Gate



9/20/21, 3:10 PM **XNOR Gate**

