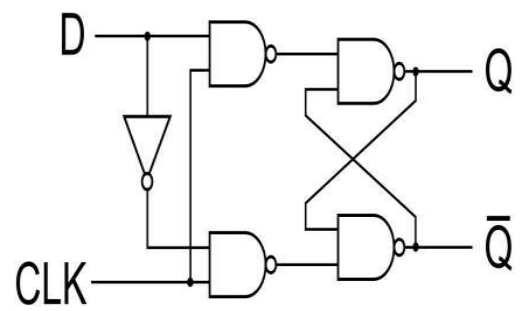
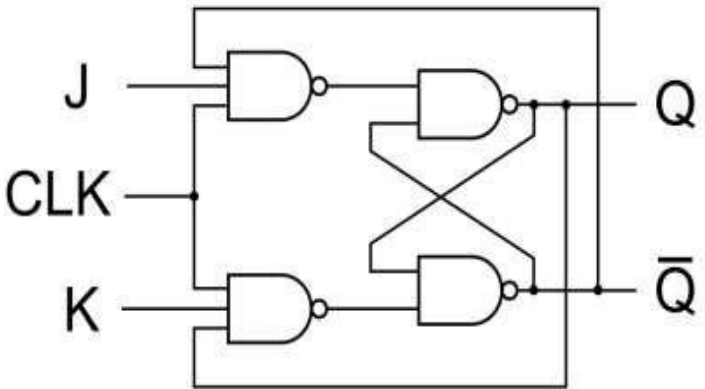
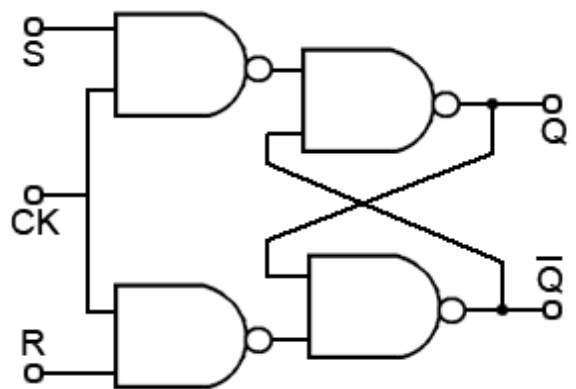


Flip-Flop Conversion

Steps To Convert from One Flip Flop to Other :

1. Draw the **Truth Table** of required flip flop.
2. Write the corresponding outputs of sub-flip flop to be used from the **Excitation Table**.
3. Draw the **Conversion table**.
4. Draw **K-Maps** using required flip flop inputs and obtain excitation functions for sub-flip flop inputs.
5. Construct logic diagram according to the functions obtained.

Truth Table (Characteristics Table)



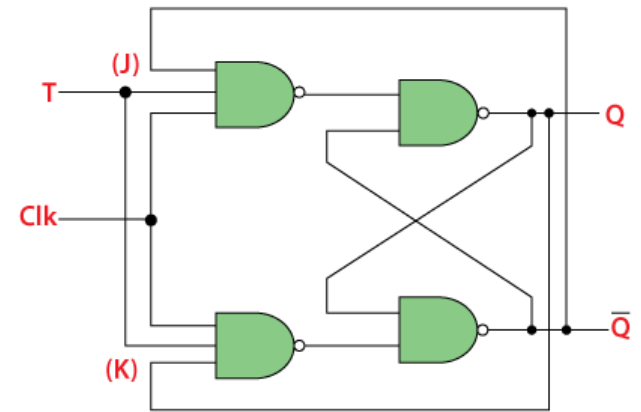
Q	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

TRUTH TABLE

S	R	Q_N	Q_{N+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	-
1	1	1	-

TRUTH TABLE

J	K	Q_N	Q_{N+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Excitation Table:

- During design of sequential circuits,
Required transition from present state to next state and to find Flip Flop input conditions that will cause the required transition.
- For this reason we need a table , Such a table is called a **flip-flop excitation table**.

Excitation Table

Q_N	Q_{N+1}	S	R	J	K	D	T
0	0	0	X	0	X	0	0
0	1	1	0	1	X	1	1
1	0	0	1	X	1	0	1
1	1	X	0	X	0	1	0

Conversion of SR Flip Flop to JK Flip Flop

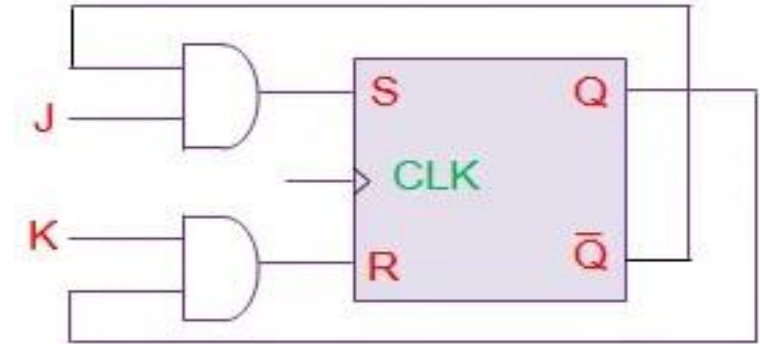
1. Truth Table for JK flip-flop

Inputs		Outputs	
J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

2. Excitation Table for SR flip-flop

Outputs		Inputs	
Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

5. Circuit Design



3. Conversion Table

J	K	Q_n	Q_{n+1}	S	R
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	X	0
1	1	0	1	1	0
1	1	1	0	0	1

4. K-map Simplification

J \ KQ_n	00	01	11	10
0	0 ⁰	X ¹	0 ³	0 ²
1	1 ⁴	X ⁵	0 ⁷	1 ⁶

$$S = J\bar{Q}_n$$

J \ KQ_n	00	01	11	10
0	X ⁰	0 ¹	1 ³	X ²
1	0 ⁴	0 ⁵	1 ⁷	0 ⁶

$$R = KQ_n$$

Q. Conversion of D Flip Flop to SR Flip Flop

1. Truth Table for SR flip-flop

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	invalid	
1	1	invalid	

2. Excitation Table for D flip-flop

Outputs		Input
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

3. Conversion Table

S	R	Q_n	Q_{n+1}	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	invalid		X
1	1	invalid		X

4. K-map Simplification

S \ RQ_n				
	00	01	11	10
0	0 ⁰	1 ¹	0 ³	0 ²
1	1 ⁴	1 ⁵	X ⁷	X ⁶

$$D = S + \bar{R}Q_n$$

5. Circuit Design

