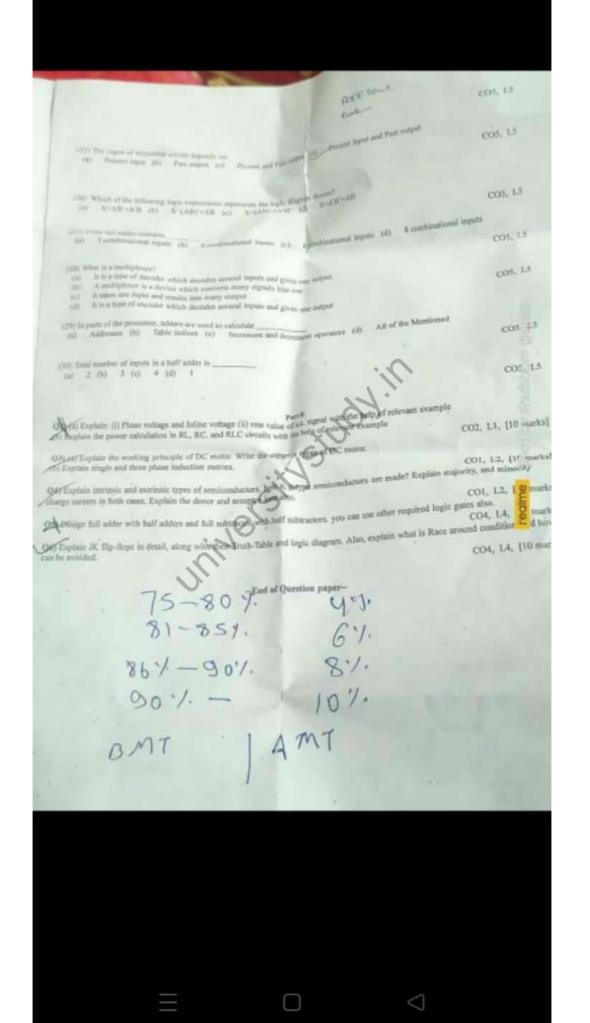
and the state of t
common base BIT to at (a) 1 to
(10) The topos revisioner of common base Off is of the Order 1 and (2) (10) The topos revisioner of common base Off is of the Order (2) (10) The topos revisioner of common base Off is of the Order (2) (10) The topos revisioner of common base Off is of the Order (2) (10) The topos revisioner of common base Off is of the Order (2) (10) The topos revisioner of common base Off is of the Order (2) (10) The topos revisioner of common base Off is of the Order (2) (10) The topos revisioner of common base (10) (10) The topos revisioner of common base (10) (10) The topos of the Order (10) (10) The topos of the Order (10) (10) The topos (10) The Order (10) (10) The topos (10) The Order (10) (10) The topos (10) The Order (10) The Order (10) (10) The topos (10) The Order (10
(a) 100 oten 101
sign squarery
(11) NACINITY is ideal for: (a) Law switching frequency (b) overfrom voltage applications (d) constraint applications
that I am away hing frequency govern
(c) Low voltage applications (d)
(12) Which of the Killowing does not holong to MOSPETT (12) Which of the Killowing does not holong to MOSPETT (12) Which of the Killowing does not holong to MOSPETT (12) Which of the Killowing does not holong to MOSPETT (12) Which of the Killowing does not holong to MOSPETT (12) Which of the Killowing does not holong to MOSPETT (12) Which of the Killowing does not holong to MOSPETT (12) Which of the Killowing does not holong to MOSPETT (13) Which of the Killowing does not holong to MOSPETT (14) Which of the Killowing does not holong to MOSPETT (15) Which of the Killowing does not holong to MOSPETT (16) Which of the Killowing does not holong to MOSPETT (17) Which of the Killowing does not holong to MOSPETT (18) Which does not hold the MOSPETT (18) Whi
(22) Which of the following does not former (1) Source
(12) Which of the following store (d) Sample: (a) Deale (d) Gate (c) those (d)
(d) OR (d) XOR (d) EXOR (d) OR
(4) NOR (2) NOR (4) EXOR (d) OR
50. mm
(14) Simplify A(A+B) (1+AB) (d) A
(14) Simplify A(A + D) (a) AB (b) 1 (c) (1 + AB) (d) A -
(a) An (b) 1 (c)
The same to the sa
(15) The susput will be a LOW for any case when one or more inputs are zero in a/an
(15) The sulput will be a Love Code (c) AND Gate (d) NAND Gate
(15) The sulput will be a LOW for any case when one of into a NAND Gate (a) OR Gate (b) NOT Gate (c) AND Gate (d) NAND Gate
outputs.
(16) A decoder converts a inputs to outputs.
(16) A decoder converts n impact to (d) 2*1 (d) 2*1
(17) Which of the following can be represented for decoder? (17) Which of the following can be represented for decoder? (17) Which of the following can be represented for decoder? (18) Which of the following can be represented for decoder? (18) Which of the following can be represented for decoder? (19) Which of the following can be represented for decoder?
(17) Which of the following can be represented for decoder? (a) Sequential circuit (b) Combinational circuit (c) Locial Virgini (d) None of the mentioned
(a) Saquentai circuit (b)
(18) The standard TTL gates are marketed asseries
(a) 80 (b) 82 (c) 74 (d) 08
19
A Collection series
(19) CMOS gates are commercially available as which of the following series?
(a) 1000 (b) 3000 (c) 2000 (d)
- and order order order
(20) Which logic gate has low power considerion?
(a) RIL (b) TIL (c) DO (d) CS1US
11.
(21) Latch can be called Memory Device as it has the capability of storing 24-bit
(21) Latch can be carried Membry 3. (2) Latch can be carried Membry 3. (2) storing 1-bit (b) storing 1-byte (c) storing 16-bit (d) storing 24-bit
(b) storing (-bit (c) storing storing
2221 R indicates in SR-latch.
(22) R Indicates in SR-latch. (a) Re-arrange (b) Reset (c) Recombine (d) Residue
* (a) Re-arrange (b) Resea (c)
at the STA Gin flam island
(23) The number of input sin case of D-flip flop is/are:
(a) 1 (b) 3 (c) 2 (d) 4
* - 1
(24) Identify the flip flop which can be used to make D-flip flop
The state of the s
(a) JK (b) SK (c) 1 (d) MS



	Registration No.:		
		mcre240	
Time All Cour	se Title:BASIC EL ECTION	e Code: ECELEGI CAL AND ELECTRONICS ENGI	NEERING Max l
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1. March the Paper Code sho	one carefully before attempting the	question paper. aper code mentioned on the question paper	and ensure that both
		uper code mentioned on the question	
3. Part A contains 30	kided into two parts A and B.		
4. Part B contains 5 question	Per of to	ill be deducted for each wrong answer. 4 questions out of these 5 questions. In case	ALE FORESTER
then only the tirst four after	tipled questions will be evaluated	4 questions out of these 5 questions. In case	all the 3 questions are
3. Attempt all the questions	in serial order		
7. After completion of first	90 minutes, the OMR sheet will I	Pi your regist when so, on the designated sput	ce.
R. Submit the question paper	er and the rough short(s) along w	or taken by the invigitation. ith the second about to the invigitator before t	leaving the examination.
		and activity access to one more primary occurs.	
		Park A	
Q1) -		Part-A	
A LONG and Done both a	are disabled in case of SR the flow		
(1) It set and sceed book a	are disabled in case of SR flip flop	Warn outsid its	
(a) Reset (b) Set	t (c) Previous output (d)	Preses input	
	and the same of th		
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	rister is capable of storing vie (c) 2 bit (d) 2 byte	, //	
(a) 1 bit (b) 1 b;	yte (c) 2 bit (d) 2 byte	17.	
		.03	
(3) Synchronus counter is		Minister (d) tripple counter	
(a) asynchronous co	santer (b) parallel counter (c	The same of	
	1	9	
(4) Identify the basic but	lding block of Shift registers	on D tile flee	
(a) T flip flop (b)	28 tub nob (c) 12 febru	No. del. in sub-such	
	(3)		
(5) Shift counter is also b	The state of the s	synchronus counter (d) Asynchronus co	onter
(a) Johnson country	(p) Mibole countrie. (c)	Auctional comes (e)	
	1		
(6) The zerow direction in	the Biode symbol indicates		
(a) Direction of ele	otors flow		
(h) Direction of to	le flow (Direction of conventional	eurrent)	
(c) Opposite to the	direction of hole flow		
(d) None of the above			
The state of the state of the later	formed by bonds.		
(v) Covalent (b)	Electrovalent (c) Co-ordin	nate (d) None of the above	
(a) Secrement			
	s temperature coefficien	nt of resistance.	
(a) Positive (b)	Zero (c) Negative (d)	None of the above	
IN COUNTY OF			
	the depend in case of BIT.		***
(a) Collector (b)	rily doped in case of DFT. Base (c) Emister (d)	Gute	
(a)			
- A			
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1			

 \Diamond

(11) XOR gate is also called	
(a) Inverter (b) amplifler (c) comparator (d) BCD	COS, LS
(12) The number of inputs in case of Half adder are	60, 6
(a) 1 (b) 2 (c) 1 (d) 4	FOR 15
(13) Carry is obtained in case of:	CO4, L5
(a) Subtraction (b) Addition (c) Multiplication (d) Both addition and subtraction	
20 10 10 10 10 10 10 10 10 10 10 10 10 10	CO5, 1.5
(14) The binary addition of 1 + 1 = 7 (a) Sum = 1, Carry = 1 (b) Sum = 0, Carry = 0 (c) Sum = 1, Carry = 0 (d) Sum = 0, Carry = 1	
	CO5, L5
(15) Number of AND gates required to for a 1 to 8 Mux (a) 2 (b) 6 (c) 8 (d) 10	
	ene 14
CLOS La S Communication solved lines	CO5, L5
(16) 1 to 8 Demus require select lines. (a) 2 (b) 3 (c) 4 (d) 5	
The state of the annied for the LMIN	CO5, 1.5
(17) NOT gates will be required for 4 to 1 MUX (a) 3 (b) 1 (c) 2 (d) 4	
	CO5, 1.5
(18) Identify the building blocks for Encoder. (a) OR gate (b) AND gate (c) XOR gate (d) NOR rate	
	CO5, L5
(19) Identify the type of circuit for decoder? (a) Logical circuit (b) Sequential circuit (c) Combinational circuit (d) None of the mentioned	
(3)	COS, LS
(20) TCTL stands for:	
(a) Transistor-complementary transistor fact. (b) Transistor-complemented transistor logic (c) Transistor-capacitor transistor fact. (d) Transistor-coupled transistor logic	
	C05, L5
(21) D flip-flop is also known as lip-flop. (a) transparent (b) TTL (b) Fun-transparent (d) None of these	
	CO5, L5
(22) I flip-flop is known asflip-flop. (a) Toggie (b) Transparent (c) Set-Reset flip-flop (d) None of these	
	COS, 1.5
(23) The output of JK flip-flop when J=1, K=1, and present state output=1 is	
	COS, L5
(24) The output of SR flip-flop when S=1, R=1, and present state output=1 is	CAN, 50
(a) Invalid State (b) Memory State (c) Toggle State (d) Race Around Condition	
	CO5, 1.5
(25) The race around condition is related with (a) SR flip-flop (b) JK flip-flop (c) D flip-flop (d) T flip-flop	
	COS. LE

Course Code: ECE249

Course Title: BASIC ELECTRICAL AND ELECTRONICS ENGINEERING

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Max Marks: 70

Read the following instructions carefully before attempting the question paper.

- 1. Match the Paper Code shaded on the OMR. Sheet with the Paper code mentioned on the question paper and ensure that both are the same.
- 2. This question paper is divided into two parts A and B.
- 3. Part A contains 30 questions of 1 mark each, 0.25 marks will be deducted for each wrong answer.
- 4. Part B contains 5 questions of 10 marks each. Attempt any 4 questions out of these 5 questions. In case all the 5 questions are attempted then only the first four attempted questions will be evaluated.
- 5. Attempt all the questions in serial order,
- 6. Do not write or mark anything on the question paper except your registration no. on the designated space.
- 7. After completion of first 90 minutes, the OMR sheet will be taken by the invigilator.
- 8. Submit the question paper and the rough sheet(s) along with the answer sheet to the invigilator before leaving the examination half.

Part-A	
Q1) (1) An ideal diode under reverse bias condition operates as	
	CO4, L4
and the state of the Comment have consider a commentary as	CO1, D1
(2) An ideal diode under forward bias condition operates as	
(a) closed switch (b) open switch (c) either open switch or closed switch (d) Pione of these	
10.	CO4, L4
(3) If the voltage across the p-type and n-type terminals of a diode is 5 V and 2 V respectively. This diode is operating in	
(a) reverse bias (b) forward bias (c) both in forward bias and reverse bias (d) none of these	
	CO4, L4
VX.	-
(4) Enhancement mode is present in	
(a) MOSFET (b) JFET (c) Tunnel diode (d) projunction diode	
	CO4, L4
(5) The concept of virtual ground is applicable in	
(a) BJT (b) MOSFET (c) Digde (d) Operational Amplifier	
(5) BUT (0) MODITY (4) STATE	
	CO4, L4
(6) MOSFET acts as an amplifier in	
(a) saturation region (b) stative region (c) cut-off region (d) None of these	
	CO4, 1.4
	CU4, LA
(7) BJT acts as an amplifier in (4) None of these	
(a) saturation region (b) active region (c) cut-off region (d) None of these	
	CO4, L4
(8) A XOR B is equivalent to (8) A OR B (d) None of these	
(a) A XNOR B (b) Complement of (A XNOR B) (c) A OR B (d) None of these	
	CO4, L4
(0) 1 Nov. 1 (1) 1 Nov. 1 (1) 1 Nov. 1 (1) 1 Nov. 1	
(a) A XOR B XOR C is equivalent to Complement of (A XNOR B XNOR C) (c) A.B.C (d) None of these	
(8) A XNOR B XNOR C (6) Compression	004.14
	CO4, 1.4
(10) The BJT as acts a closed switch in	
(a) linear region (b) cut-off region (c) saturation region (d) None of these	
	CO4, 1.4

(26) Thi (a) (c)	e one of the major differences between flip-flop and latch is that a flip-flip is tevel triggered, edge triggered (b) edge triggered, level triggered ievel triggered, level triggered (d) edge triggered, adga triggered	CO5, L5
(27) In. (a)	there are different clock alguals used to produce the output. (b) Synchronous counters (c) None of these	
(c)	BothAsynchronous counters and Synchronous counters (d) None of these	CO5, L5
(28) A	is a in which the output from the last flip flop is inverted and fed back a Johnson counter, modified ring counter (b) modified ring counter, Johnson counter	o an input to the first.
(a) (c)	Johnson counter, Johnson counter (d) ring counter, modified ring counter	CO5, 1.5
(29) T	The next state output of D flip-flop when input D=1 and present state output=1 is	
	1);	C05, L5
(30) 7 (2)	The next state output of T flip-flop when T=1 and present state output=1 is 1 (b) 0 (c) Invalid State (d) None of these	CO5, L5
	Part-B	
(22)	Perform steady state analysis on RLC circuits.	
alleri I	Explain the working principle of electric machines in detail.	CO2, L1, [10 marks]
		CO1, LZ, [10 marks]
	Explain Op-amps and their ideal characteristics, what do you understand by inverting and non-inverting configu	COT, Lot 110 market
Q5)	Explain Multiplexer (MUX) in detail. Show how a 32 K I MUX can be implemented using 8 X 1 and 4 X1 MU	X.
	Design a Mod-12 Asynshoronous counter with the seign of JK flip-flop. Draw its waveform and truth table also.	CO4, L4, [10 marks]
(00)	Design & stop-12 Asymmetrian country and	CO4, L4, [10 marks]
	-End of Question paper-	