Unit-6

Sequential Logic Circuits : Applications

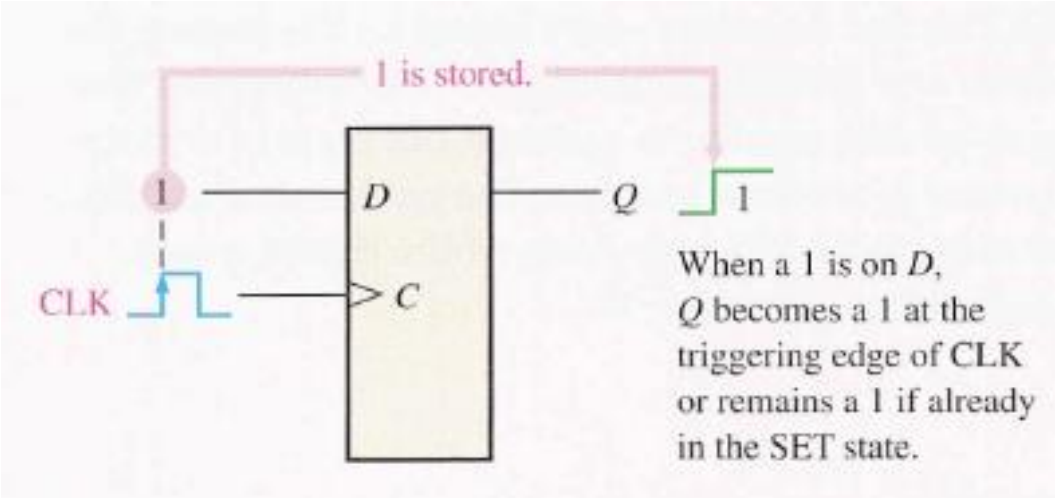
Register

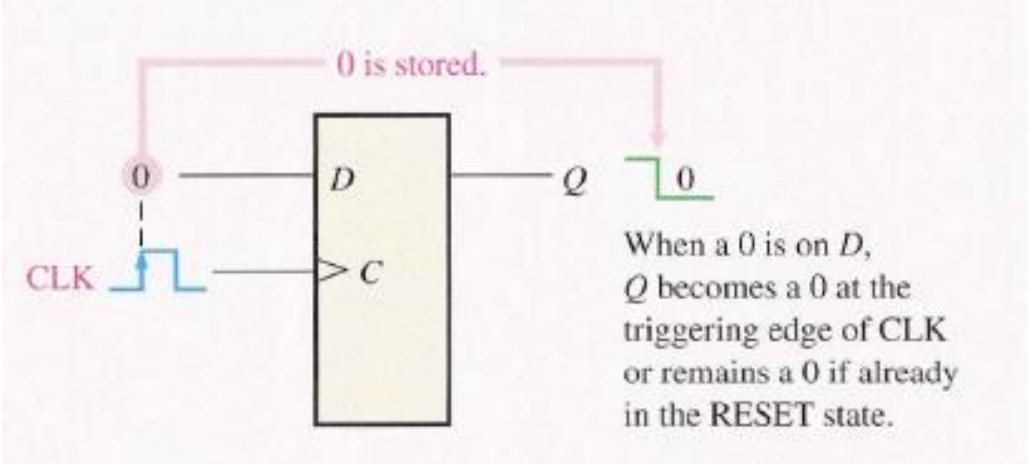
Register

Flip-flop is a 1 bit memory cell which can be used for storing the **digital** data.

To increase the storage capacity in terms of number of bits, we have to use a group of flip-flop. Such a group of flip-flop is known as a **Register**.

The **n-bit register** will consist of **n** number of flip-flop and it is capable of storing an **n-bit** word.





Two Function of register

1. Data Storage
2. Date Movement

Shift Registers

- Another function of a register, besides storage, is to provide for *data movements*.

- Each *stage* (flip-flop) in a shift register represents one bit of storage,

And, shifting capability of a register permits the movement of data from stage to stage within the register, or into or out of the register upon application of clock pulses.

Application of shift register

•Shift register is used as **Parallel to serial converter**, which converts the parallel data into serial data. It is utilized at the transmitter section after Analog to Digital Converter ADC block.

•Shift register is used as **Serial to parallel converter**, which converts the serial data into parallel data. It is utilized at the receiver section before Digital to Analog Converter DAC block.

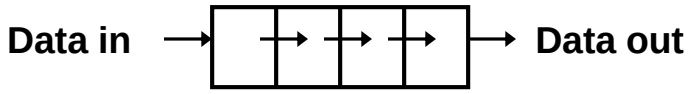
•Shift register along with some additional gates generate the sequence of zeros and ones. Hence, it is used as **sequence generator**.

•Shift registers are also used as **counters**.

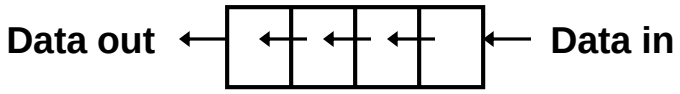
There are two types of counters based on the type of output from right most D flip-flop is connected to the serial input. Those are Ring counter and Johnson Ring counter.

Shift Registers

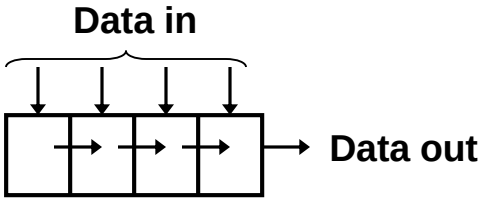
- Basic data movement in shift registers (four bits are used for illustration).



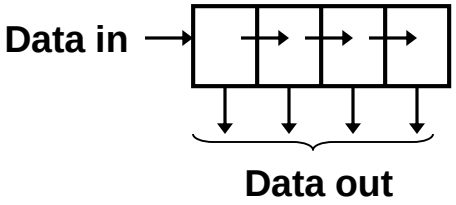
(a) Serial in/shift right/serial out



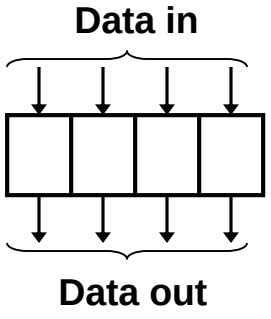
(b) Serial in/shift left/serial out



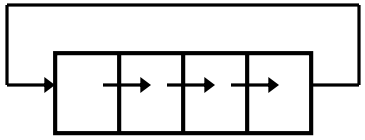
(c) Parallel in/serial out



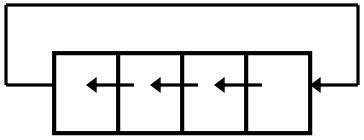
(d) Serial in/parallel out



(e) Parallel in / parallel out



(f) Rotate right



(g) Rotate left

The Shift Register

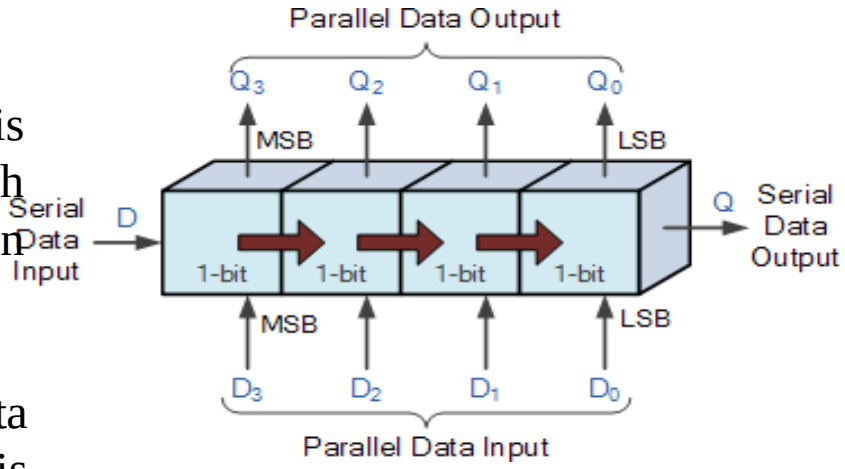
The **Shift Register** used for the storage or the transfer of binary data.

Serial-in to Serial-out (SISO) - Data is shifted serially "IN" and "OUT" of the register, one bit at a time in either a left or right direction under clock control.

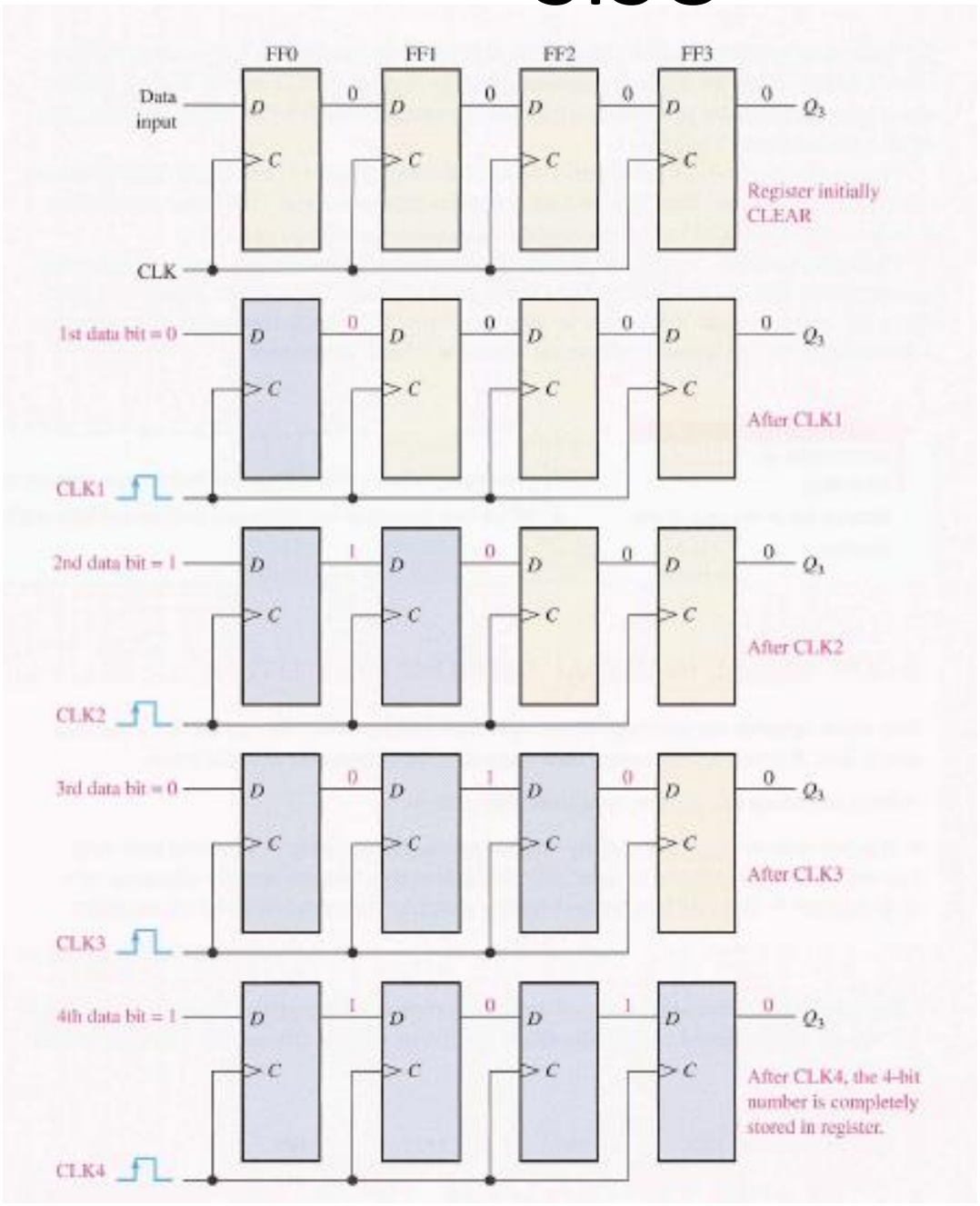
Serial-in to Parallel-out (SIPO) - Register is loaded with serial data, one bit at a time, with the stored data being available at the output in parallel form.

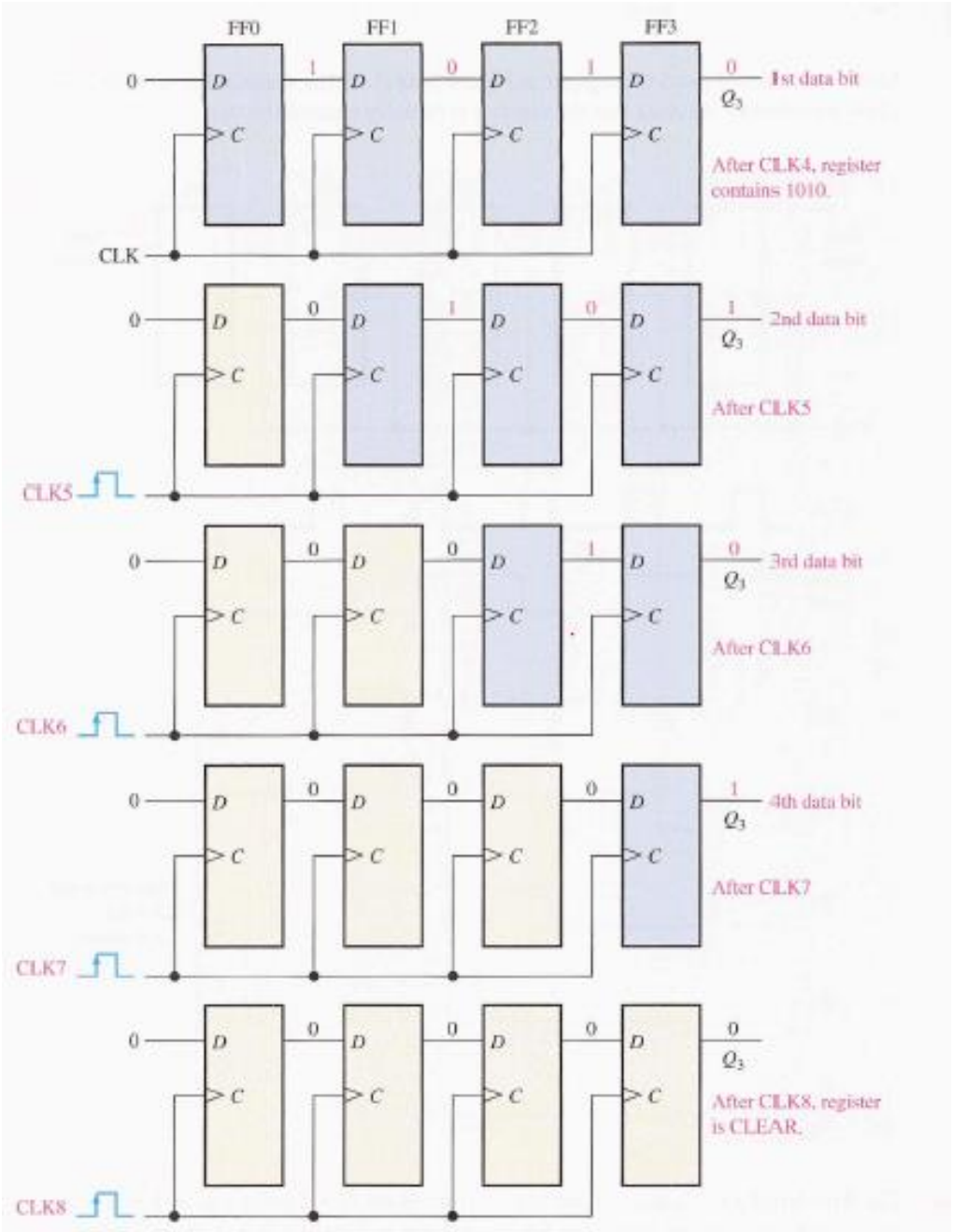
Parallel-in to Serial-out (PISO) - Parallel data is loaded into the register simultaneously and is shifted out of the register serially one bit at a time under clock control.

Parallel-in to Parallel-out (PIPO) - Parallel data is loaded simultaneously into the register, and transferred together to their respective outputs by the same clock pulse.

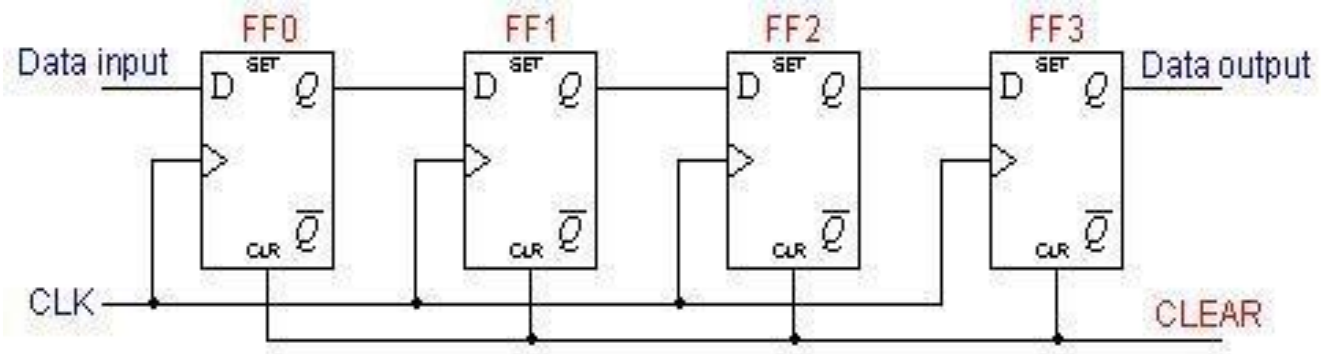


SISO


FF0
FF1
FF2
FF3
Data input
D
C
0
Q_3
Register initially CLEAR
CLK
1st data bit = 0
After CLK1
CLK1
2nd data bit = 1
1
After CLK2
CLK2
3rd data bit = 0
After CLK3
CLK3
4th data bit = 1
After CLK4, the 4-bit number is completely stored in register.
CLK4


FF0
FF1
FF2
FF3
0
1
0
1
0
1st data bit
Q_3
After CLK4, register contains 1010.
CLK
0
0
1
0
1
2nd data bit
Q_3
After CLK5
CLK5
0
0
0
1
0
3rd data bit
Q_3
After CLK6
CLK6
0
0
0
0
1
4th data bit
Q_3
After CLK7
CLK7
0
0
0
0
0
Q_3
After CLK8, register is CLEAR.
CLK8

Serial-in to Serial-out (SISO) Shift Register



All the FF are reset and a logical input 1011 is applied at the serial input line connected to stage FF0

Operation of the Shift-right Register

Timing pulse	Q_A	Q_B	Q_C	Q_D	*Serial output at* Q_D
Initial value	0	0	0	0	0
After 1st clock pulse	1	0	0	0	0
After 2nd clock pulse	1	1	0	0	0
After 3rd clock pulse	0	1	1	0	0
After 4th clock pulse	1	0	1	1	1

MCQ

The group of bits 11001 is serially shifted (right-most bit first) into a 5-bit serial output shift register with an initial state 01110. After three clock pulses, the register contains _____ .

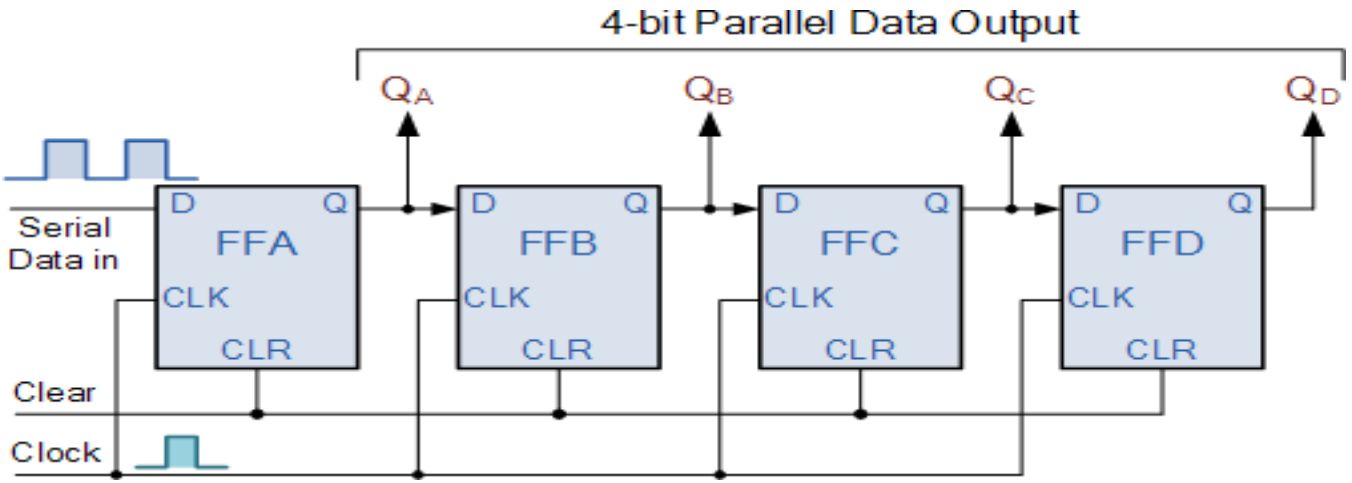
a) 01110
b) 00001
c) 00101
d) 00110

MCQ

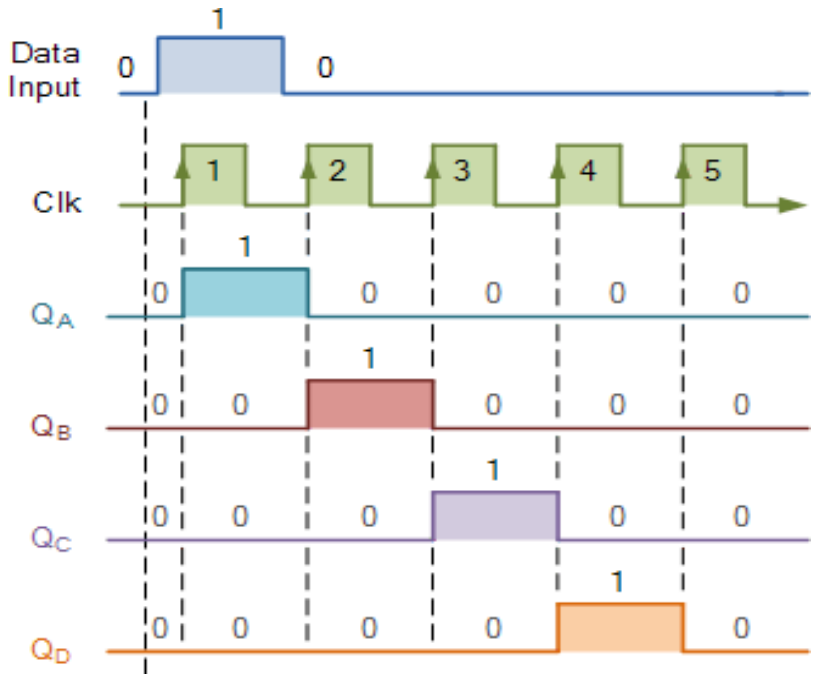
Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first)

a) 1100
b) 0011
c) 0000
d) 1111

4-bit Serial-in to Parallel-out Shift Register



Clock Pulse No	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	0	0	0	0

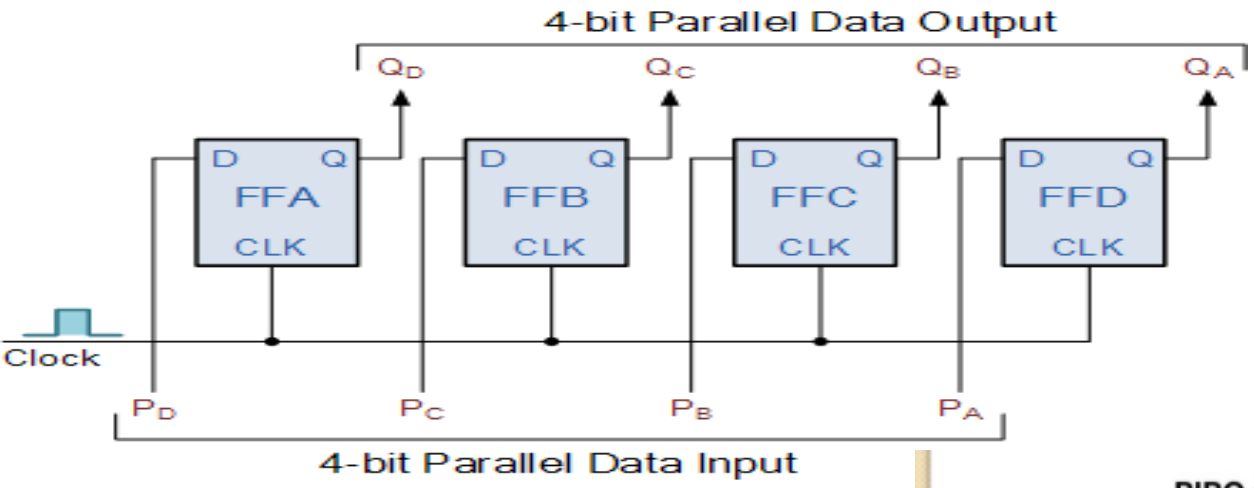


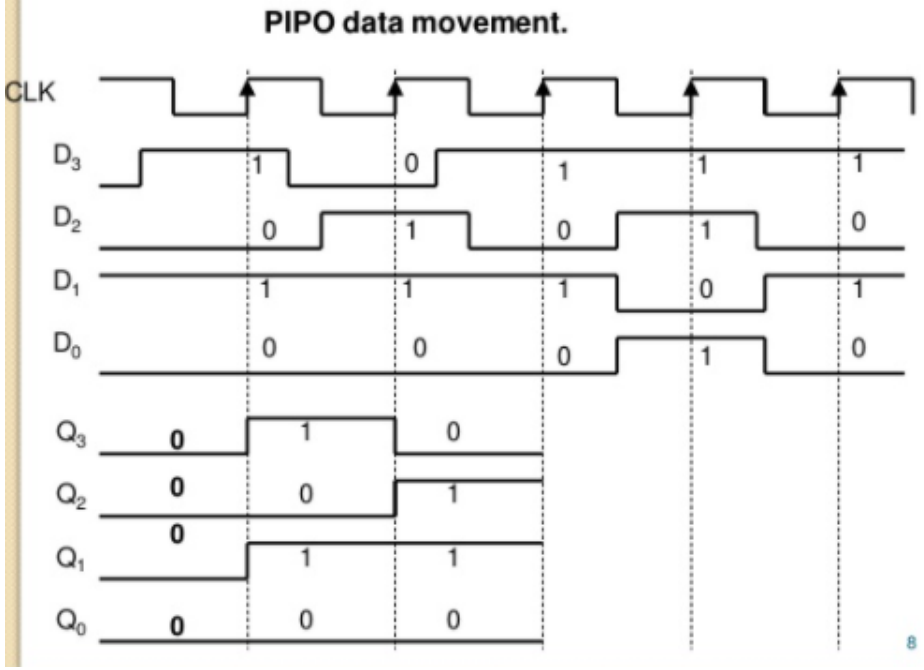
MCQ

A serial in/parallel out, 4-bit shift register initially contains all 1s. The data nibble 0111 is waiting to enter. After four clock pulses, the register contains _____ .

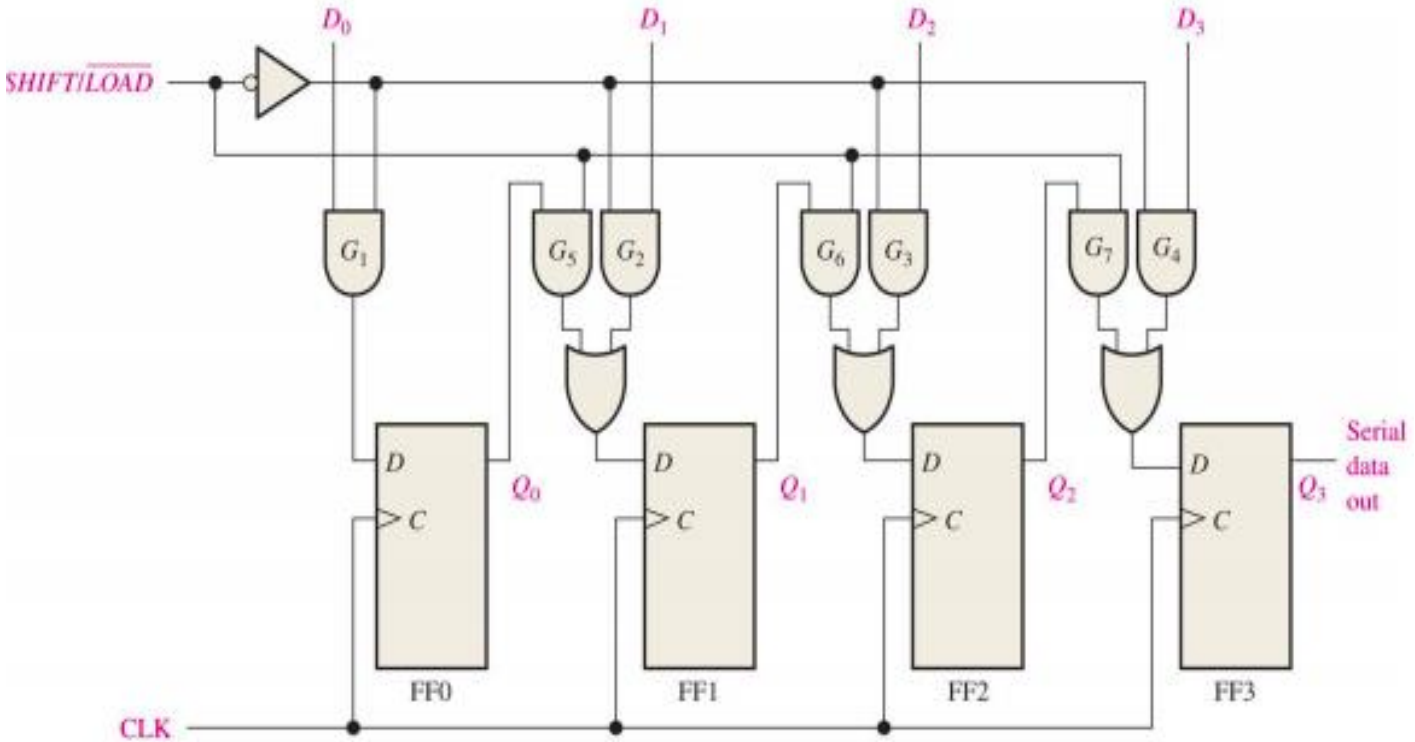
a) 0000
b) 1111
c) 0111
d) 1000

4-bit Parallel-in to Parallel-out Shift Register

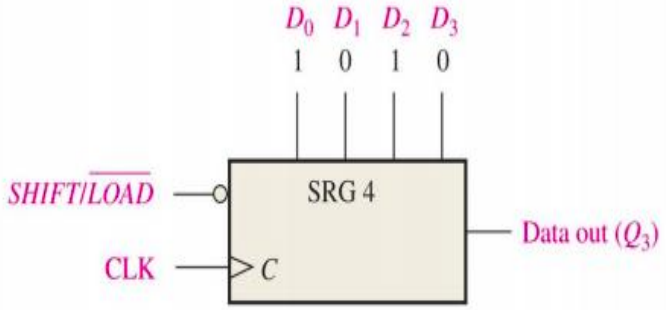


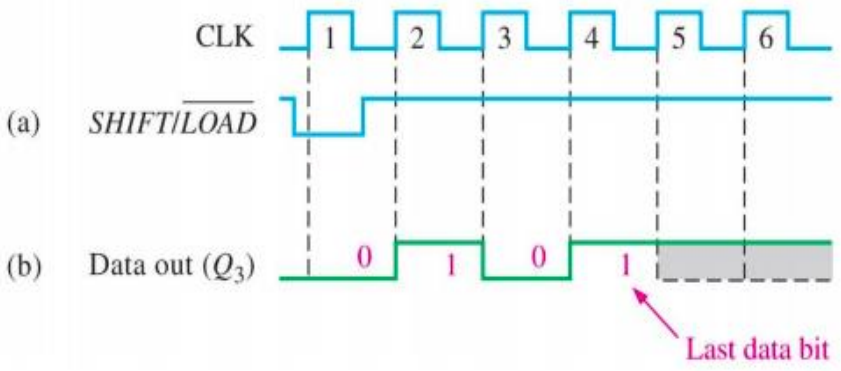


PISO Shift Register



(a) Logic diagram





Require 1 clk to load parallel data

Ring Counter

- It is a type of counter in which the output of the last flip flop is connected as an input to the first flip-flop is known as a *Ring counter*.

- The input is shifted between the flip-flops in a ring shape , so it is known as a Ring counter.

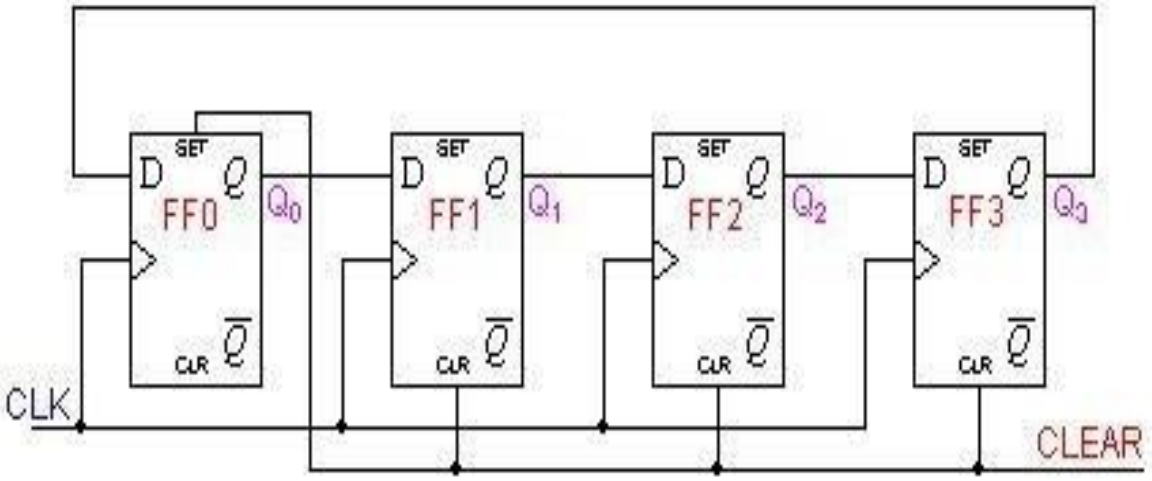
- A Ring counter is a synchronous counter.

The synchronous counter has a common clock signal that triggers all the Flip-flops at the same time.

Ring Counter

- Ring counter consists of D-flip flops connected in cascade setup with the output of last Flip-flop connected to the input of first Flip-flop.

Ring counter has Mod = n ‘n’ is the number of bits.
It means 4-bit ring counter has 4 states.



Clock Pulse	Q3	Q2	Q1	Q0
0	0	0	0	1
1	0	0	1	0
2	0	1	0	0
3	1	0	0	0

Ring counter divides the frequency of the clock signal by ‘n’.

Merits

Can be implemented using D and JK flip-flops. It is a self-decoding circuit.

Demerits

A ring counter of n-bits has only n valid states instead of 2^n.

This makes them inefficient in terms of state-usage.

MCQ

. the number of flip flops required for a mod 16 ring counter are

A. 4 flip flops

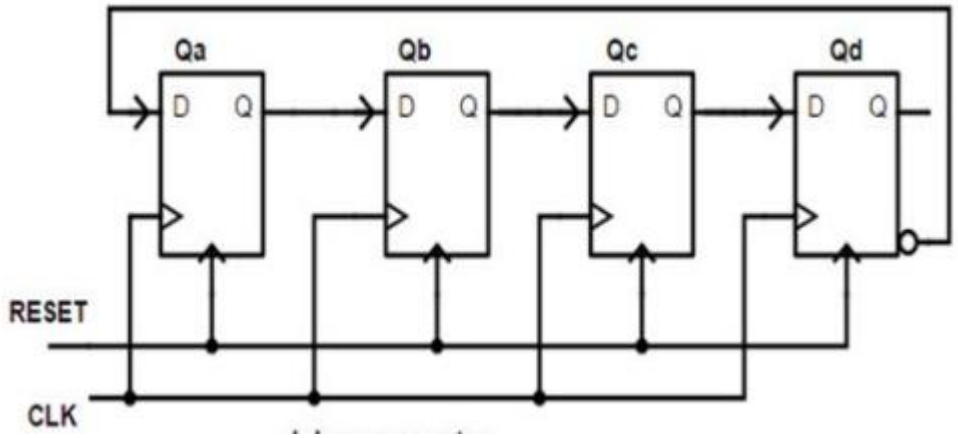
B. 8 flip flops

C. 10 flip flops

D. 16 flip flops

Johnson or Twisting Ring Counter

- The Johnson counter is a modification of ring counter.
- In this the inverted output of the last stage flip flop is connected to the input of first flip flop.
- If we use N flip flops to design the Johnson counter, it is known as 2N bit Johnson counter or Mod 2N Johnson counter.



Q_A	Q_B	Q_C	Q_D
0	0	0	0
1	0	0	0
1	1	0	0
1	1	1	0
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1
repeat			

Last FF output(~Q) feed back input to first FF
Count 2n clock pulse
MOD-2N counter

This is an advantage of the Johnson counter that it requires only half number of flip flops that of a ring counter uses, to design the same Mod.

Johnson counter divides a clock signal's frequency by '2N'.

N is the bit size of the counter.

MCQ

Ring shift and Johnson counters are _____ .

a) Synchronous counters
b) Asynchronous counters
c) True binary counters
d) Synchronous and true binary counters

MCQ

In a 4-bit Johnson counter sequence, there are a total of how many states or bit patterns?

a) 1
b) 3
c) 4
d) 8