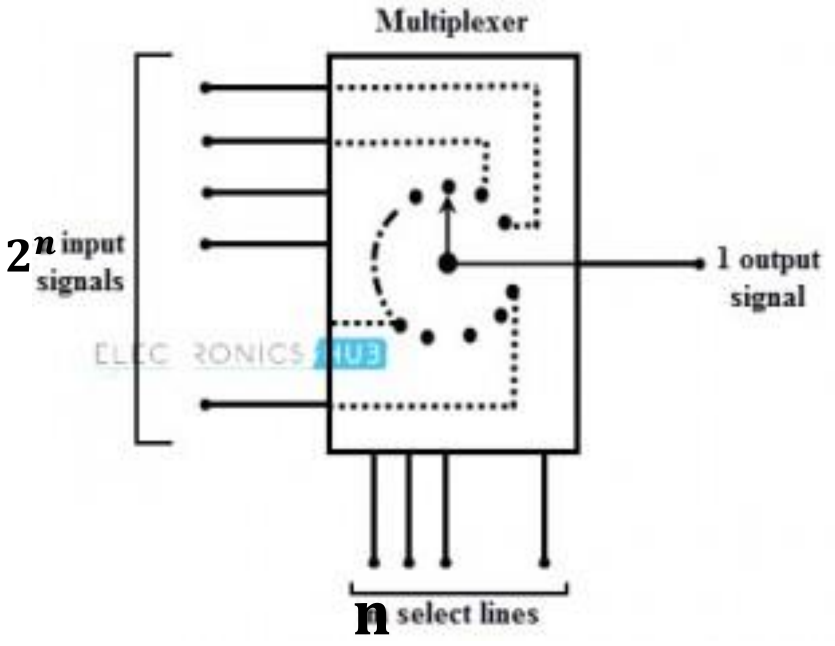
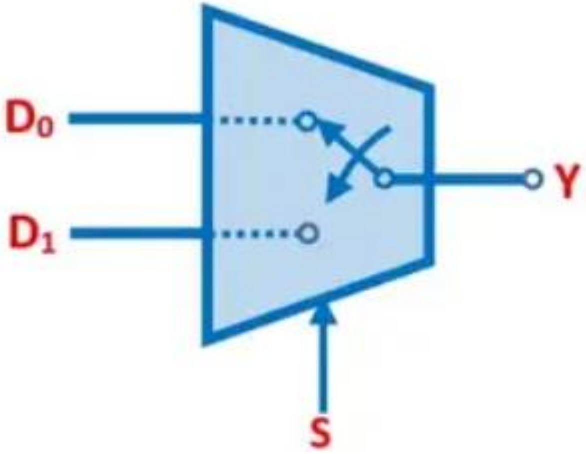
Unit-5 : Combinational Circuit

Multiplexers-De-multiplexers
Decoder-Encoder

Multiplexer

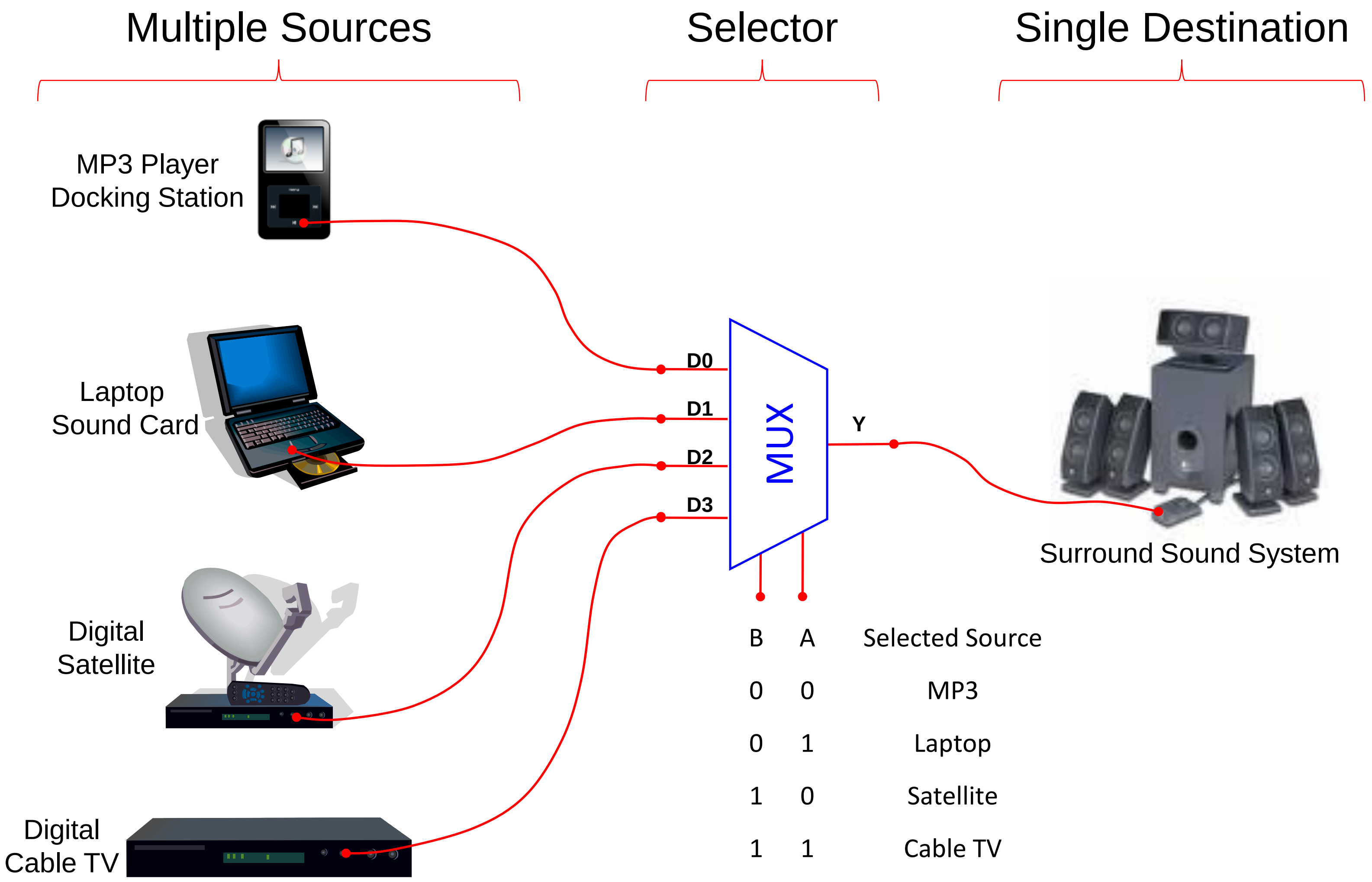
- Also called data selectors.
- Basic function: Select one of its 2^n data input lines and place the corresponding information onto a single output line.
- n input bits needed to specify which input line is to be selected.
  - Place binary code for a desired data input line onto its n select input lines.





Typical Application of a MUX

- One of the primary applications of multiplexers is to provide for the transmission of information from several sources over a single path. This process is known as multiplexing.



B	A	Selected Source
0	0	MP3
0	1	Laptop
1	0	Satellite
1	1	Cable TV

MCQ

Q. The two input MUX would have ___________

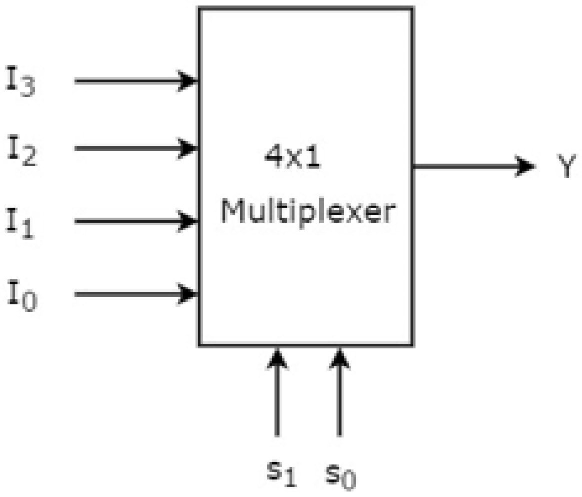
a) 1 select line
b) 2 select lines
c) 4 select lines
d) 3 select lines

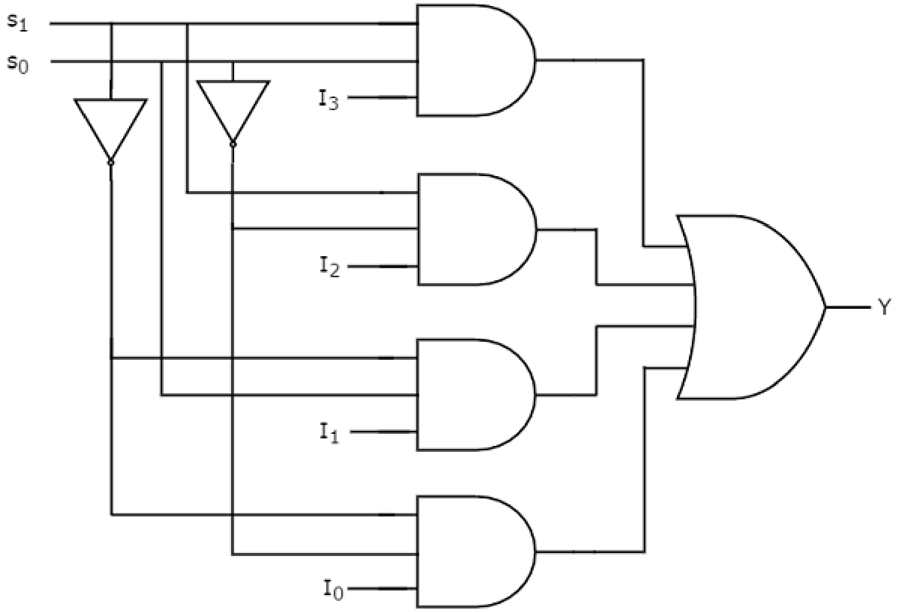
MCQ

Q. 4 to 1 MUX would have _______________

a) 2 inputs
b) 3 inputs
c) 4 inputs
d) 5 inputs

4:1 Multiplexer





Selection Lines		Output
S_1	**S_0**	**Y**
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

$$Y = S_1{}'S_0{}'I_0 + S_1{}'S_0I_1 + S_1S_0{}'I_2 + S_1S_0I_3$$

Q. Y(A, B,C) = $\sum m$ (1, 3, 5, 6) implement with 4:1 multiplexer

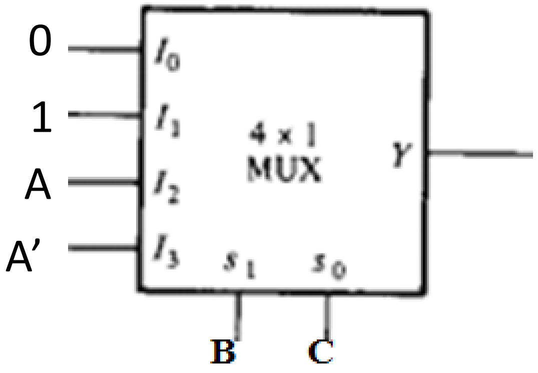
Q. Y(A, B,C) = ∑m (1, 2, 4, 5) implement with 4:1 multiplexer.

Expression implementation with Multiplexer

Q. Y(A, B,C) = ∑m (1, 3, 5, 6) implement with 4:1 multiplexer

$$Y = \overline{A}\,\overline{B}C + \overline{A}BC + A\overline{B}C + AB\overline{C}$$

Any 2 input (AB/BC/AC) select line



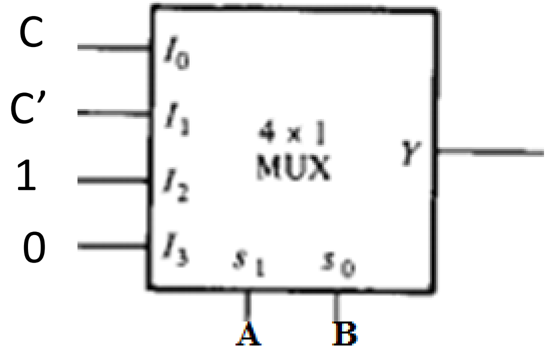
Rearrange equation with selection line

$$Y = \underset{\text{I0}}{\underline{0.(\overline{B}\,\overline{C})}} + \underset{\text{I1}}{\underline{\overline{B}C(\overline{A}+A)}} + \underset{\text{I2}}{\underline{AB\overline{C}}} + \underset{\text{I3}}{\underline{\overline{A}BC}}$$

Q. Y(A, B,C) = ∑m (1, 2, 4, 5) implement with 4:1 multiplexer

$$Y = \overline{A}\,\overline{B}C + \overline{A}B\overline{C} + A\overline{B}\,\overline{C} + A\overline{B}C$$

Any 2 input (AB/BC/AC) select line

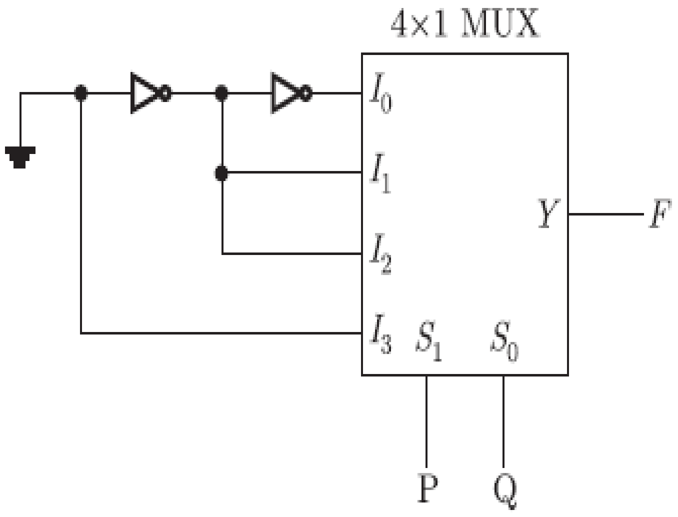


Rearrange equation with selection line

$$Y = \underset{\text{I0}}{\underline{\overline{A}\,\overline{B}C}} + \underset{\text{I1}}{\underline{\overline{A}B\overline{C}}} + \underset{\text{I2}}{\underline{A\overline{B}(\overline{C}+C)}} + \underset{\text{I3}}{\underline{AB.0}}$$

MCQ

The logic function implemented by the circuit below is (ground implies a logic "0")



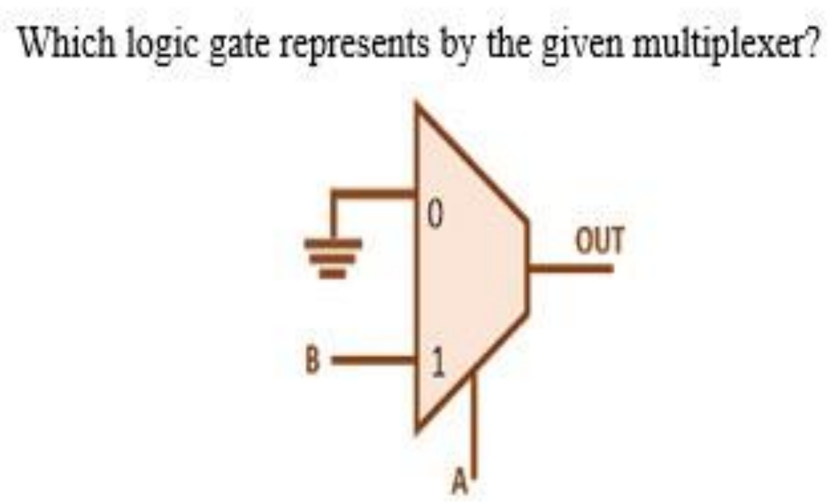
(A) $F = \text{AND}(P, Q)$

(B) $F = \text{OR}(P, Q)$

(C) $F = \text{XNOR}(P, Q)$

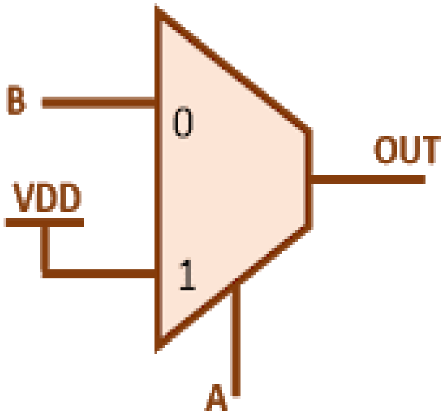
(D) $F = \text{XOR}(P, Q)$

Logic Gate implementation with 2:1 Multiplexer



Which logic gate represents by the given multiplexer?

(a)AND
(b)OR
(c)XOR
(d)NAND



(a) AND
(b) OR
(c) XOR
(d) NAND

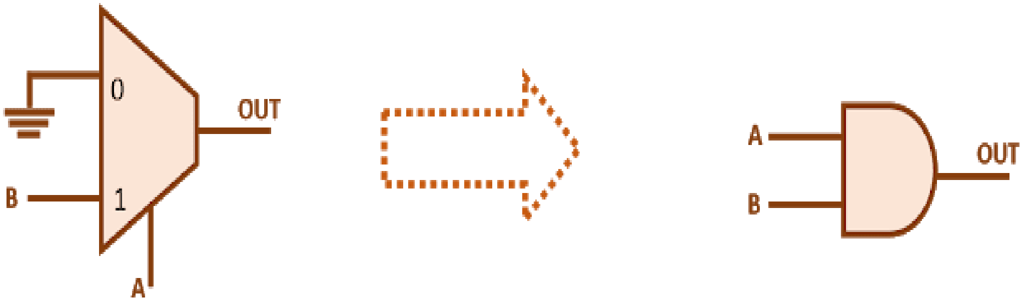
Logic Gate implementation with 2:1 Multiplexer

AND GATE

A	B	OUT
0	0	0
0	1	0
1	0	0
1	1	1

OUT = 0
when A = 0

OUT = B
when A = 1

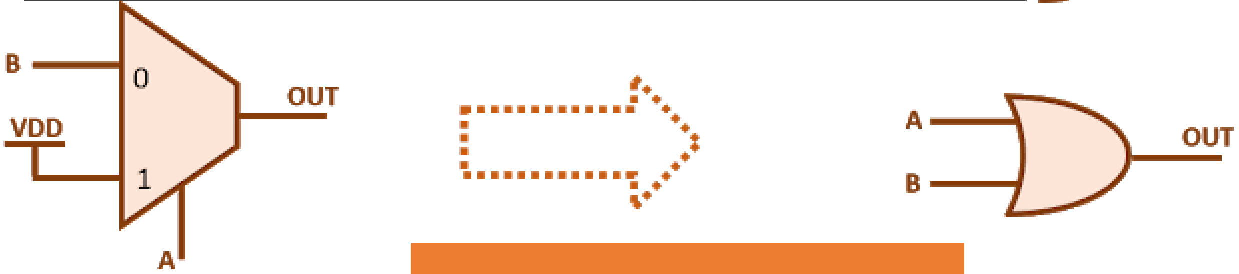


OR GATE

A	B	OUT
0	0	0
0	1	1
1	0	1
1	1	1

OUT = B
when A = 0

OUT = 1
when A = 1

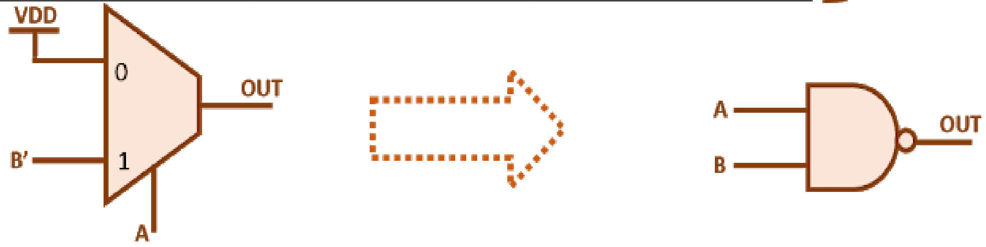


NAND GATE

A	B	OUT
0	0	1
0	1	1
1	0	1
1	1	0

OUT = 1
when A = 0

OUT = B'
when A = 1

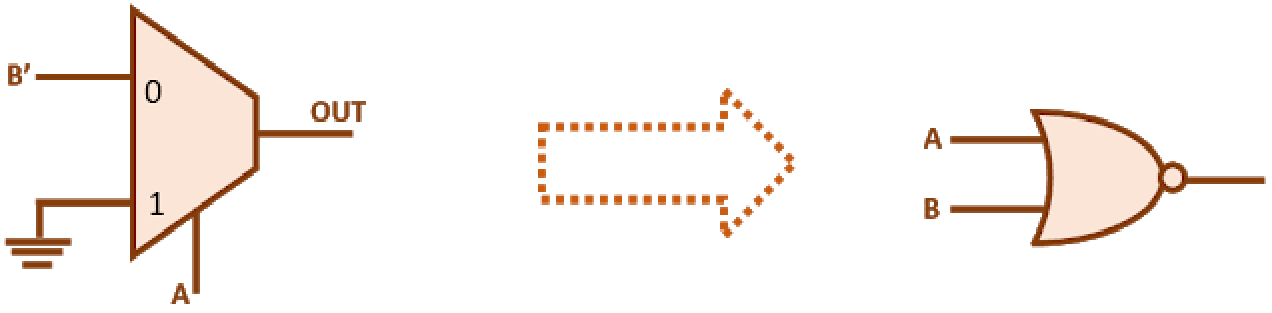


NOR GATE

A	B	OUT
0	0	1
0	1	0
1	0	0
1	1	0

OUT = B'
when A = 0

OUT = 0
when A = 1



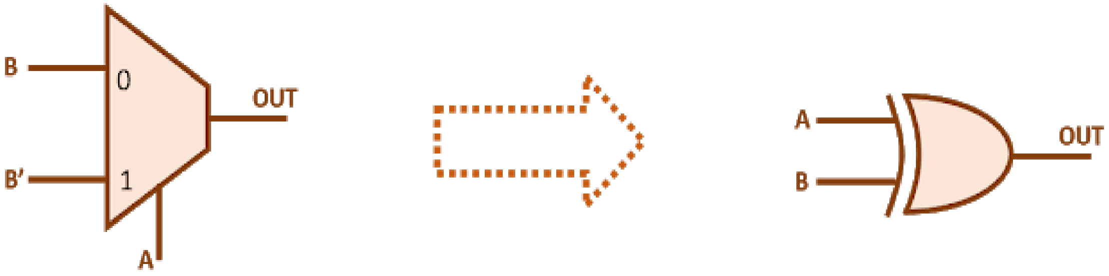
Logic Gate implementation with 2:1 Multiplexer

XOR GATE

A	B	OUT
0	0	0
0	1	1
1	0	1
1	1	0

OUT = B
when A = 0

OUT = B’
when A = 1

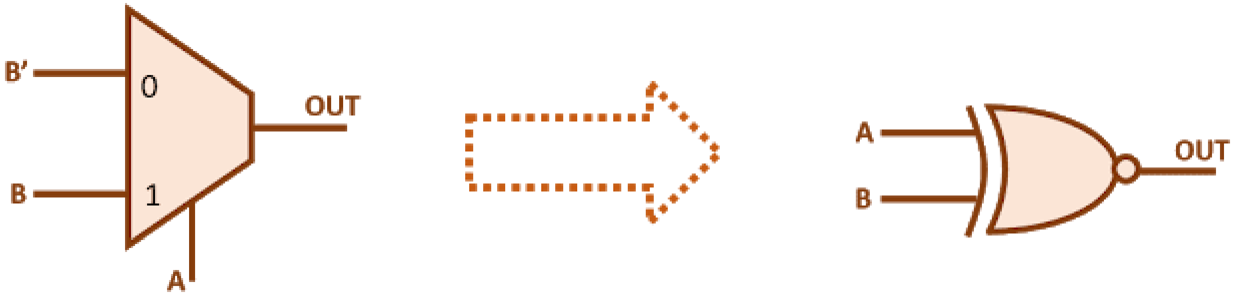


XNOR GATE

A	B	OUT
0	0	1
0	1	0
1	0	0
1	1	1

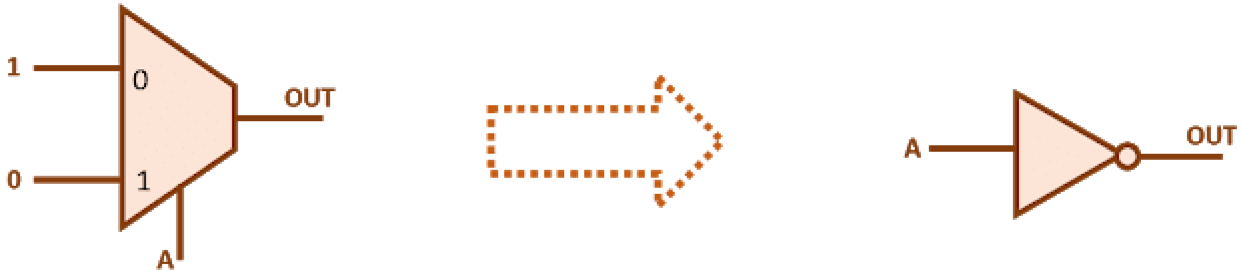
OUT = B’
when A = 0

OUT = B
when A = 1



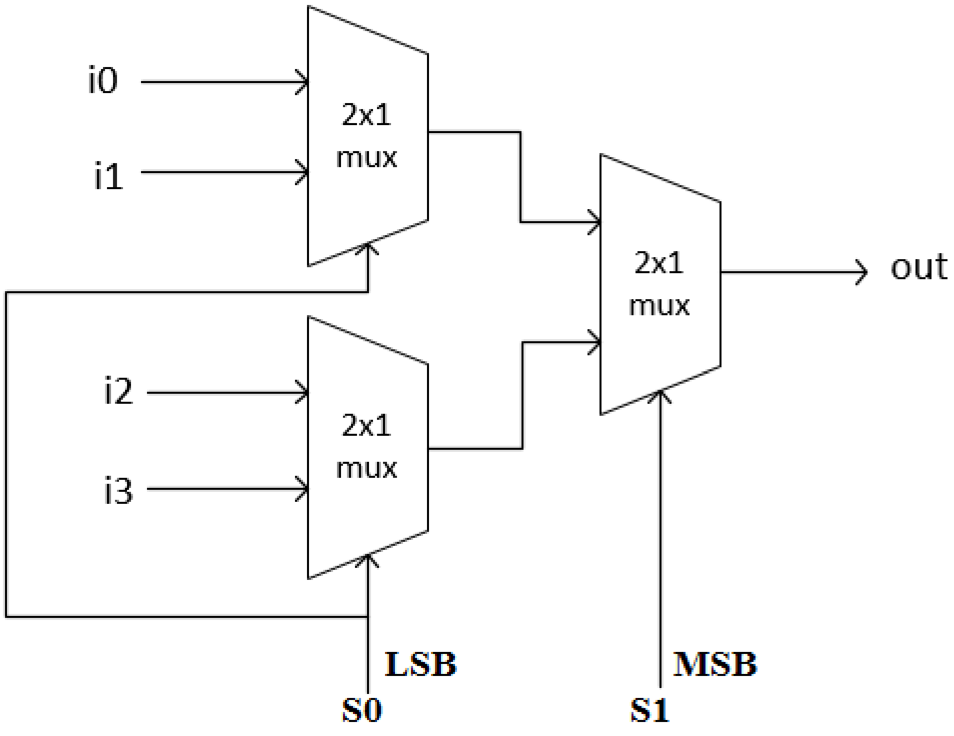
NOT GATE

A	OUT
0	1
1	0

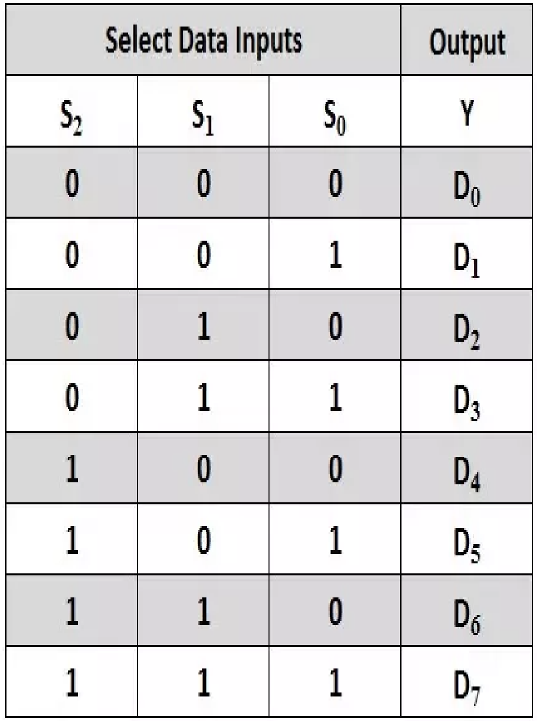


4:1 Mux using 2:1 Mux

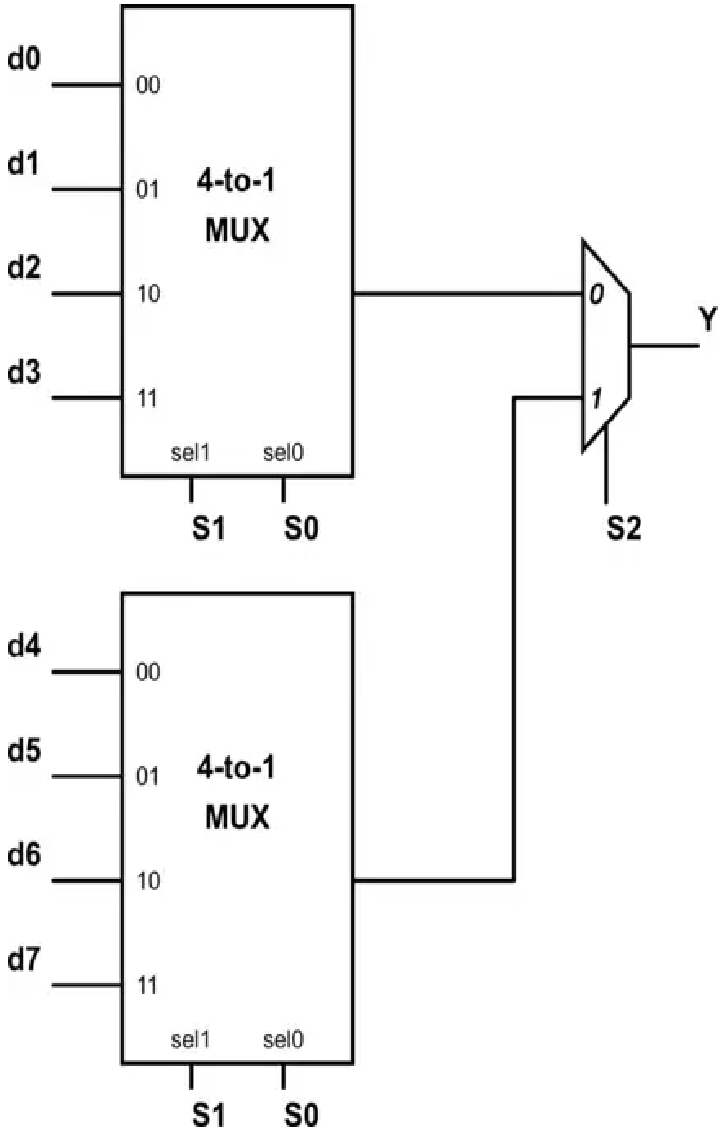
S1 (MSB)	S0(LSB)	Out
0	0	I0
0	1	I1
1	0	12
1	1	I3



8:1 Mux using 4:1 and 2:1 Mux



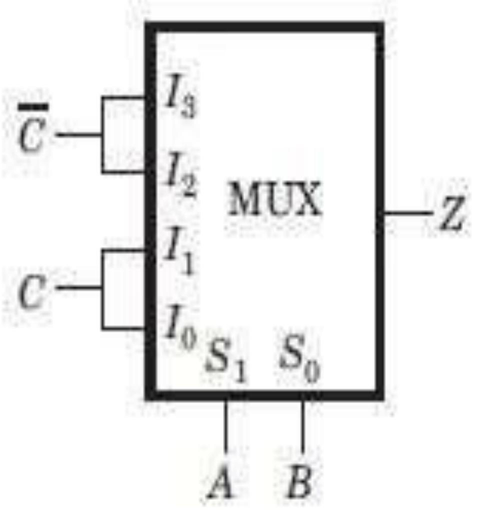
Select Data Inputs			Output
S_2	S_1	S_0	Y
0	0	0	D_0
0	0	1	D_1
0	1	0	D_2
0	1	1	D_3
1	0	0	D_4
1	0	1	D_5
1	1	0	D_6
1	1	1	D_7



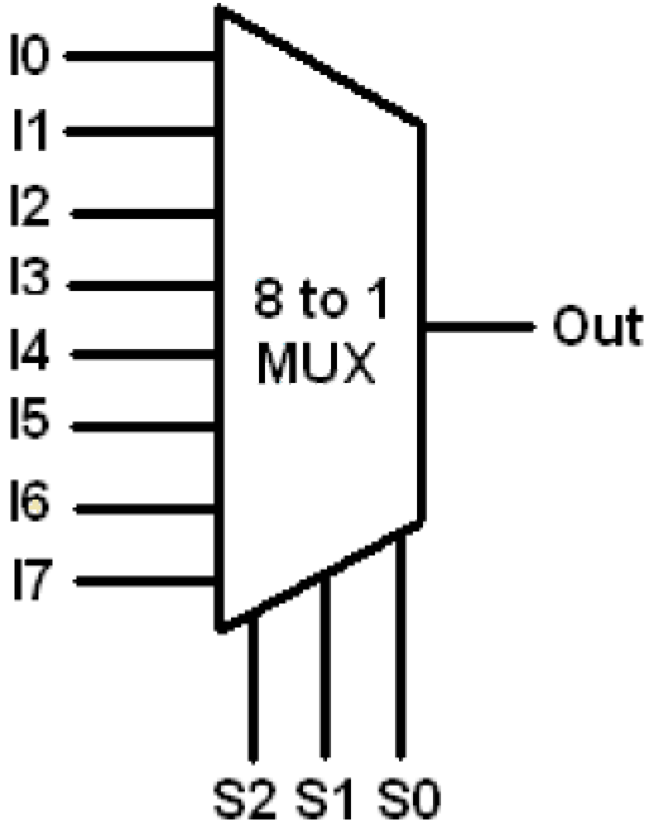
Q. Design 16:1 MUX using 4:1 MUX

Question:

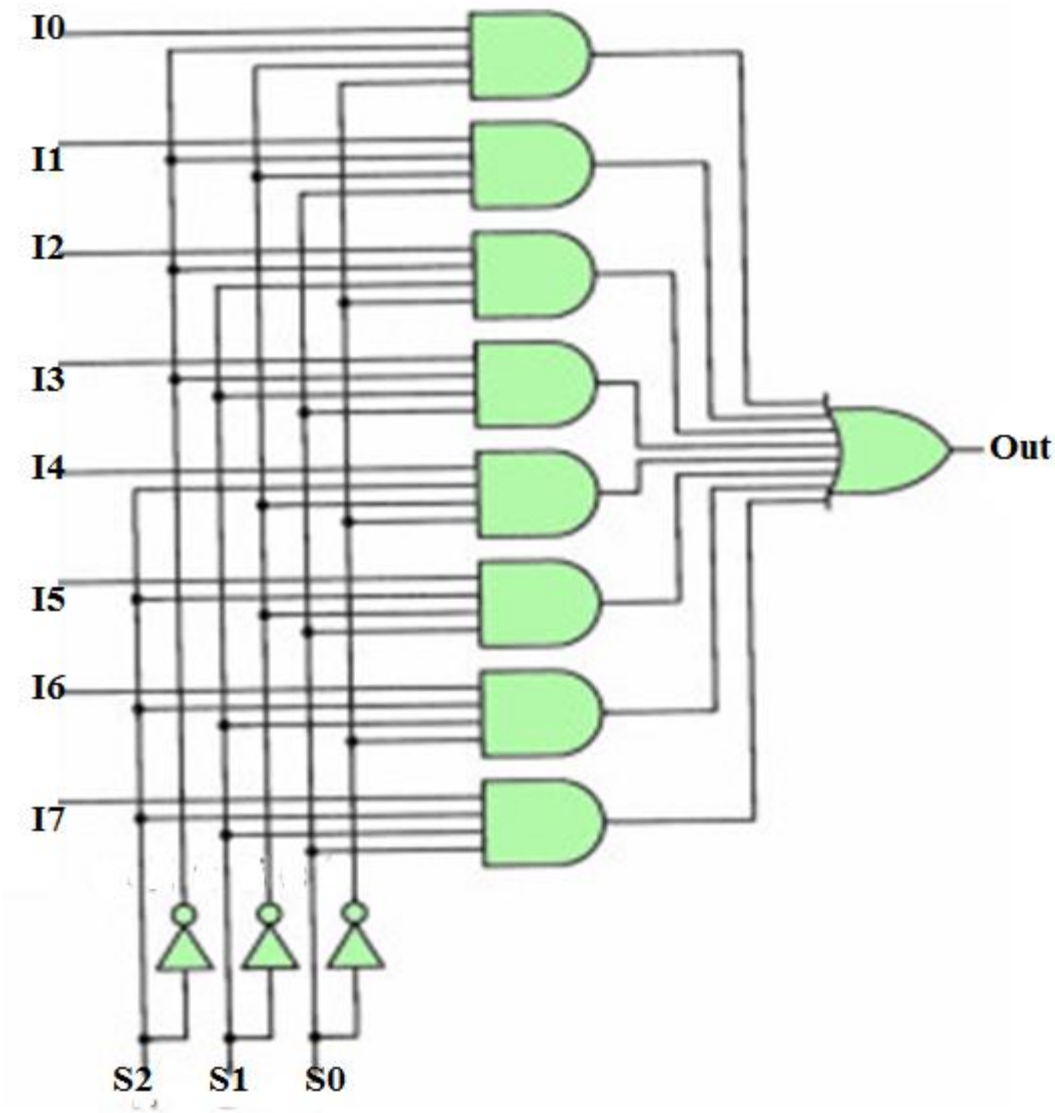
What will be the expression for the output Z.



8:1 Multiplexer



S2	S1	S0	Out
0	0	0	I0
0	0	1	I1
0	1	0	I2
0	1	1	I3
1	0	0	I4
1	0	1	I5
1	1	0	I6
1	1	1	I7

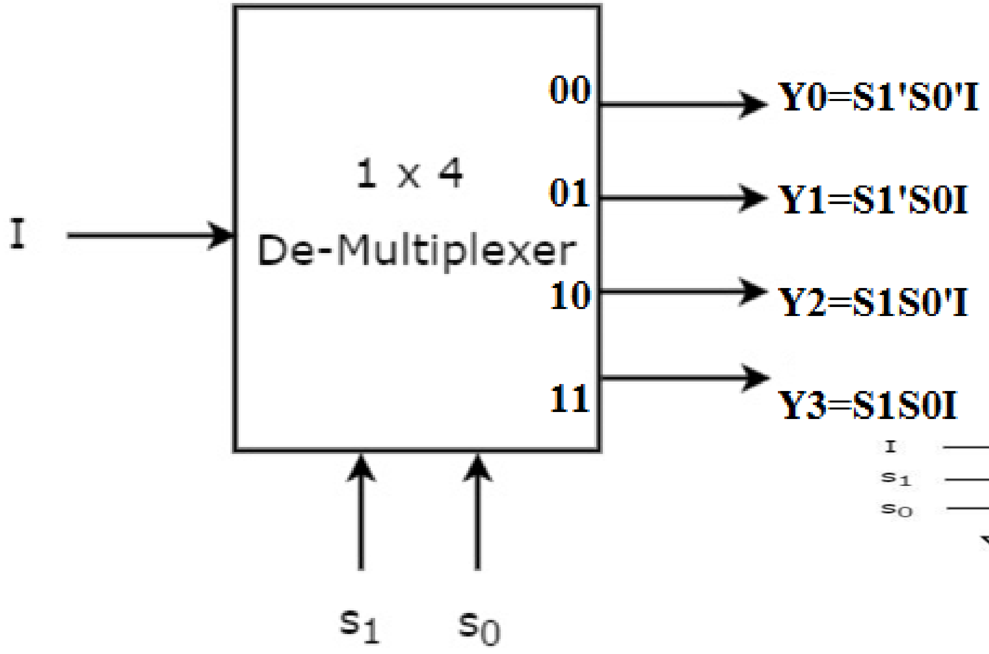


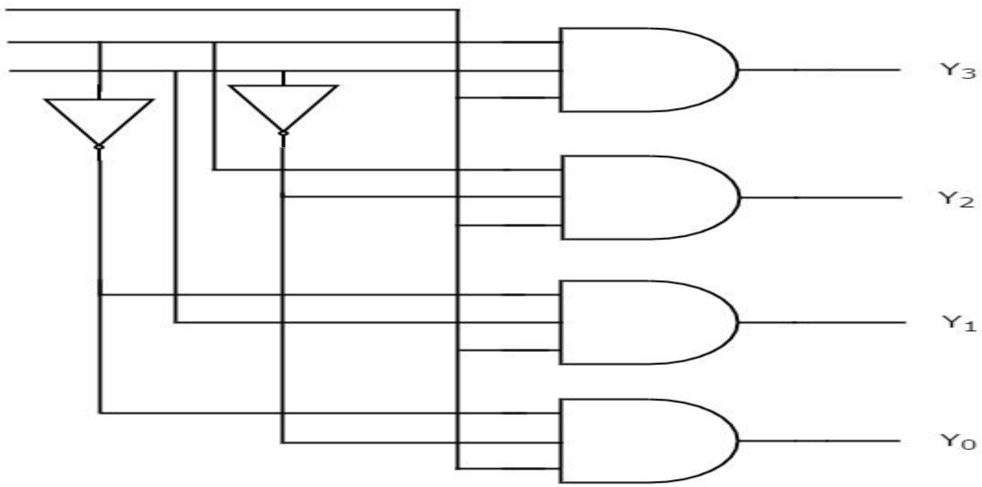
Out=S2’S1’S0’I0 + S2’S1’S0I1+ S2’S1S0’I2+ S2’S1S0I3
S2S1’S0’I4+ S2S1’S0I5+ S2S1S0’I6+ S2S1S0I7

De-multiplexer

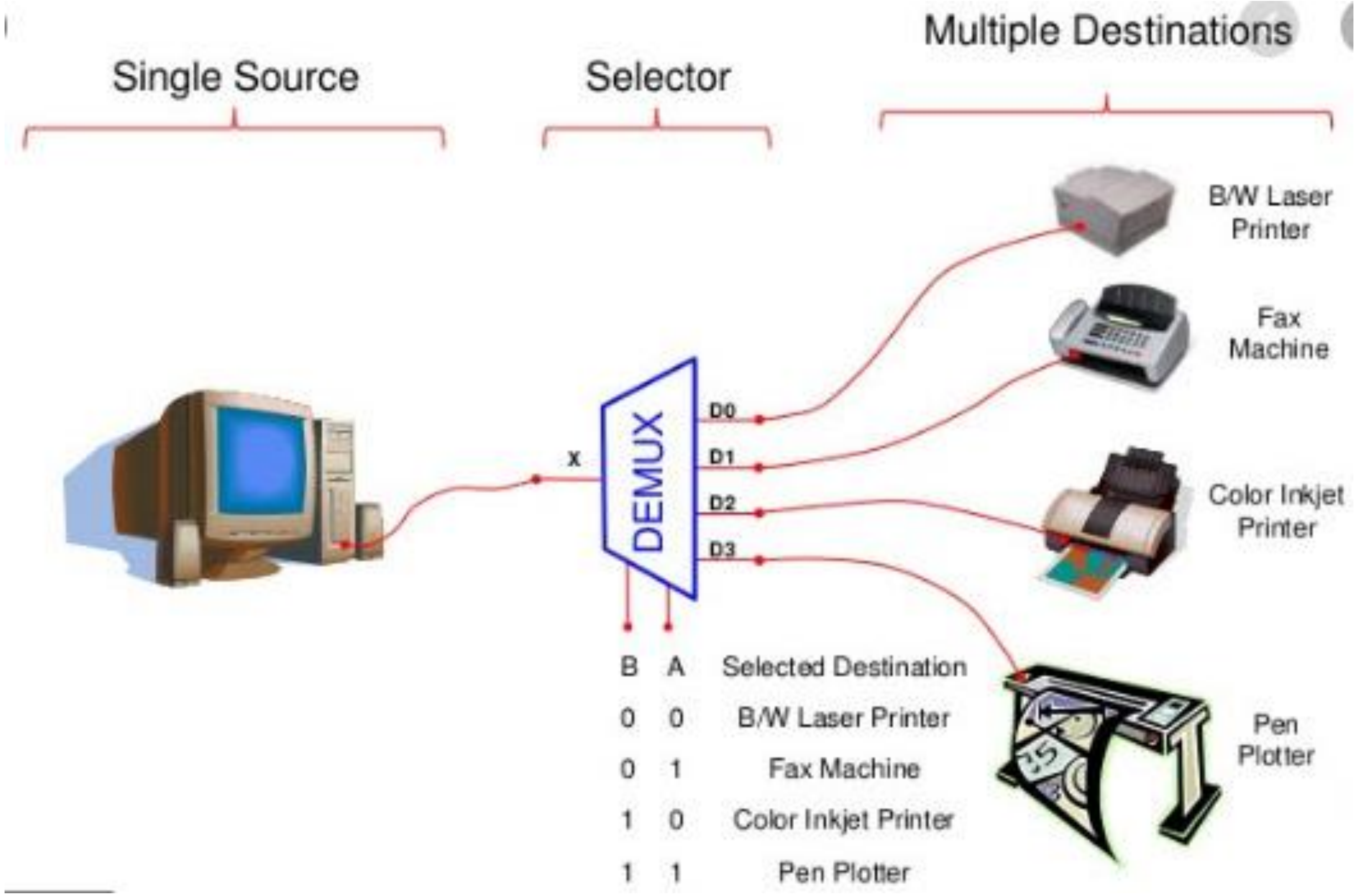
- Switch one common input line to one of several output line based on select input.
- It is data distributor.
- Size of demux $1{:}2^n$
- Example 1:4, 1:8, 1:16….. Demultiplexer

Selection Inputs		Outputs			
S_1	S_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	I
0	1	0	0	I	0
1	0	0	I	0	0
1	1	I	0	0	0



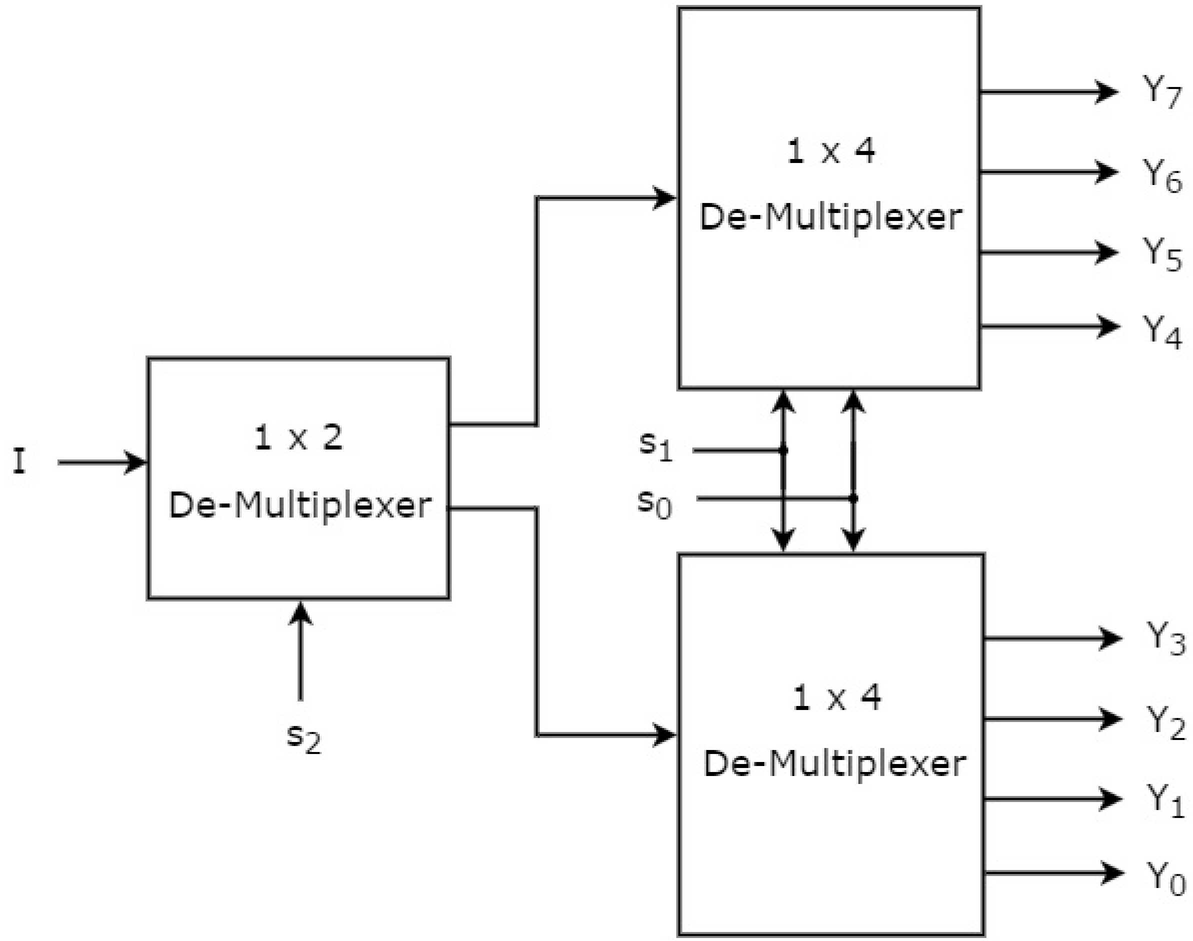


Application



B	A	Selected Destination
0	0	B/W Laser Printer
0	1	Fax Machine
1	0	Color Inkjet Printer
1	1	Pen Plotter

1:8 De-Multiplexer using lower order De-Mux

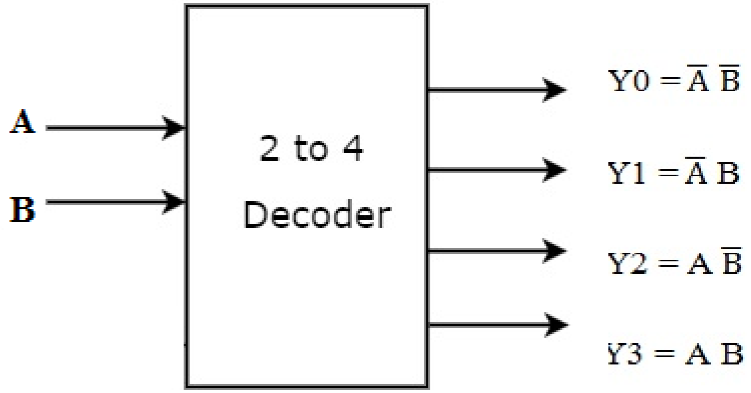


Decoder

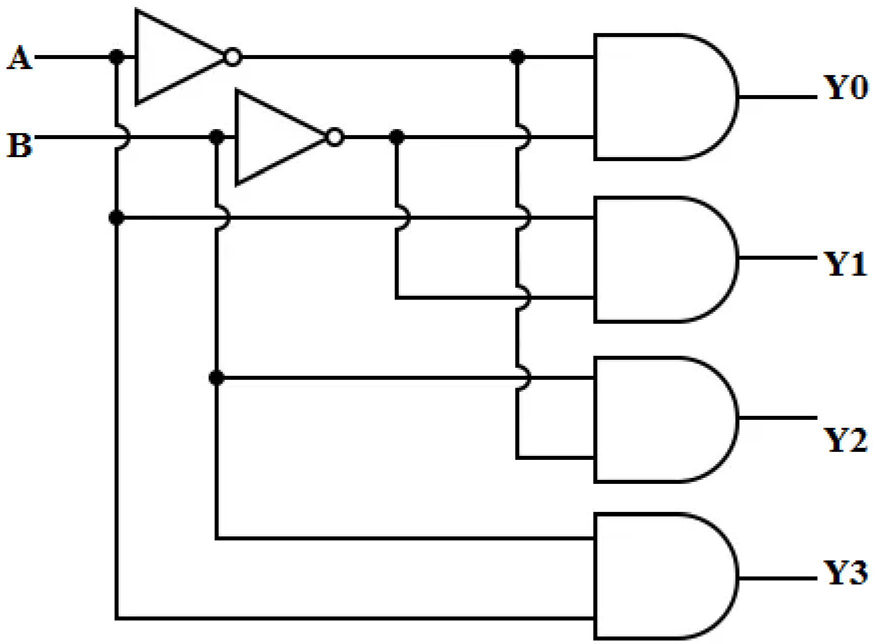
- A combinational circuit that has ‘n’ input lines and maximum of 2^n output lines.
- One of these outputs will be active High based on the combination of inputs present, when the decoder is enabled.

The outputs of the decoder are **min terms** of ‘n’ input variables lines when it is enabled.

Size of Decoder are 2:4, 3:8, 4:16….



A_1	A_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0



MCQ

Which one of the following represents the decoder ?

(a) 4:1

(b) 1:4

(c) 3:8

(d) 8:3

MCQ

How many inputs and outputs for four variable function in a decoder.

(a) 4,1

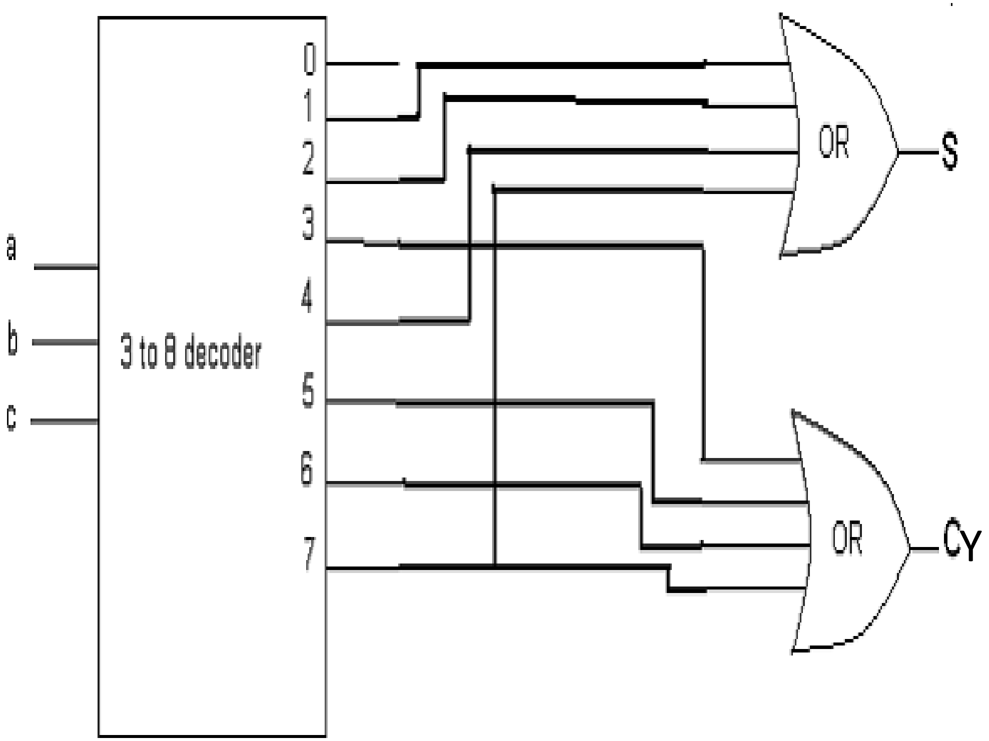
(b) 4,16

(c) 3,8

(d) 16, 1

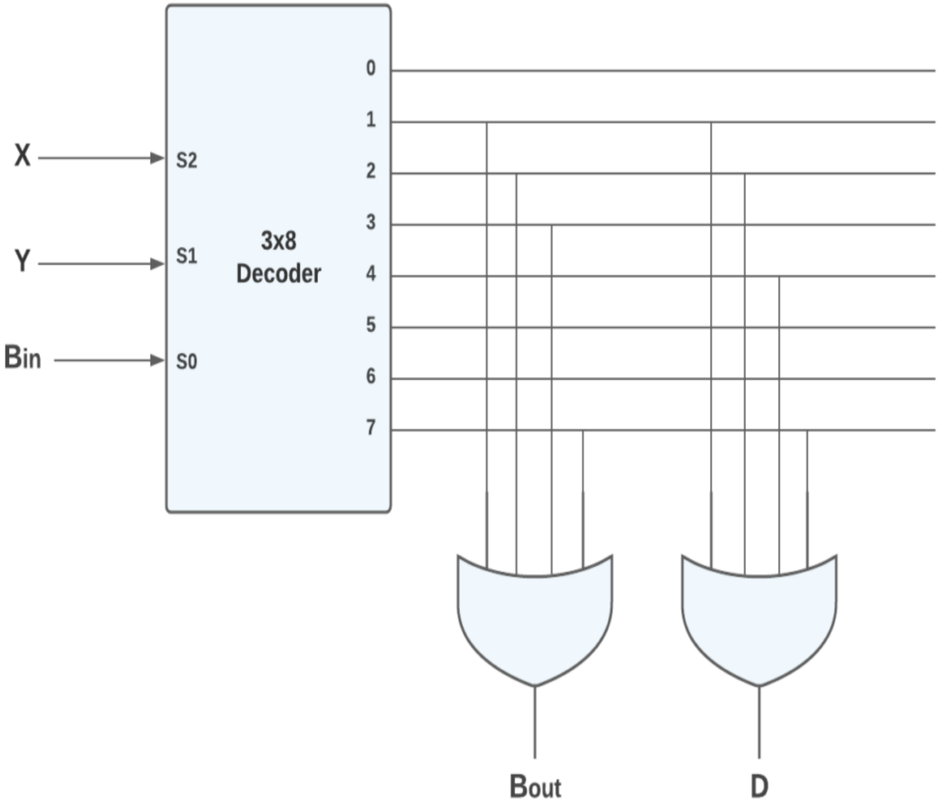
Full Adder using 3:8 Decoder

S = A’B’C + A’BC’ + AB’C’ + ABC = Σ(1,2,4,7)
CY = A’BC +AB’C +ABC’+ABC= Σ (3, 5, 6, 7)

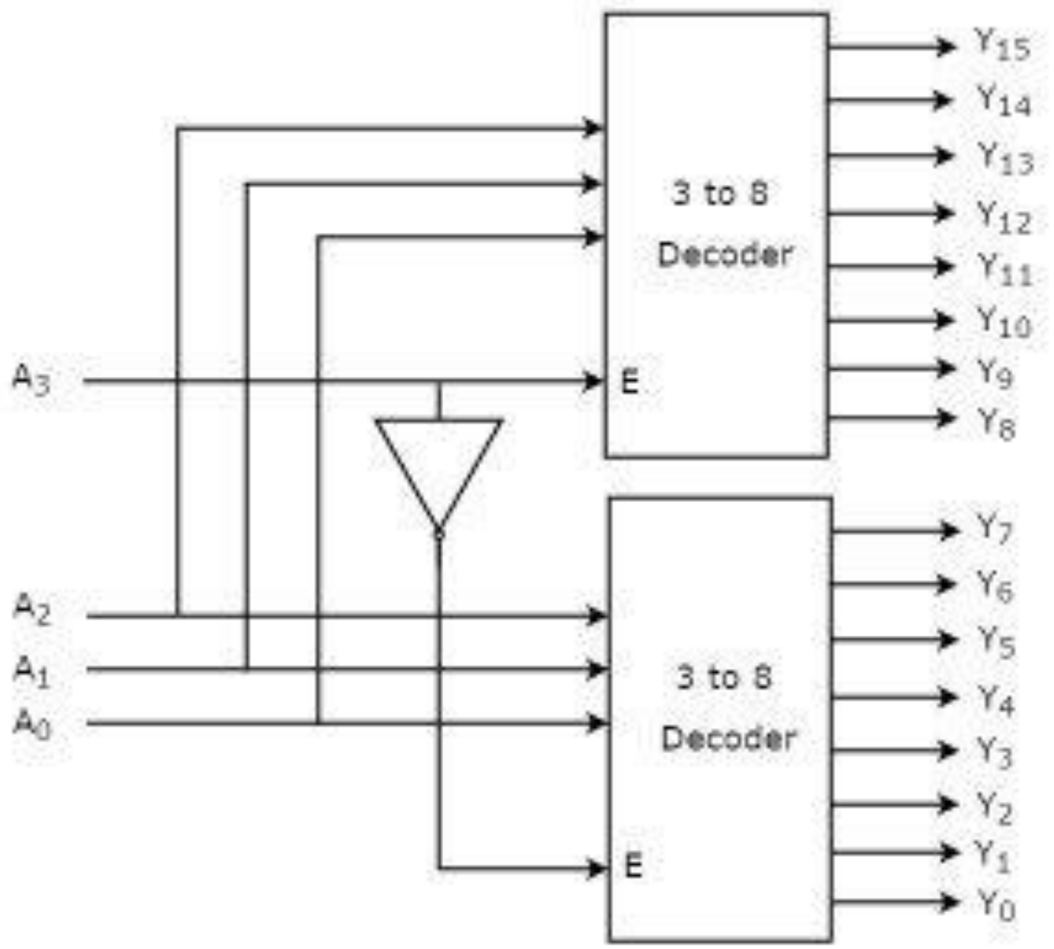


Full Subtractor using 3:8 Decoder

Difference (D) = A’B’C + A’BC’ + AB’C’ + ABC = Σ(1,2,4,7)
Borrow(Bout) = A’B’C +A’BC’ +A’BC+ABC= Σ (1, 2, 3, 7)

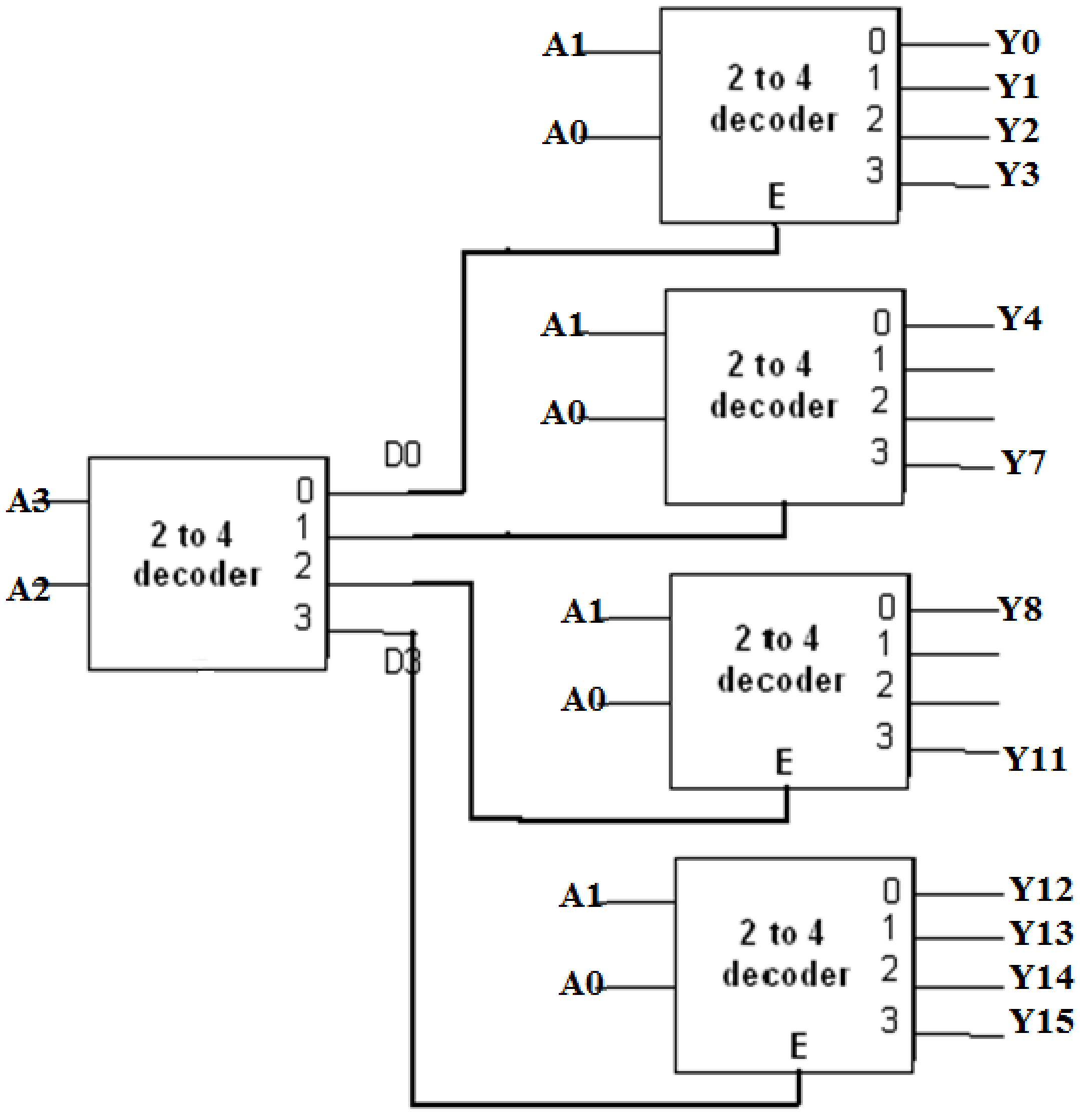


Q. Implement 4:16 decoder using 3:8 decoder.



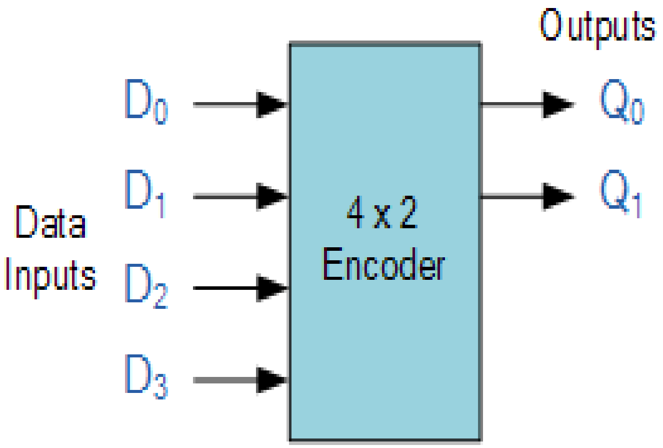
Q. Implement 4:16 decoder using 2:4 decoder

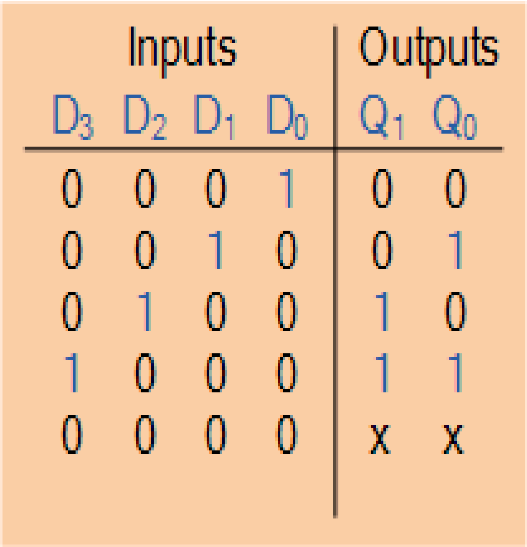
A3	A2	A1	A0	HIGH OUTPUT
0	0	0	0	Y0
0	0	0	1	Y1
0	0	1	0	Y2
0	0	1	1	Y3
0	1	0	0	Y4
0	1	0	1	Y5
0	1	1	0	Y6
0	1	1	1	Y7
1	0	0	0	Y8
1	0	0	1	Y9
1	0	1	0	Y10
1	0	1	1	Y11
1	1	0	0	Y12
1	1	0	1	Y13
1	1	1	0	Y14
1	1	1	1	Y15



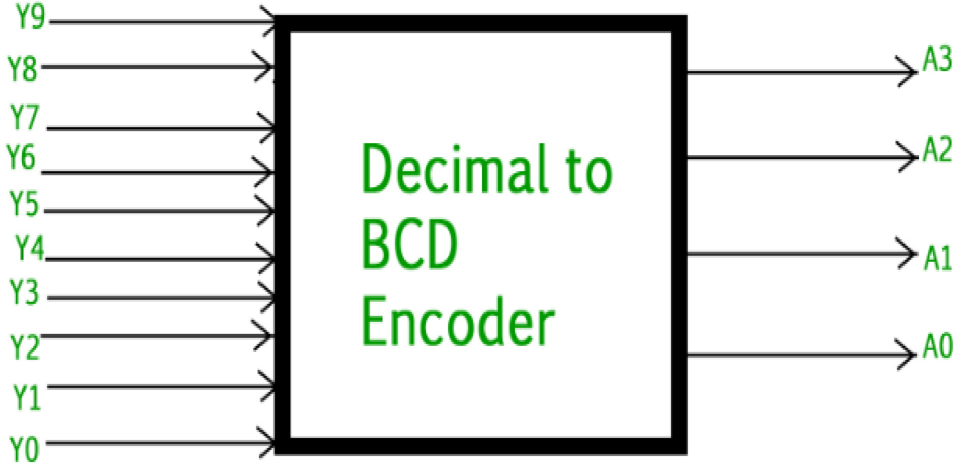
Encoder

- Reverse operation of a Decoder.
- It has a maximum of 2^n input lines and 'n' output lines.
- It encodes the information from 2^n inputs into an n-bit code.
- It will produce a binary code equivalent to the input, which is active High.

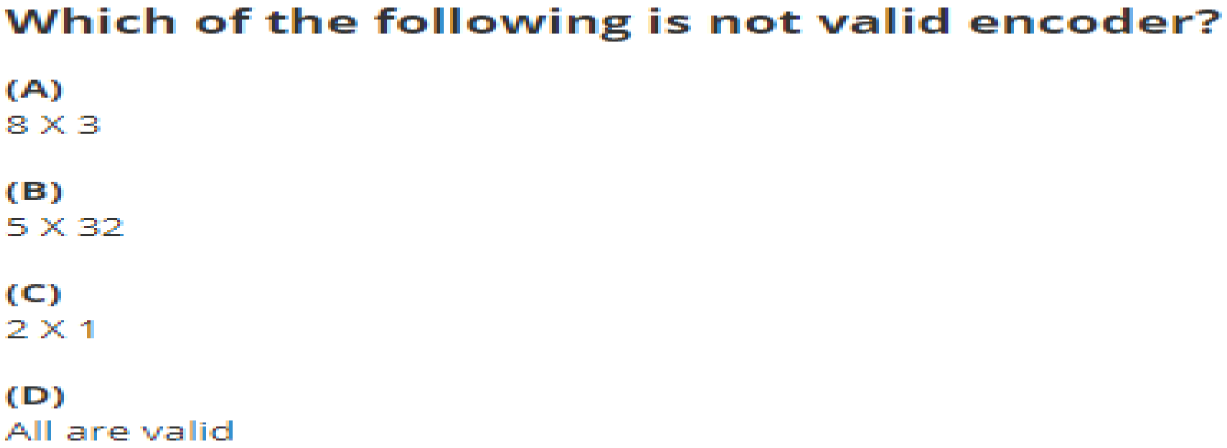




Inputs				Outputs	
D3	D2	D1	D0	Q1	Q0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1
0	0	0	0	x	x



MCQ



Which of the following is not valid encoder?

(A)
8 X 3

(B)
5 X 32

(C)
2 X 1

(D)
All are valid