UNIT-6

Counter:

Asynchronous and Synchronous

What is Counter?

- A counter is a sequential circuit that goes through a prescribed sequence of states upon the application of input pulses.
- It is a cascade combination of multiple flip-flops to which the clock pulse is provided.
- Counters are generally used for the purpose of counting in digital circuits and total number of counts represent the number of clock pulses arrived.

- Two types of counters:
  - asynchronous (ripple) counters
  - synchronous (clocked /parallel) counters

- Ripple counters allow some flip-flop outputs to be used as a source of clock for other flip-flops.

- Synchronous counters apply the same clock to all flip-flops.

Difference between synchronous and asynchronous counter

Synchronous	Asynchronous
All flip-flops are triggered simultaneously by the same clock.	Various flip-flops are activated with different clocks.
Operation speed is faster.	comparatively slower.
No propagation delay observed.	Subsequent propagation delay from one flip-flop to another.
Can be operated in any desired count sequence, as it could get manipulated by changing clock sequence.	Can operate only in a fixed count sequence, i.e., UP and DOWN
Examples : Johnson and Ring counters.	Examples- Ripple UP counter and Ripple DOWN counter

MCQ

Asynchronous counters are known as

(A) Ripple counters

(B) Multiple clock counters

(c) Decade counters

(D) Modulus counter

Design Step for Asynchronous counter

Step-1: Find the number of flip flops using $2n \geq N$,
where N is the number of states and
n is the number of flip flops.

Step-2: Choose the type of flip flop.

Step-3: Draw state diagram for the counter.

Step-4: Draw the Truth Table for asynchronous counter.

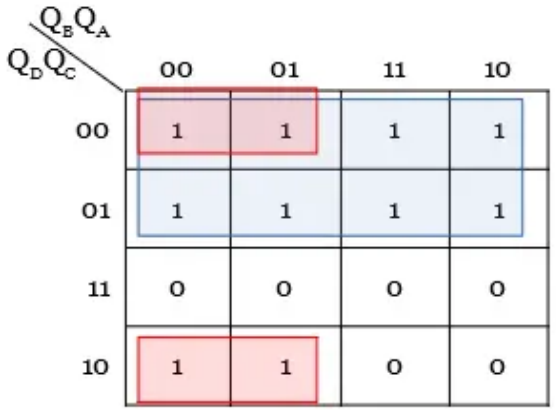
Step-5: Use K-map to derive the flip flop reset input functions.

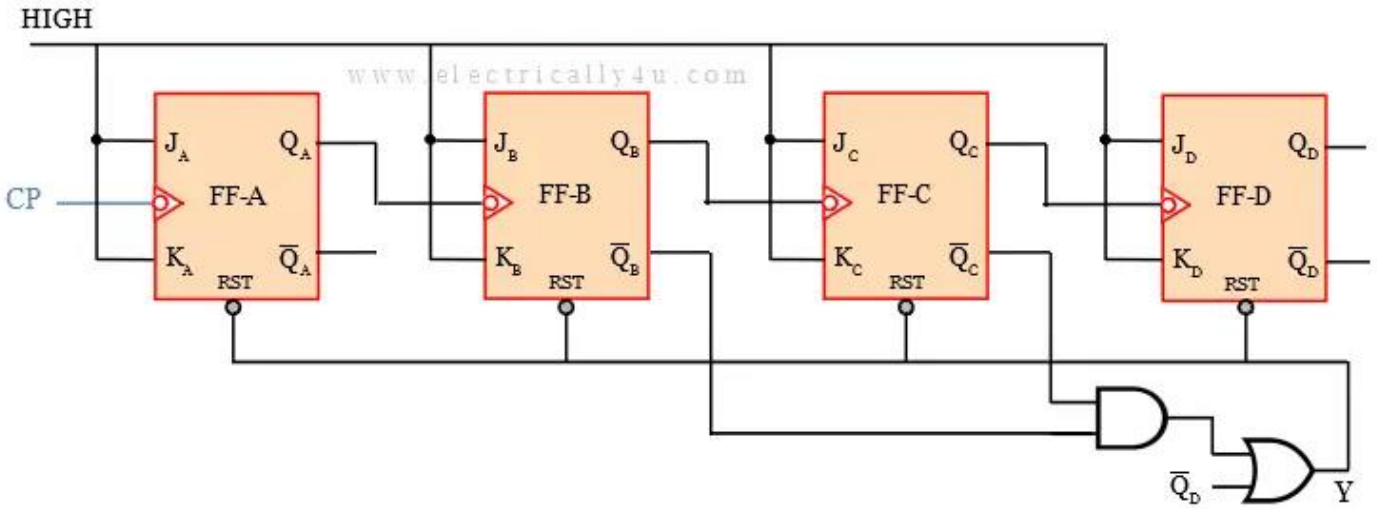
Step-6: Draw the logic circuit diagram.

Design Problem

Q. Design a BCD ripple counter (MOD 10) using JK flip flops.

Clock	BCD Counter				Output of Reset Logic Y
	Q_D	Q_C	Q_B	Q_A	
0	0	0	0	0	1
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	1
5	0	1	0	1	1
6	0	1	1	0	1
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	1

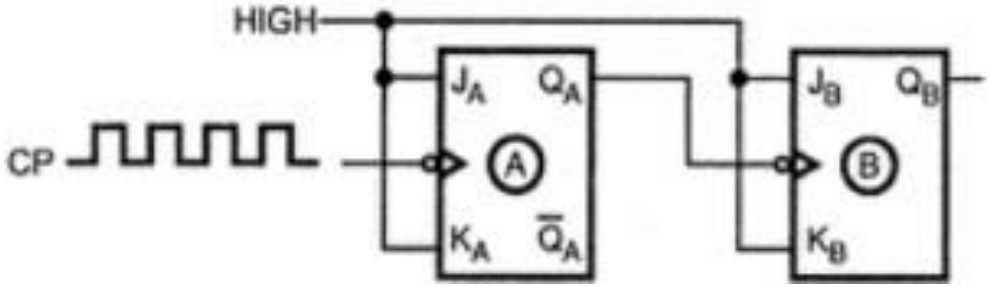


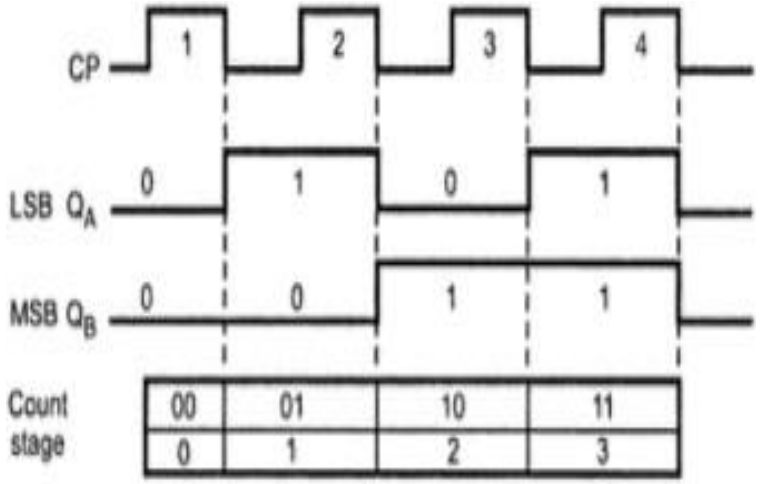


Design Mode-12 Asynchronous Counter?

Asynchronous Counter

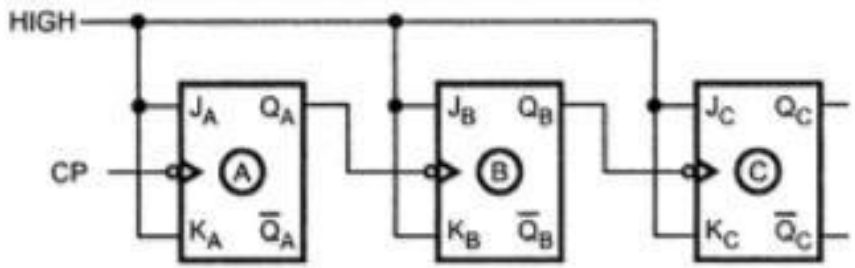
two-bit asynchronous binary counter

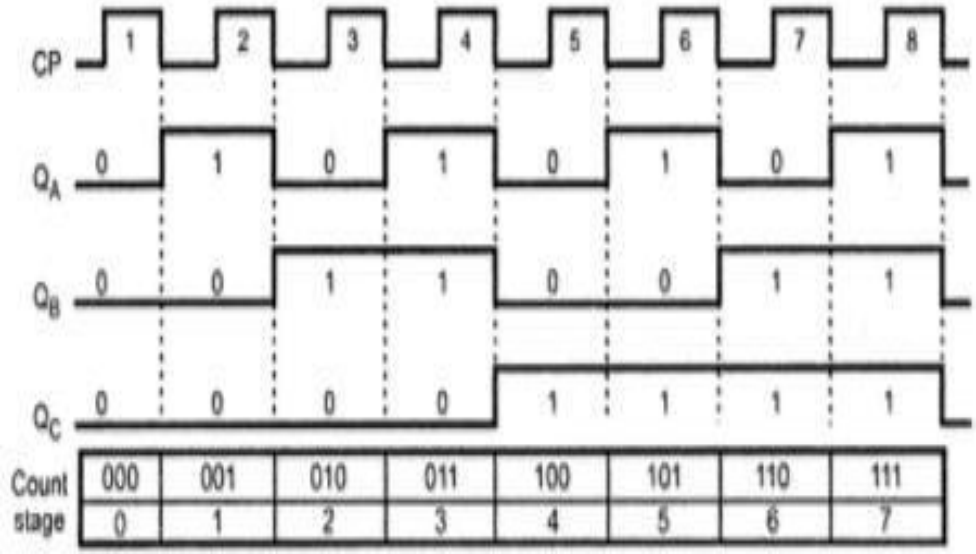




Count	00	01	10	11
stage	0	1	2	3

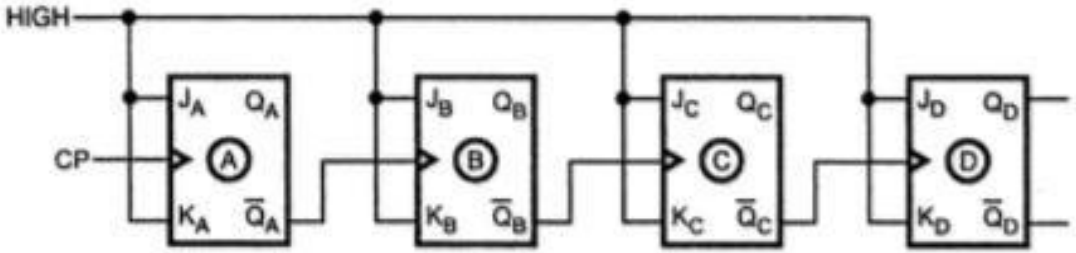
Asynchronous Counter (3- bit)





Count	000	001	010	011	100	101	110	111
stage	0	1	2	3	4	5	6	7

4-stage positive edge triggered ripple counter



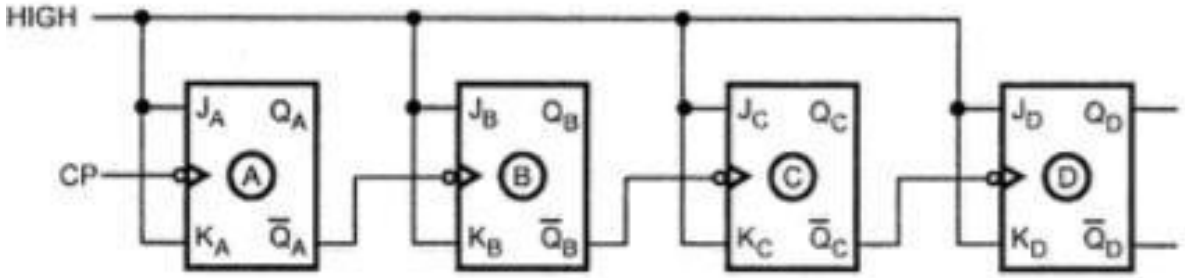
Frequency at output $Q_A = \frac{F_{CLK}}{2}$

Frequency at output $Q_B = \frac{Q_A}{2} = \frac{F_{CLK}}{4}$

Frequency at output $Q_C = \frac{Q_B}{2} = \frac{Q_A}{4} = \frac{F_{CLK}}{8}$

Frequency at output $Q_D = \frac{Q_C}{2} = \frac{Q_B}{4} = \frac{Q_A}{8} = \frac{F_{CLK}}{16}$

4-bit asynchronous down counter



Excitation Table

Q_N	Q_{N+1}	S	R	J	K	D	T
0	0	0	X	0	X	0	0
0	1	1	0	1	X	1	1
1	0	0	1	X	1	0	1
1	1	X	0	X	0	1	0

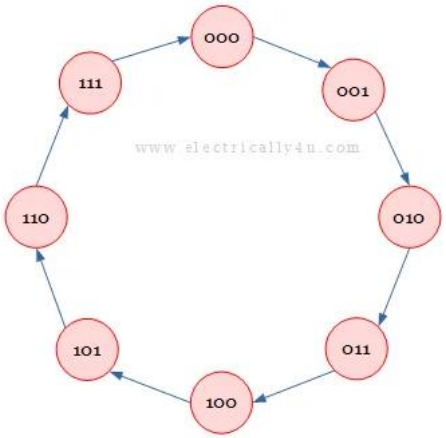
Synchronous (clocked /parallel) counters

Design Steps for Synchronous counter

Step 1: Find the number of flip flops.
Step 2: Choose the type of flip flop.
Step-3: Draw state diagram for the counter.
Step-4: Obtain excitation table for the counter.
Step 5: Derive the flip flop input functions (use K-Map)
Step-6: Draw the logic diagram of the counter.

Design Problem:

Q: **Design 3-bit Synchronous counter .**



Clock	Present State			Next State			Flip flop Inputs					
	Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_A
1	0	0	0	0	0	1	0	x	0	x	1	x
2	0	0	1	0	1	0	0	x	1	x	x	1
3	0	1	0	0	1	1	0	x	x	0	1	x
4	0	1	1	1	0	0	1	x	x	1	x	1
5	1	0	0	1	0	1	x	0	0	x	1	x
6	1	0	1	1	1	0	x	0	1	x	x	1
7	1	1	0	1	1	1	x	0	x	0	1	x
8	1	1	1	0	0	0	x	1	x	1	x	1

For J_C

Q_BQ_A / Q_C	00	01	11	10
0	0	0	1	0
1	x	x	x	x

$J_C = Q_BQ_A$

For K_C

Q_BQ_A / Q_C	00	01	11	10
0	x	x	x	x
1	0	0	1	0

$K_C = Q_BQ_A$

For J_B

Q_BQ_A / Q_C	00	01	11	10
0	0	1	x	x
1	0	1	x	x

$J_B = Q_A$

For K_B

Q_BQ_A / Q_C	00	01	11	10
0	x	x	1	0
1	x	x	1	0

$K_B = Q_A$

For J_A

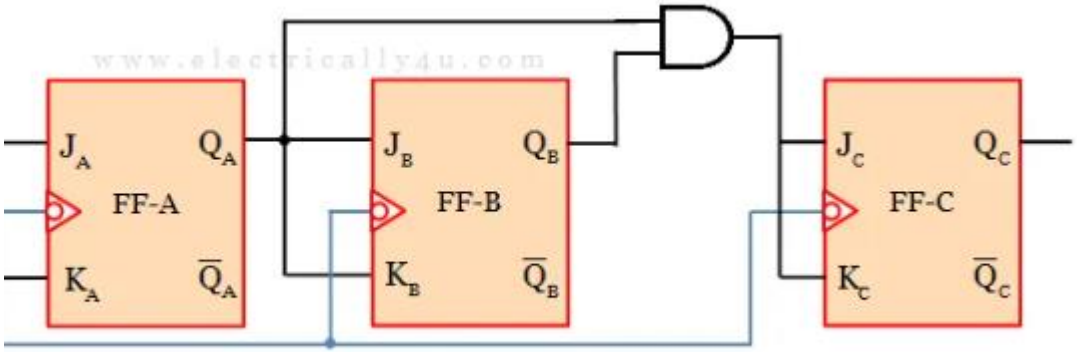
Q_BQ_A / Q_C	00	01	11	10
0	1	x	x	1
1	1	x	x	1

$J_A = 1$

For K_A

Q_BQ_A / Q_C	00	01	11	10
0	x	1	1	x
1	x	1	1	x

$K_A = 1$



MCQ

Which one is true for JK flip if present state 0 and next state 0.

(a) J= X and K= 0

(b) J= 0 and K= X

(c) J= X and K= 1

(d) J= 1 and K= X

MCQ

Which one is true for JK flip if present state 1 and next state 1.

(a) J= X and K= 0

(b) J= 0 and K= X

(c) J= X and K= 1

(d) J= 1 and K= X

Q: Design Mode-6 Synchronous Counter?

Find number of flip-flops required to build the counter.

Flip-flops required are : $2^n \geq N$.

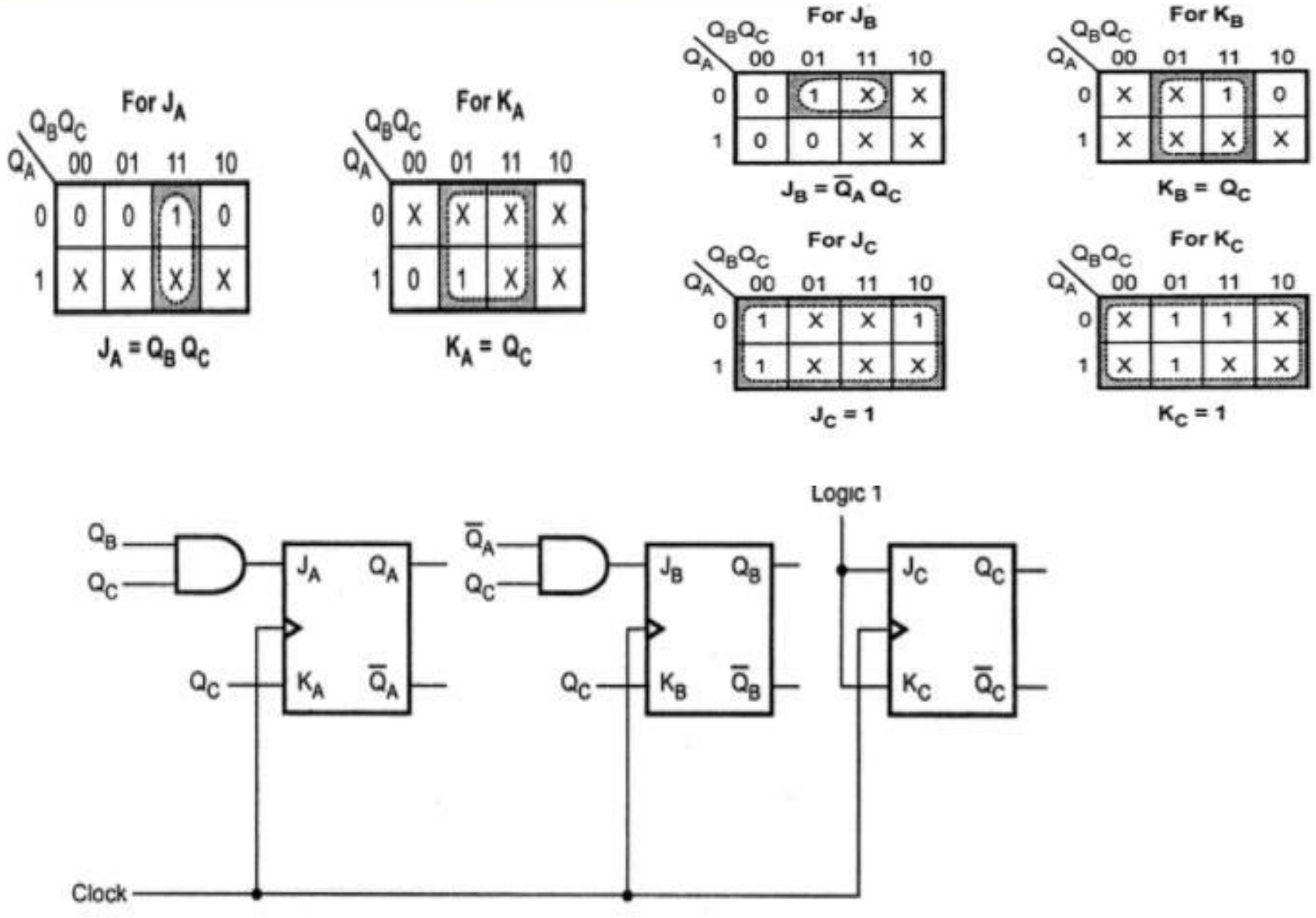
Here $N = 6 \quad \therefore n = 3$

i.e. Three flip-flops are required.

Determine the transition table.

Present state			Next state			Flip-flop inputs					
Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	x	0	x	1	x
0	0	1	0	1	0	0	x	1	x	x	1
0	1	0	0	1	1	0	x	x	0	1	x
0	1	1	1	0	0	1	x	x	1	x	1
1	0	0	1	0	1	x	0	0	x	1	x
1	0	1	0	0	0	x	1	0	x	x	1
1	1	0	x	x	x	x	x	x	x	x	x
1	1	1	x	x	x	x	x	x	x	x	x

Design of a Synchronous Mod-6 Counter using Clocked JK Flip-Flops



MCQ

What is the maximum possible range of bit-count specifically in n-bit binary counter consisting of ‘n’ number of flip-flops?

a) 0 to 2^n
b) 0 to $2^n + 1$
c) 0 to $2^n – 1$
d) 0 to $2^{n+1/2}$