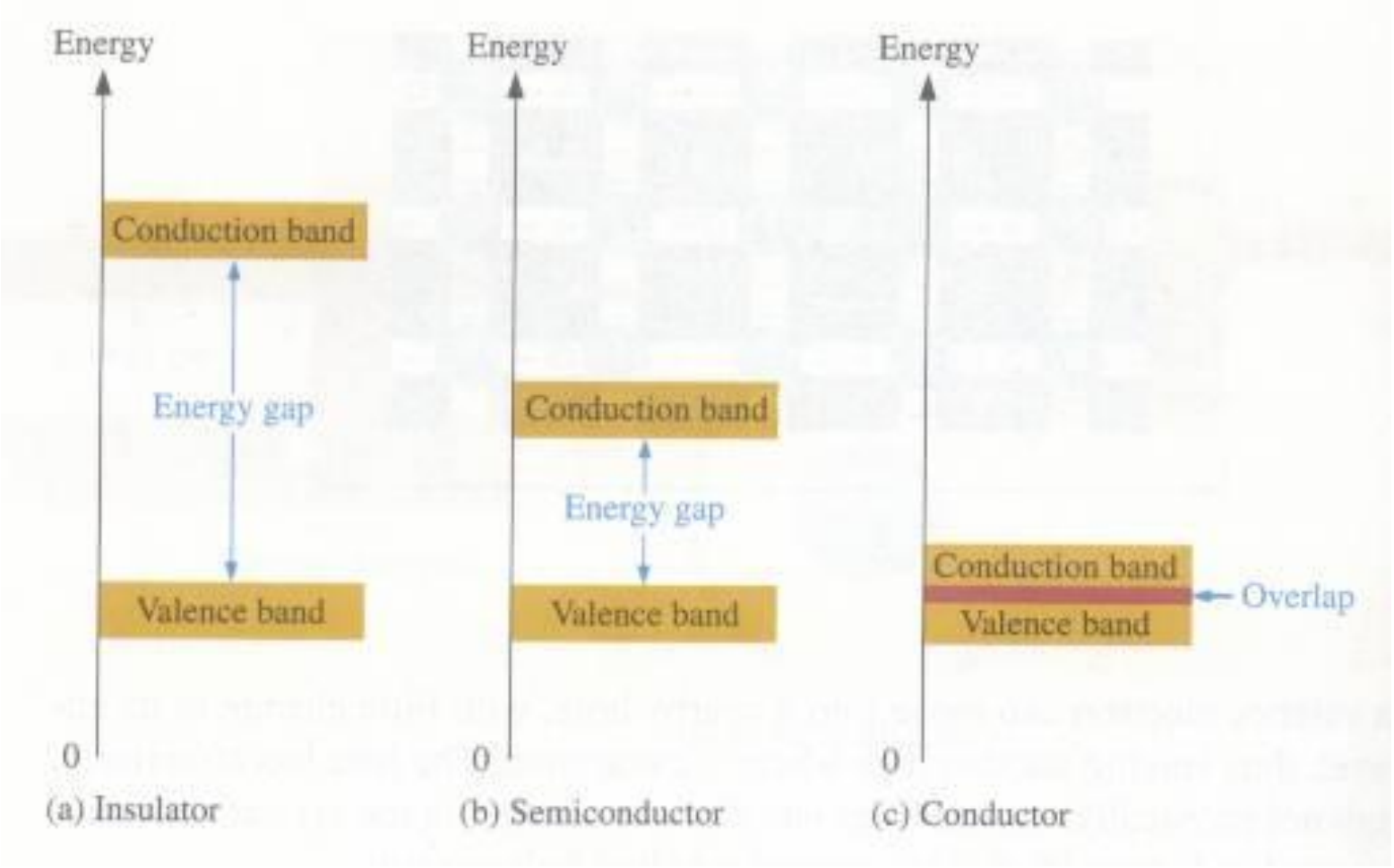
ECE249:
UNIT 2:
PN junction diode and its applications

Basic Diode Concepts

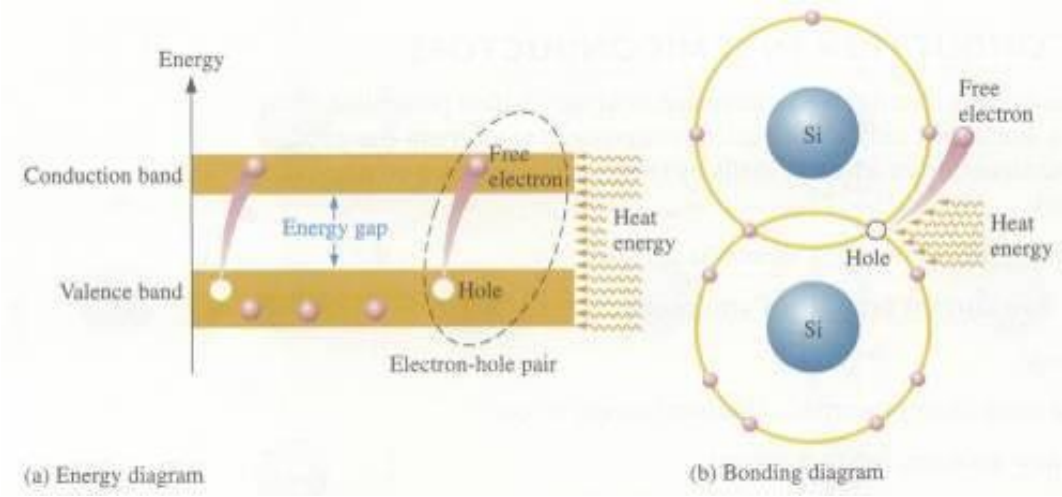
* Energy Diagrams – *Insulator, Semiconductor, and Conductor*

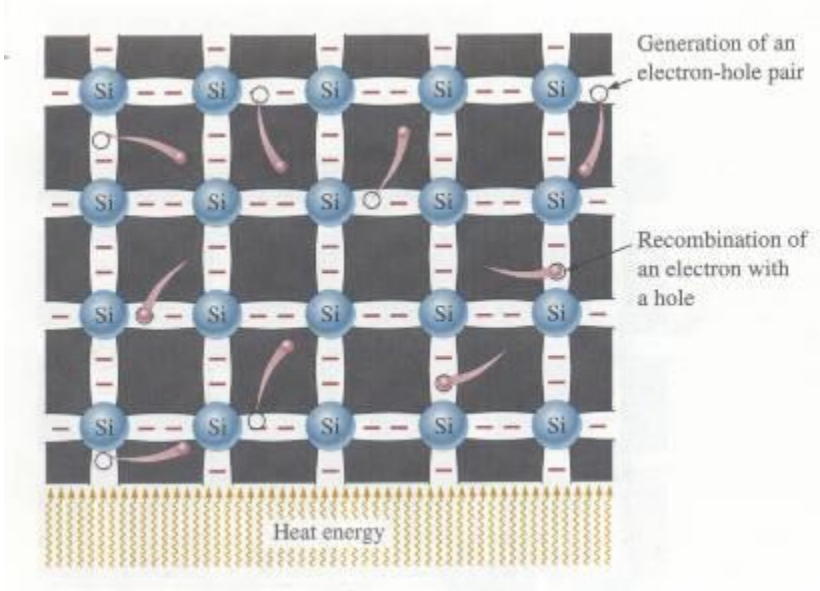
the energy diagram for the three types of solids



Intrinsic Semiconductors

* Intrinsic (pure) *Si* Semiconductor:





When equilibrium between excitation and recombination is reached:

$$\text{electron density} = \text{hole density}$$

$$n_i = p_i = 1.5\times10^{10}\ \text{cm}^{-3}$$

for intrinsic Si crystal at 300 K

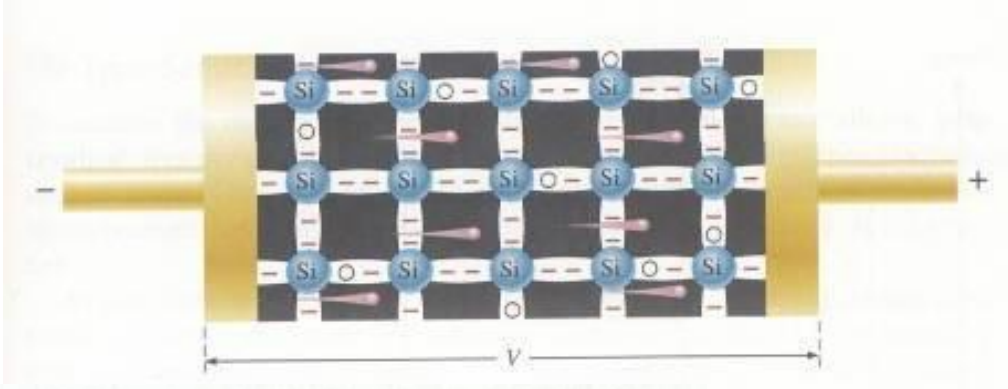
(Note: Si crystal atom density is $\sim 5\times10^{22}\ \text{cm}^{-3}$)

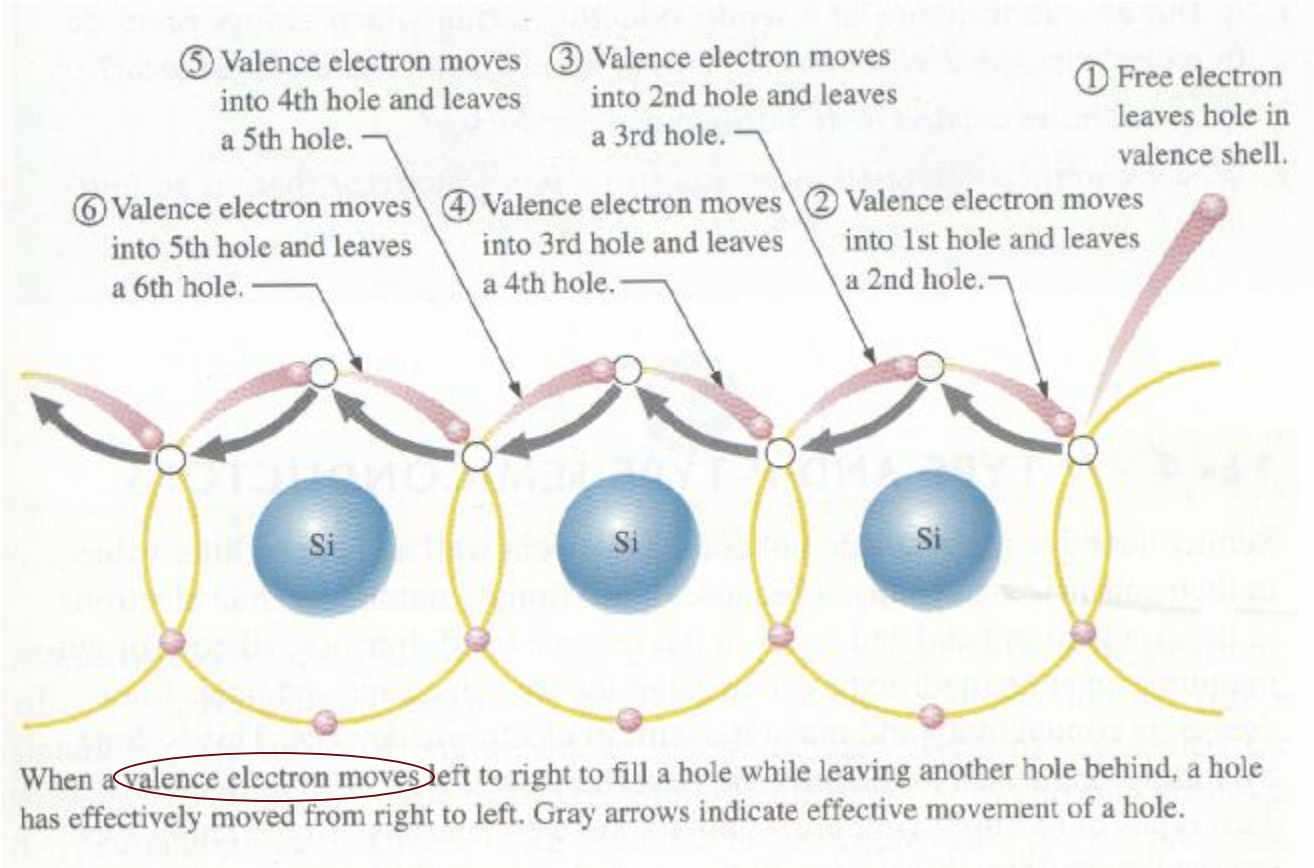
Intrinsic Semiconductors

*Apply a voltage across a piece of *Si:*

electron current

and hole current



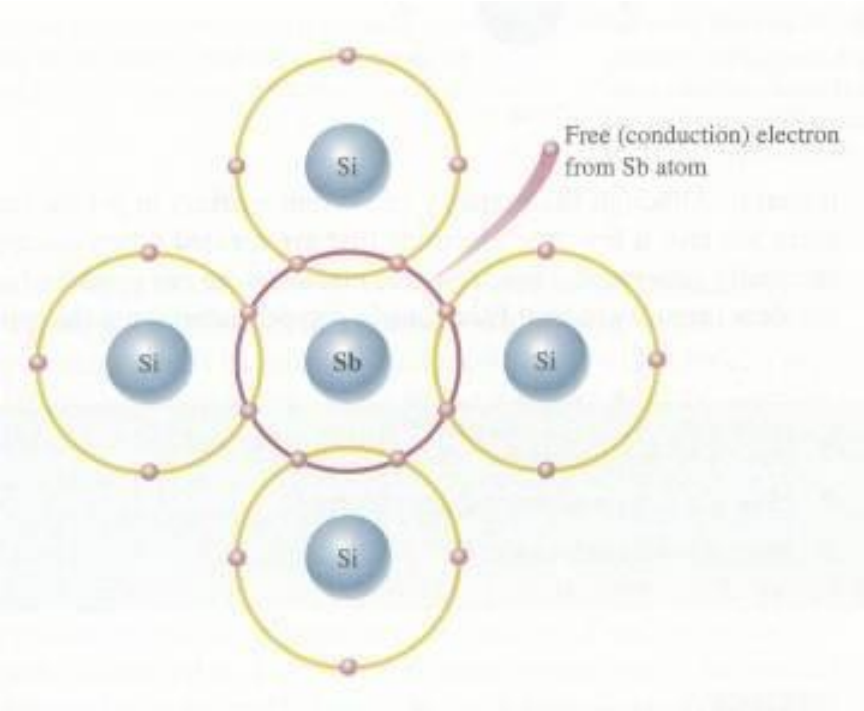


When a valence electron moves left to right to fill a hole while leaving another hole behind, a hole has effectively moved from right to left. Gray arrows indicate effective movement of a hole.

N- and P- Type Semiconductors

* *Doping*: adding of impurities (i.e., dopants) to the intrinsic semi-conductor material.

* *N-type*: adding Group V dopant (or donor) such as As, P, Sb,…



$n \cdot p = constant\ for\ a\ semiconductor$

$For\ \ Si\ \ at\ 300K$

$n \cdot p = n_i^2 = p_i^2 = \left(1.5 \times 10^{10}\right)^2$

$In\ \ n\text{-}type\ material$

$n \cong N_d\ \ the\ donor\ conceration$

$n = N_d >> n_i,\ \ p << p_i$

$We\ call$

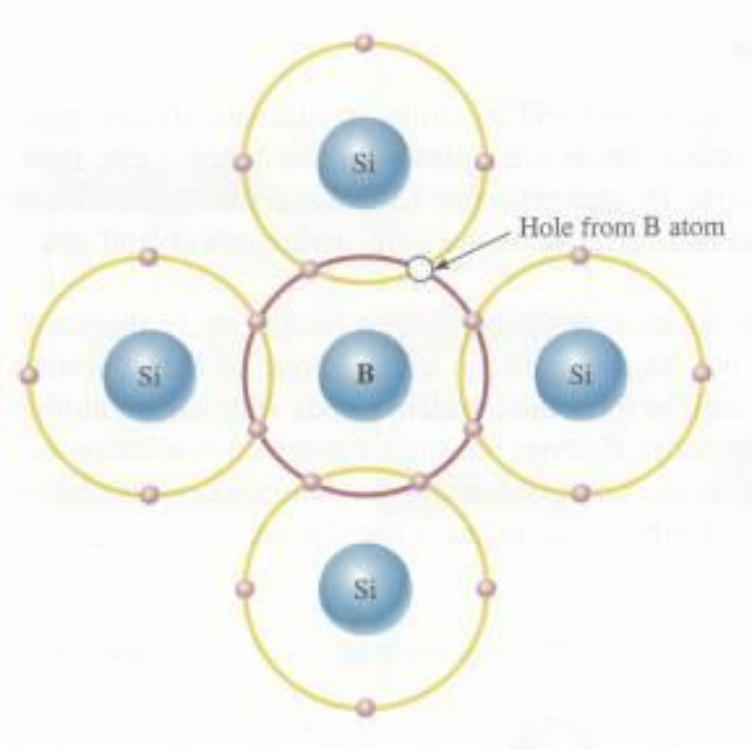
$electron\ the\ major\ charge\ carrier$

$hole\ the\ minor\ cahage\ carrier$

N- and P- Type Semiconductors

* *Doping*: adding of impurities (i.e., dopants) to the intrinsic semi-conductor material.

* *P-type*: adding Group III dopant (or acceptor) such as Al, B, Ga,…



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$$In\ \ p\text{-}type\ material$$

$$p \cong N_a\ \ the\ acceptor\ conceration$$

$$p = N_a >> p_i,\ n << n_i$$

$$We\ call$$

$$hole\ the\ major\ charge\ carrier$$

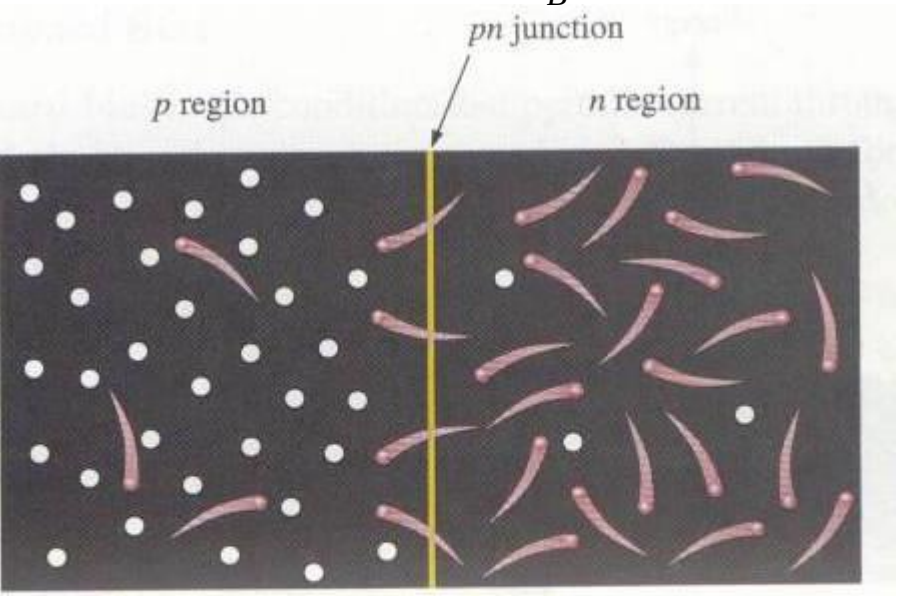
$$electron\ the\ minor\ cahage\ carrier$$

The PN-Junction

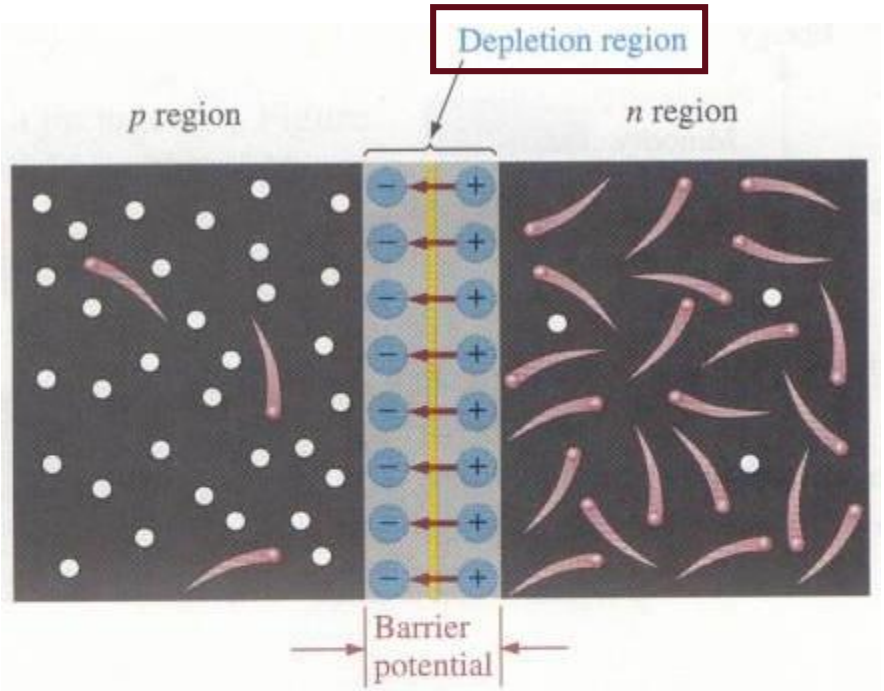
* The interface in-between p-type and n-type material is called a *pn-junction*.

$The\ barrier\ potential\ V_B \cong 0.6 - 0.7V\ \ for\ Si\ and\ 0.3V\ \ for\ Ge$

$at\ 300K:\ \ as\ T \uparrow, V_B \downarrow.$



(a) At the instant of junction formation, free electrons in the *n* region near the *pn* junction begin to diffuse across the junction and fall into holes near the junction in the *p* region.

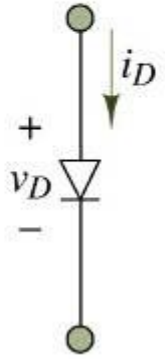


(b) For every electron that diffuses across the junction and combines with a hole, a positive charge is left in the *n* region and a negative charge is created in the *p* region, forming a barrier potential. This action continues until the voltage of the barrier repels further diffusion.

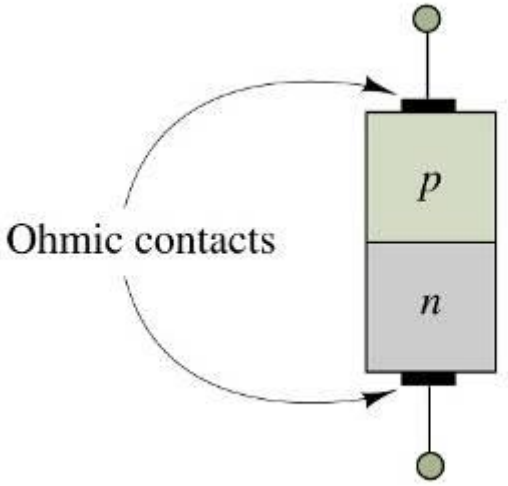
Biasing the PN-Junction

* There is no movement of charge through a PN-junction at equilibrium.
* The PN-junction form a *diode* which allows current in only one direction and prevent the current in the other direction as determined by the *bias*.

The arrow in the circuit symbol for the diode indicates the direction of current flow when the diode is forward-biased.



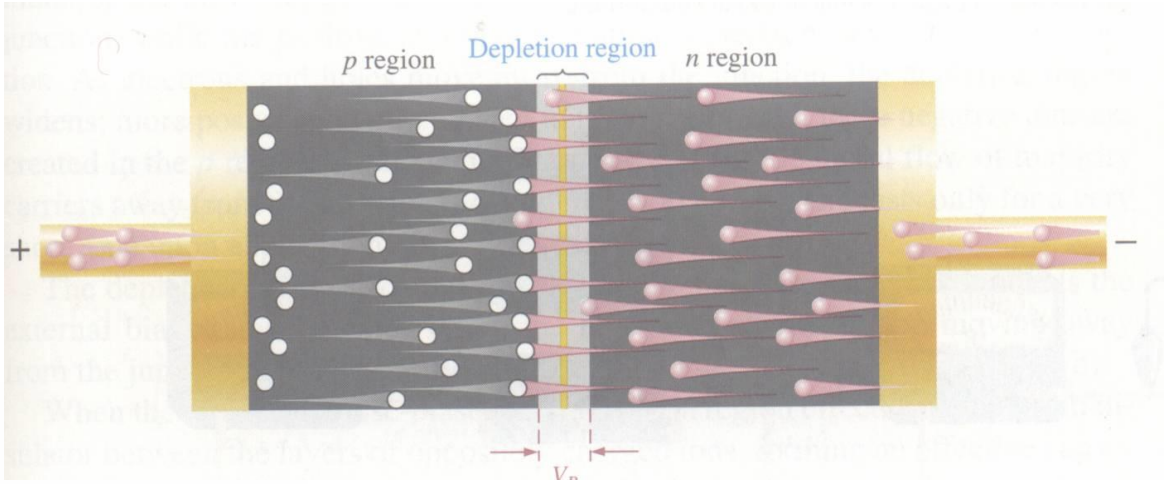
Circuit symbol

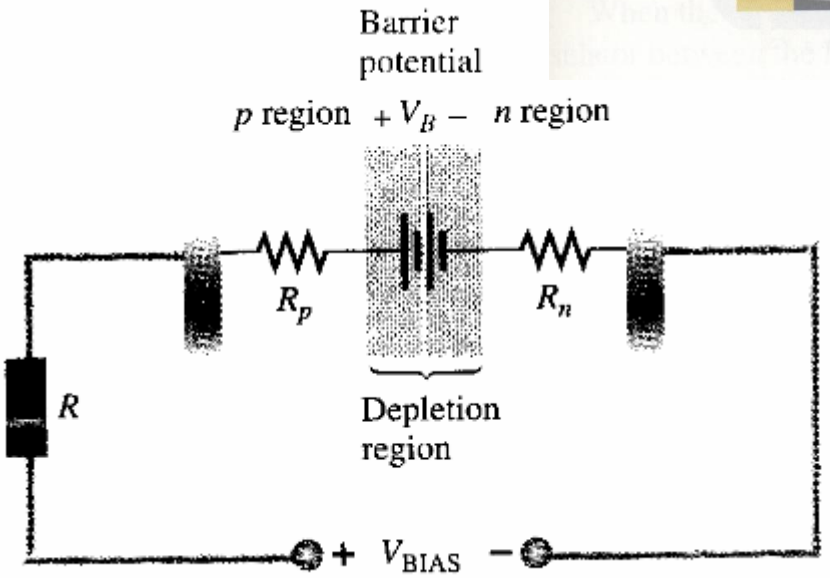


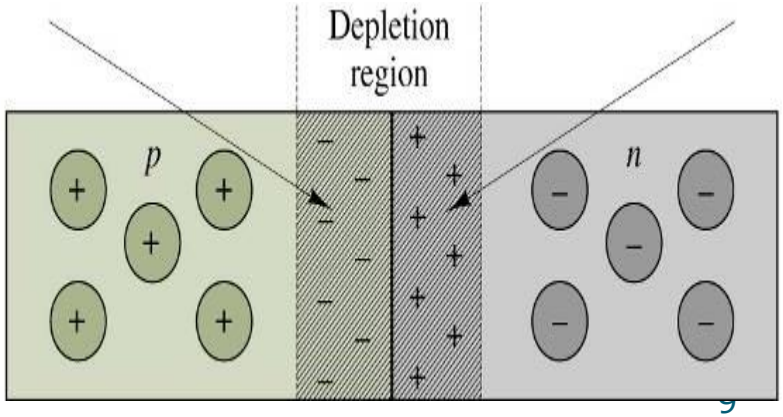
pn junction

Biasing the PN-Junction

*__Forward Bias__: *dc voltage positive terminal connected to the p region and negative to the n region*. It is the condition that permits current through the pn-junction of a diode.

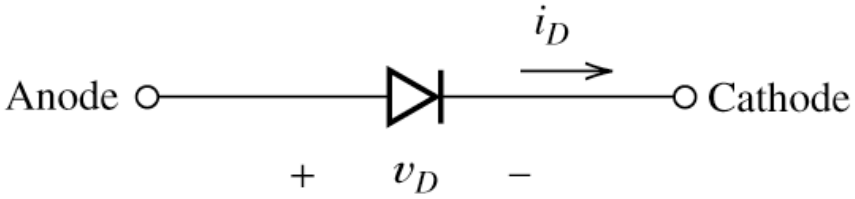


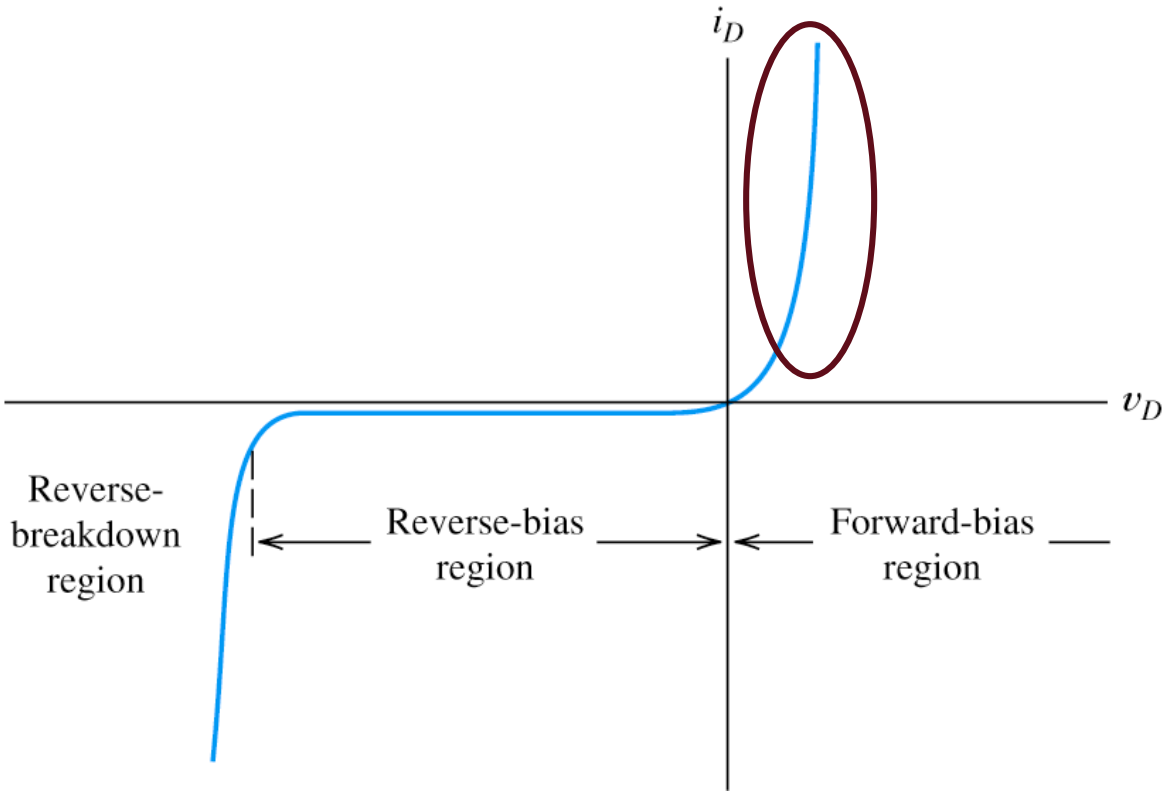




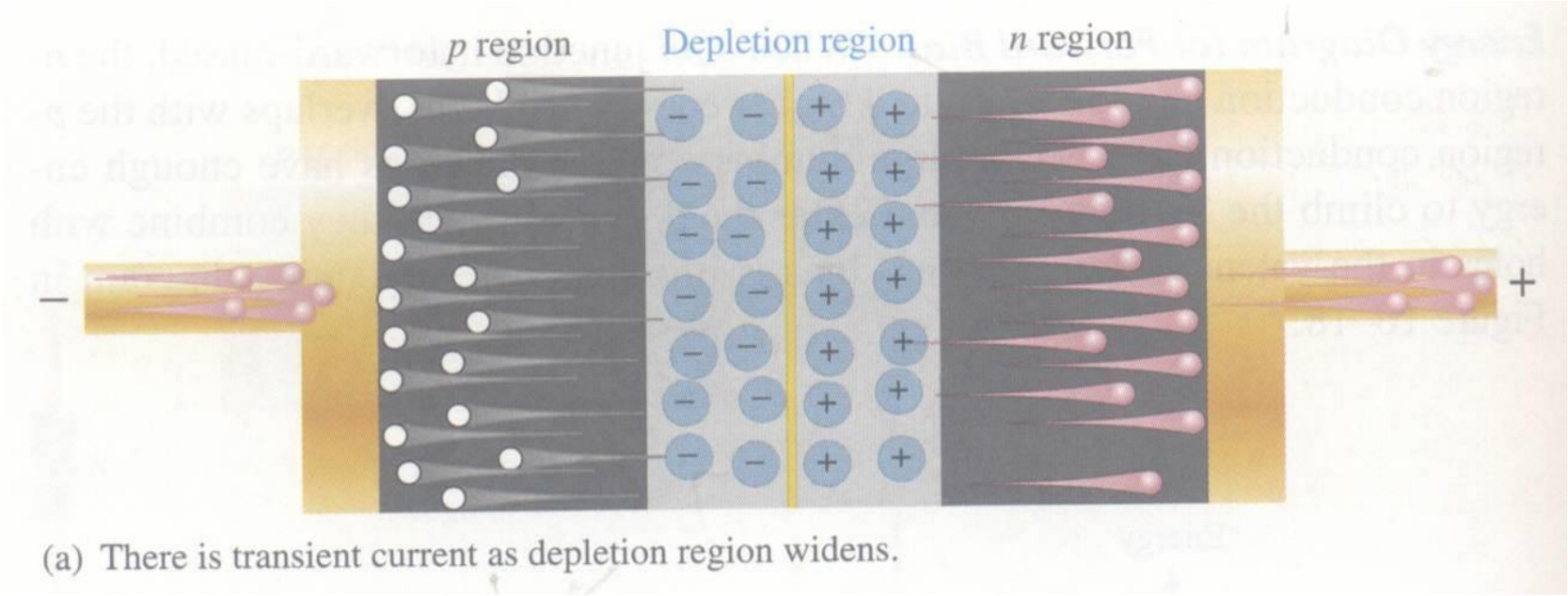
Biasing the PN-Junction

**Forward Bias*:





***Reverse Bias**: *dc voltage negative terminal connected to the p region and positive to the n region*. *Depletion region widens* until its potential difference equals the bias voltage, *majority-carrier current ceases*.

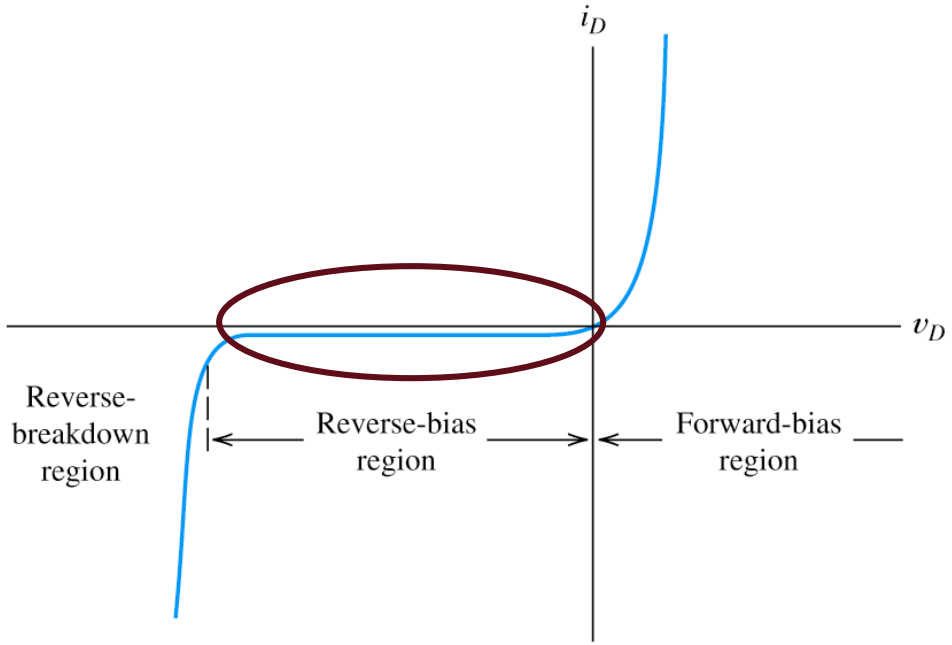


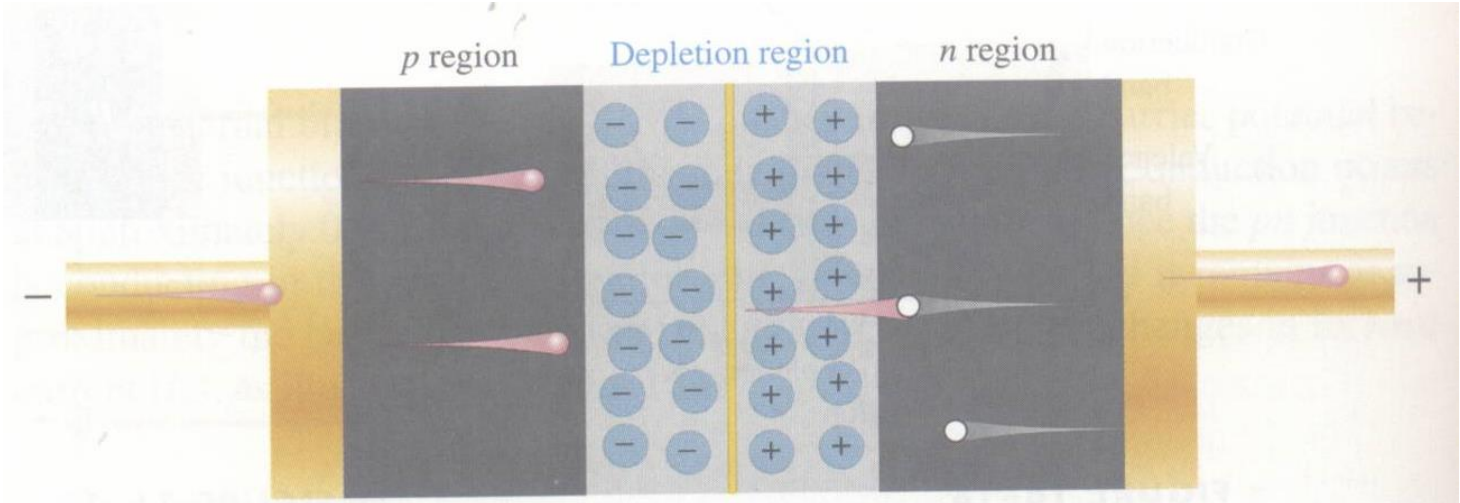
(a) There is transient current as depletion region widens.

*__Reverse Bias__:

majority-carrier current ceases.

* However, there is still a very small current produced by minority carriers.



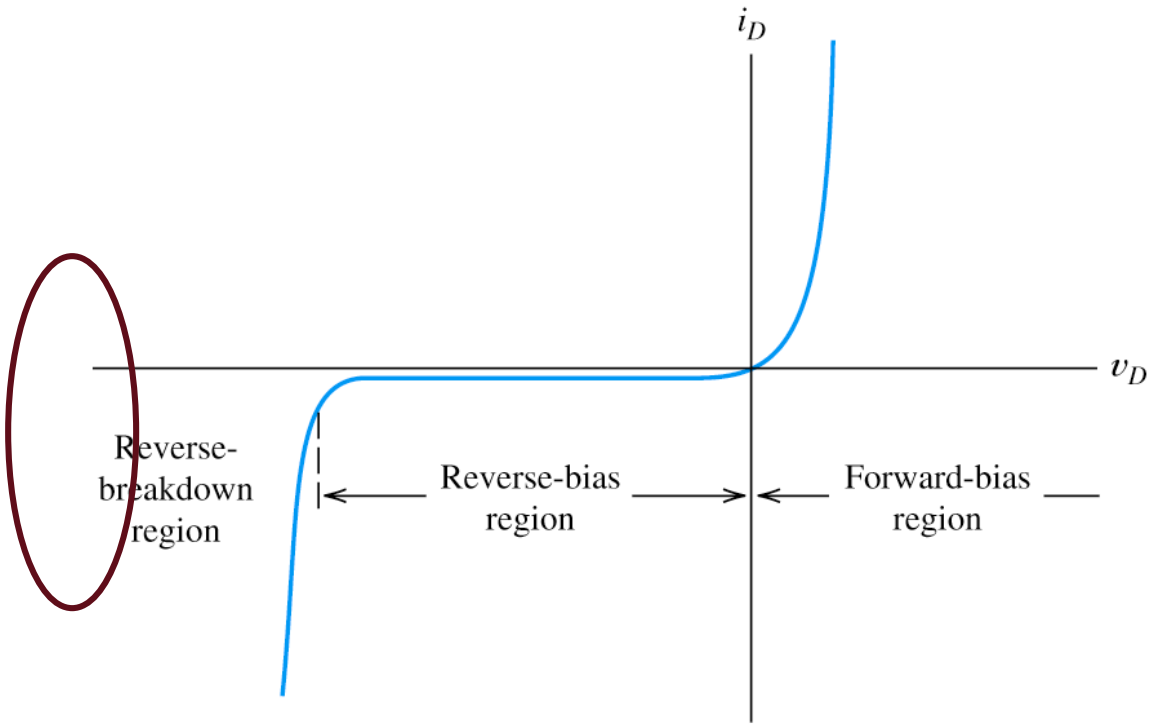


(b) Majority current ceases when barrier potential equals bias voltage. There is an extremely small reverse current due to minority carriers.

Biasing the PN-Junction

* ***Reverse Breakdown:*** As reverse voltage reach certain value, avalanche occurs and generates large current.

Diode Characteristic I-V Curve



(b) Volt–ampere characteristic

Shockley Equation

* The Shockley equation is a theoretical result under certain simplification:

$$i_D = I_s\left[\exp\left(\frac{v_D}{nV_T}\right) - 1\right]$$

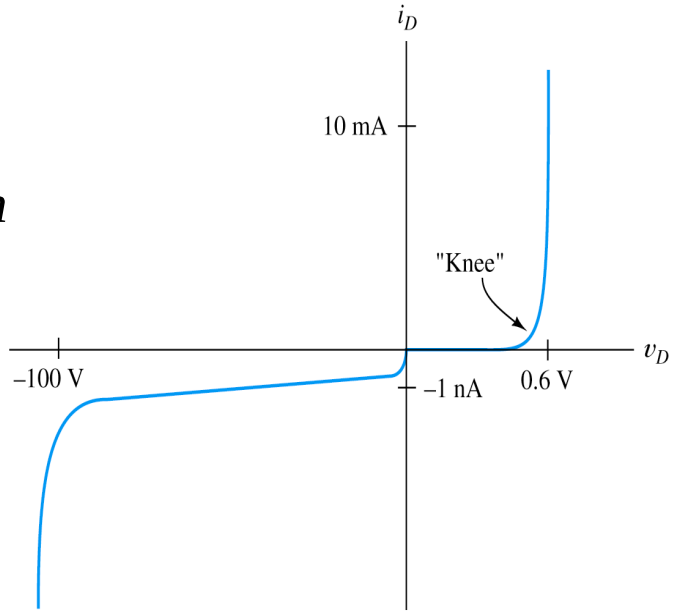
where $I_s \cong 10^{-14}$ A at 300K is the (reverse) saturation current, $n \cong 1$ to 2 is the emission coefficient,

$$V_T = \frac{kT}{q} \cong 0.026\text{V at 300K is the thermal voltage}$$

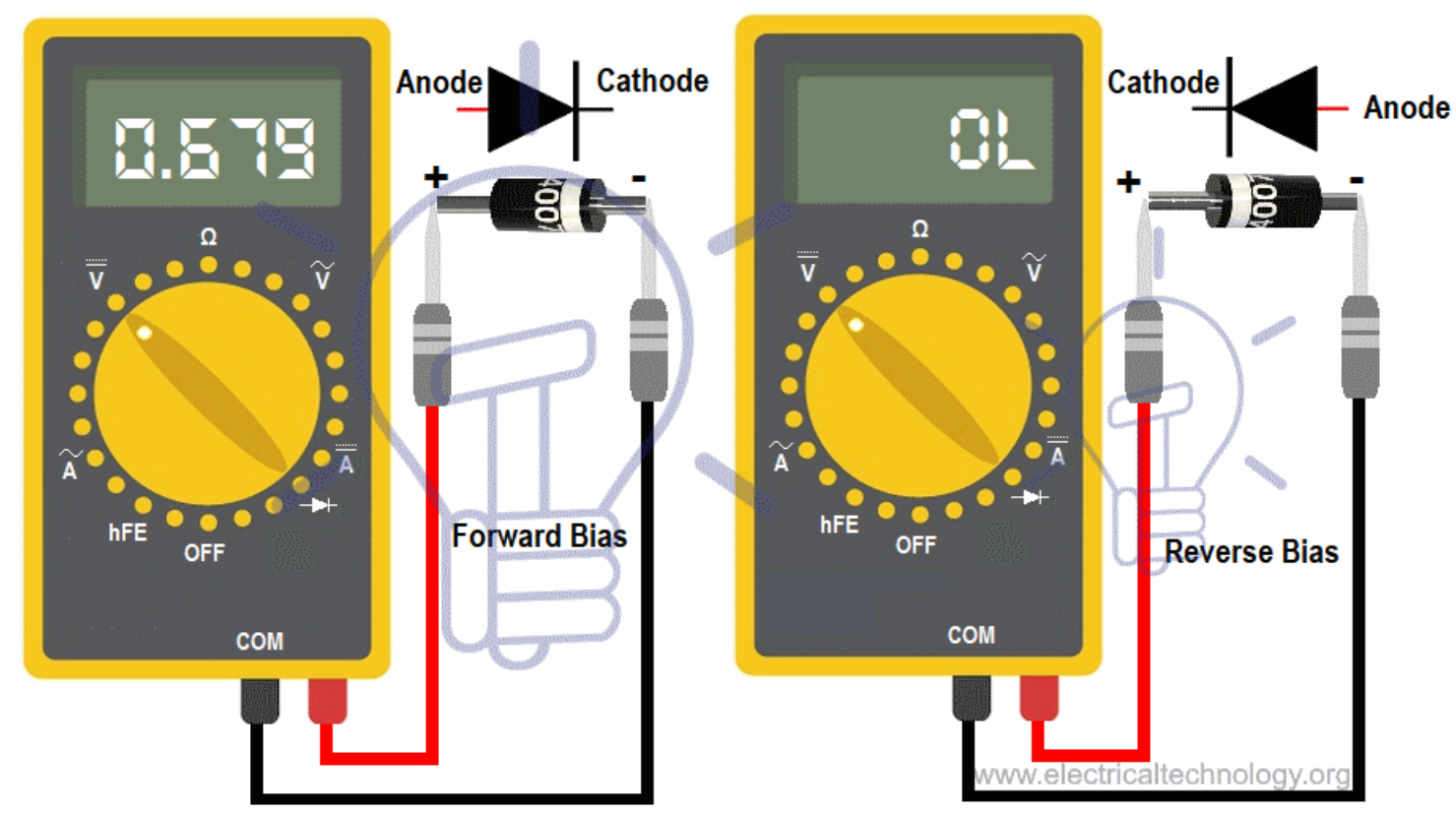
k is the Boltzman's constant, $q = 1.60 \times 10^{-19}$ C

when $v_D \geq\approx 0.1\text{V}$, $i_D \cong I_s \exp\left(\frac{v_D}{nV_T}\right)$

This equation is not applicable when $v_D < 0$



Diode Testing



Ideal-Diode Model

* We may apply "*Ideal-Diode Model*" to simplify the analysis:

(1) in forward direction: *short-circuit assumption*, zero voltage drop;

(2) in reverse direction: *open-circuit assumption*.

* The ideal-diode model can be used when the forward voltage drop and reverse currents are negligible.

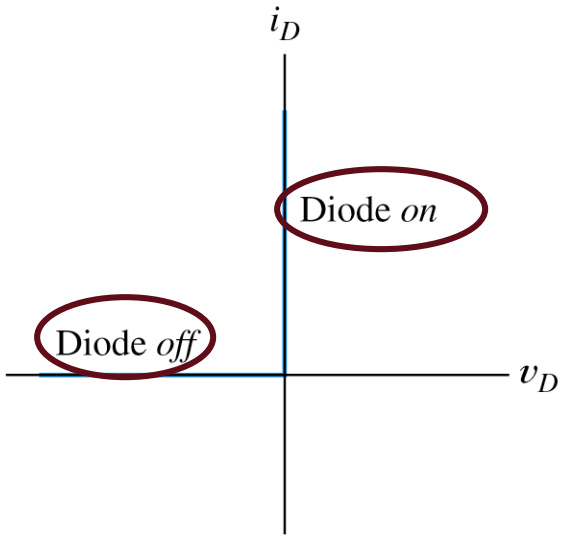


Figure 10.15 Ideal-diode volt–ampere characteristic.

2. Piecewise-Linear Diode Models

Modified Ideal-Diode Model

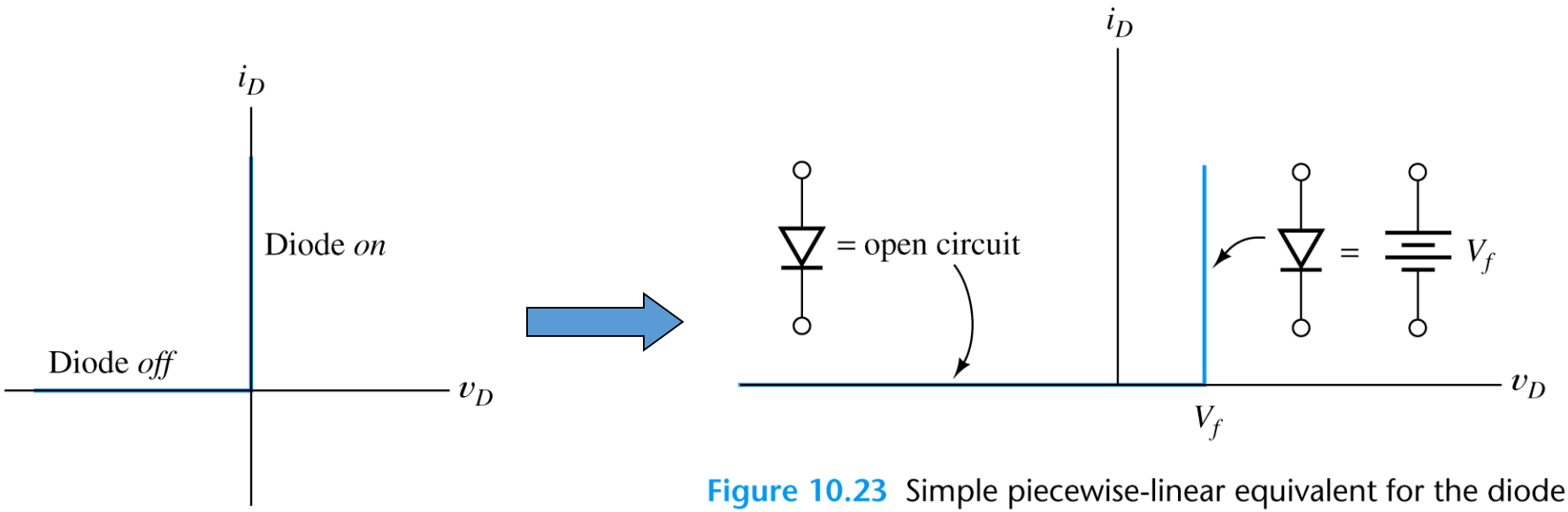


Figure 10.23 Simple piecewise-linear equivalent for the diode.

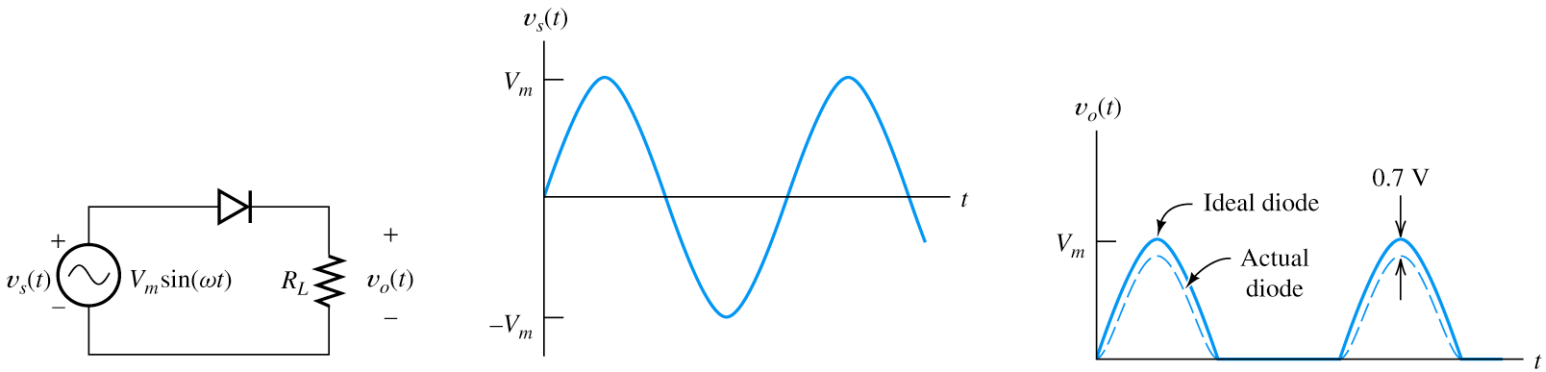
* This modified ideal-diode model is usually accurate enough in most of the circuit analysis.

Application

Rectifier Circuits

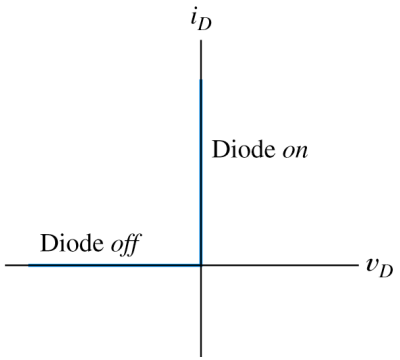
* *Rectifiers* convert ac power to dc power.
* Rectifiers form the basis for electronic power suppliers and battery charging circuits.

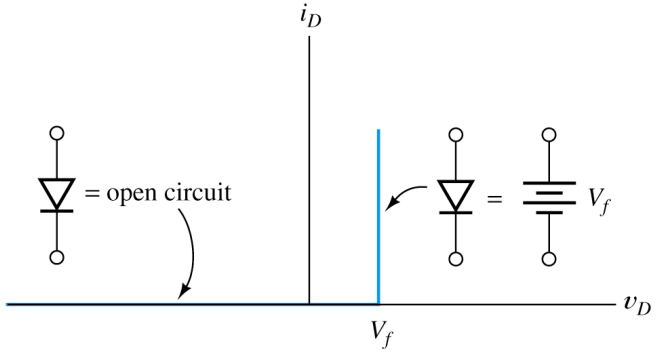
Half-Wave Rectifier



(a) Circuit diagram (b) Source voltage versus time (c) Load voltage versus time

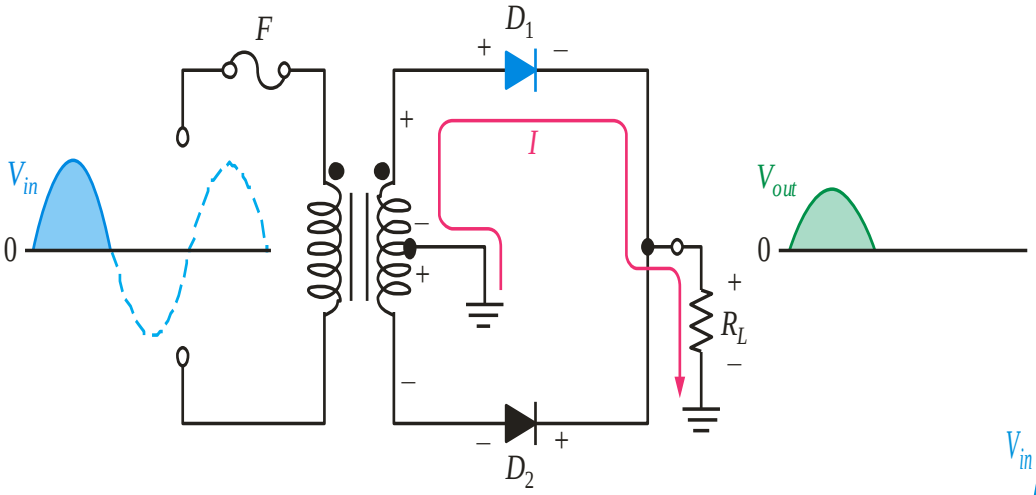
Figure 10.24 Half-wave rectifier with resistive load.





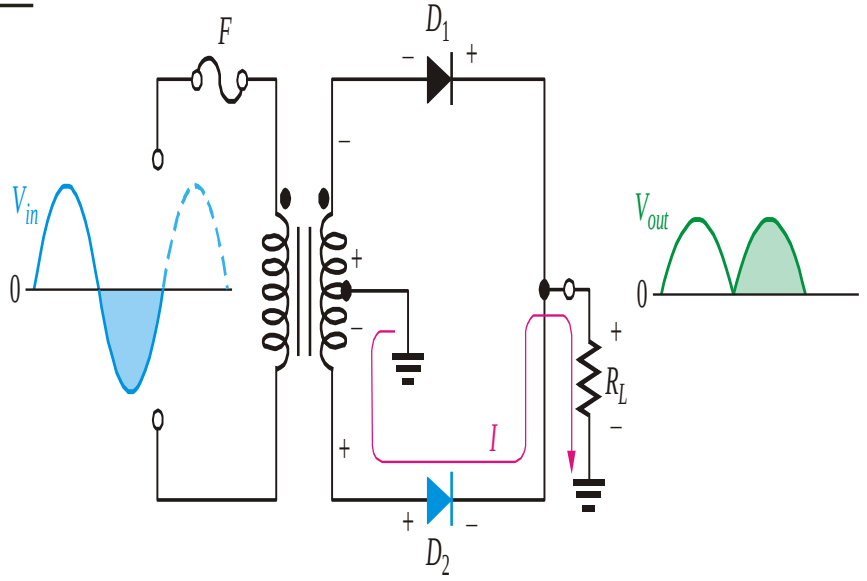
Center-Tapped Full wave rectifiers

- A center-tapped transformer is used with two diodes that conduct on alternating half-cycles.



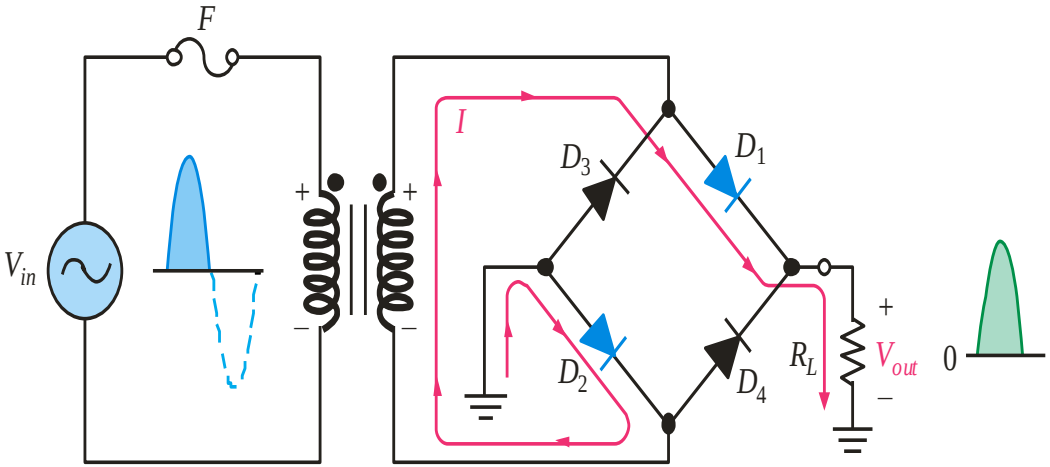
During the positive half-cycle, the upper diode is forward-biased and the lower diode is reverse-biased.

During the negative half-cycle, the lower diode is forward-biased and the upper diode is reverse-biased.



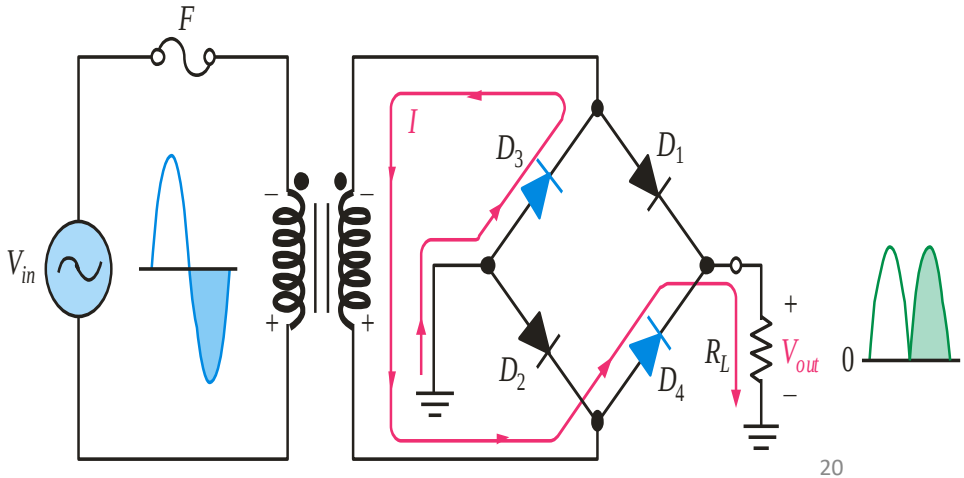
Bridge Full-wave rectifiers

❖The Bridge Full-Wave rectifier uses four diodes connected across the entire secondary as shown.



Conduction path for the positive half-cycle.

Conduction path for the negative half-cycle.



MCQ

The forward voltage drop across a silicon diode is about ……

(a) 0.3 V

(b) 3 V

(C) 7 V

(d) 0.7 V

MCQ

The leakage current in a crystal diode is due to …….

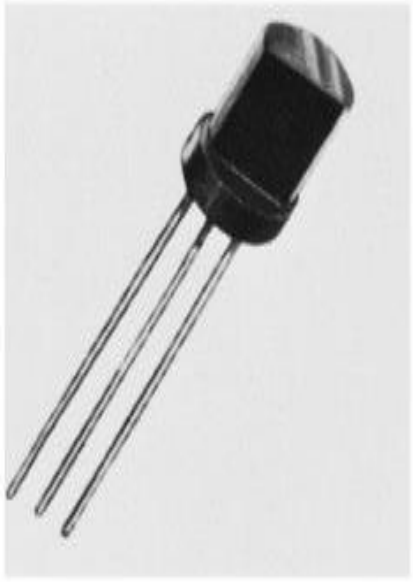
(a) minority carriers

(b) majority carriers

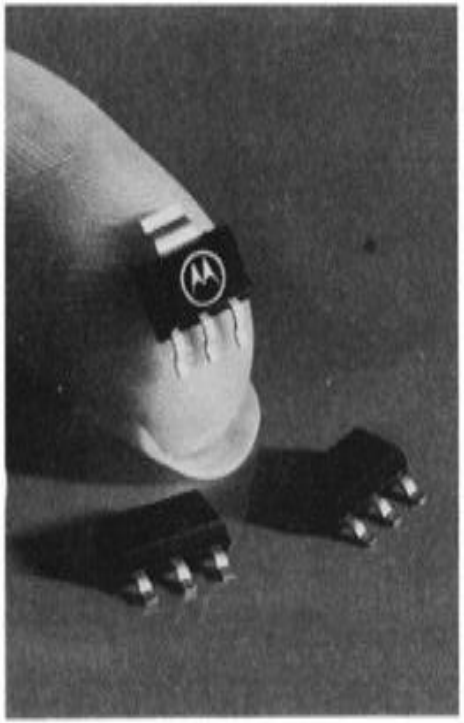
(C)junction capacitance

(d) none of the above

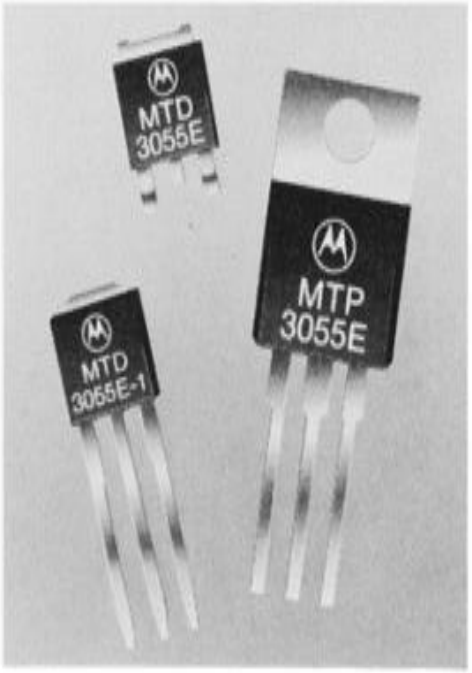
TRANSISTOR -



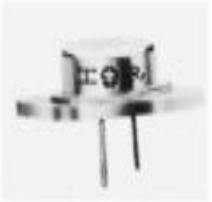
(a)



(b)



(c)



(d)

Introduction

- Beside diodes, the most popular semiconductor devices is transistors. Eg: Bipolar Junction Transistor (BJT)

- If cells are the building blocks of life, transistors are the building blocks of the digital revolution.

Without transistors, technological wonders you use every day -- cell phones, computers -- would be vastly different, if they existed at all.

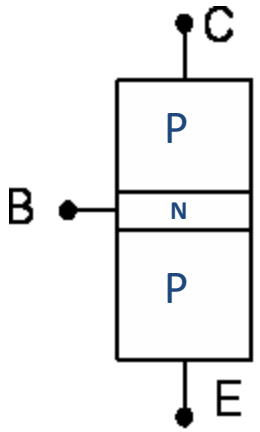
- Transistors are more complex and can be used in many ways Most important feature: can amplify signals and switch

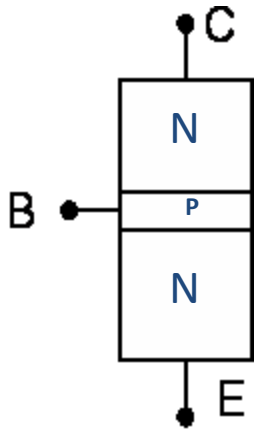
- Amplification can make weak signal strong (make sounds louder and signal levels greater), in general, provide function called Gain

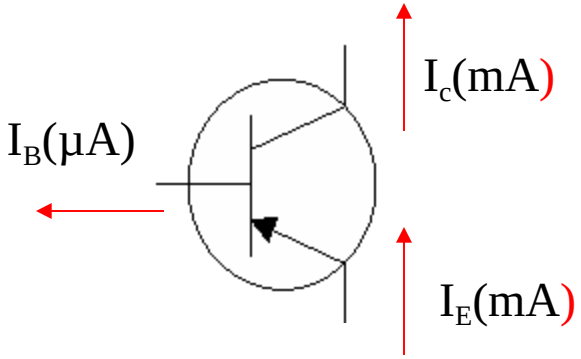
Transistor Structure

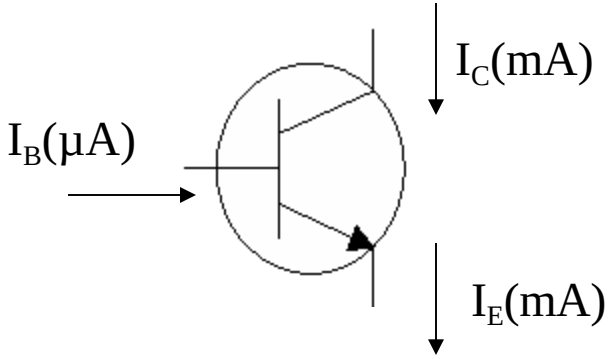
- BJT is bipolar because both holes (+) and electrons (-) will take part in the current flow through the device
  - N-type regions contains free electrons (negative carriers)
  - P-type regions contains free holes (positive carriers)
- Types of BJT
  - NPN transistor
  - PNP transistor
- The transistor regions are:
  - Emitter (E) – send the carriers into the base region and then on to the collector
  - Base (B) – acts as control region. It can allow none, some or many carriers to flow
  - Collector (C) – collects the carriers

PNP and NPN transistor structure



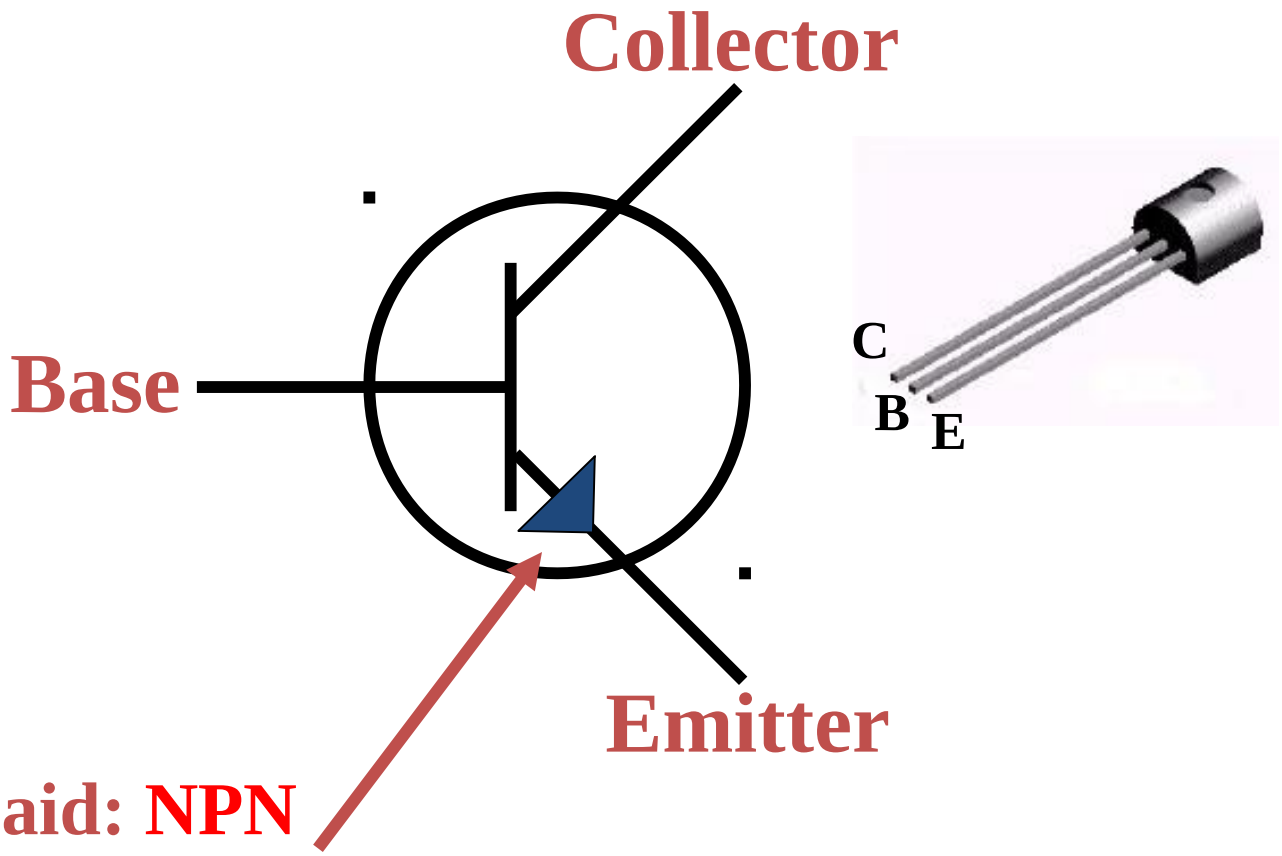






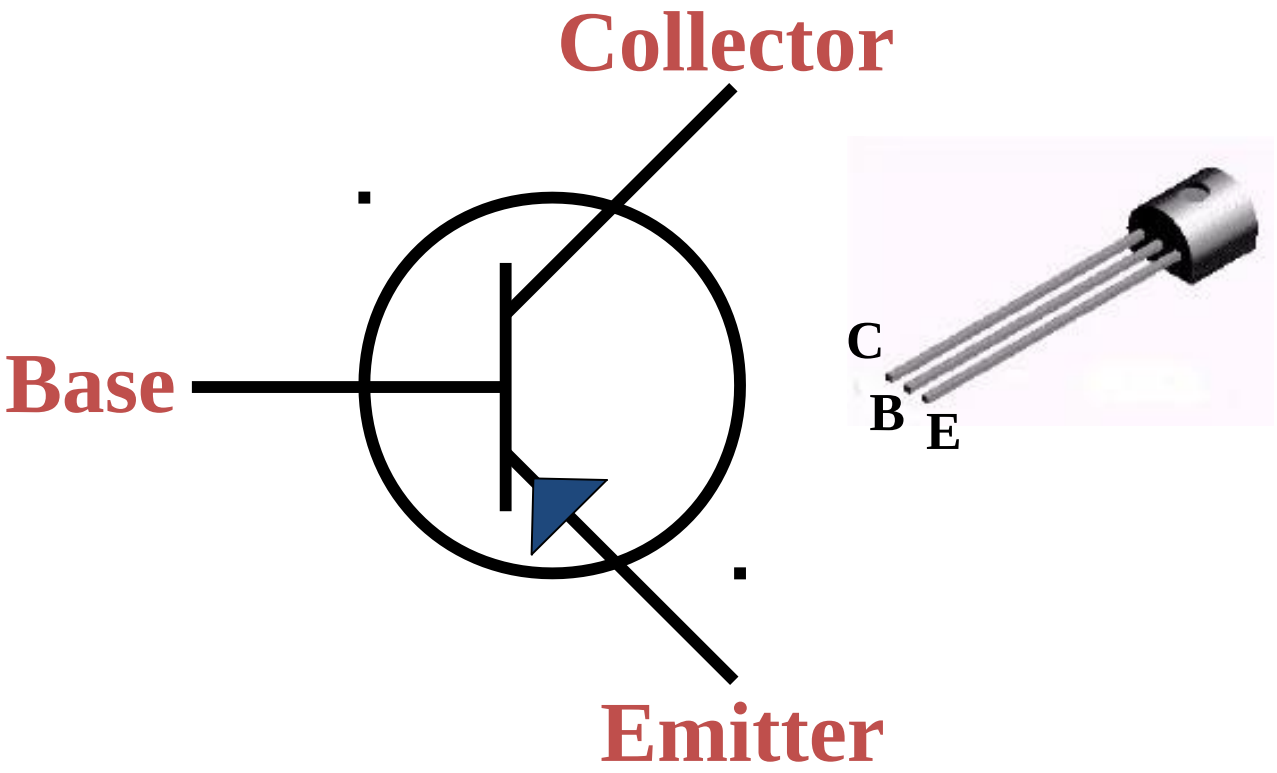
Arrow shows the current flows

NPN Schematic Symbol



Memory aid: **NPN** means **N**ot **P**ointing i**N**.

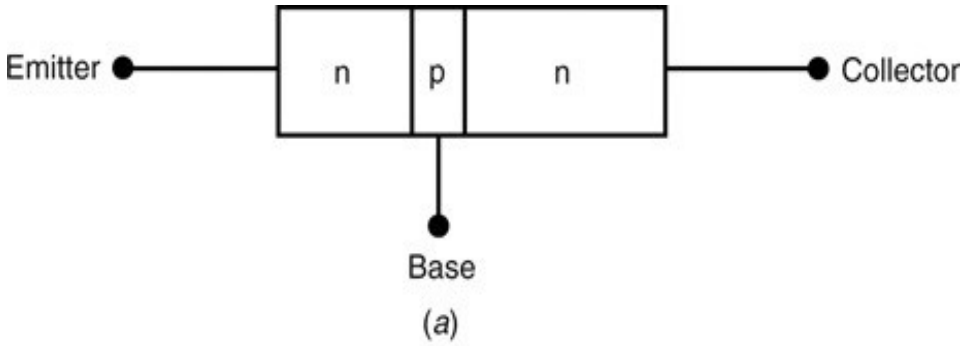
PNP Schematic Symbol



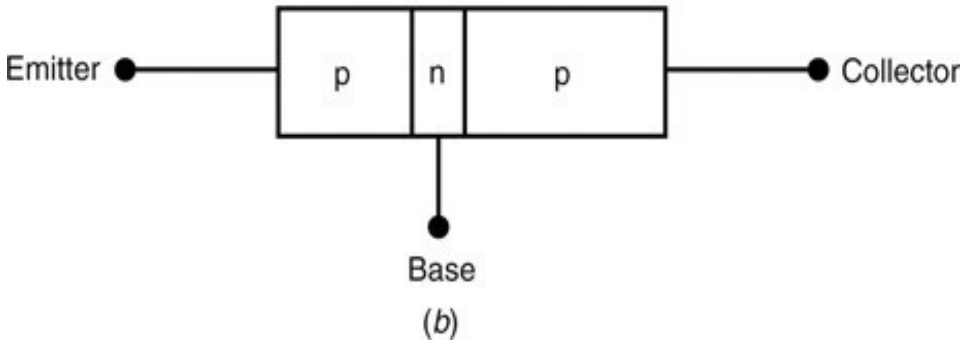
Memory aid: NPN
means Pointing iN Properly.

Transistor Construction

- **A transistor has three doped regions.**
- **For both types, the base is a narrow region sandwiched between the larger collector and emitter regions.**



(*a*)



(*b*)

▪**The emitter region is heavily doped and its job is to emit carriers into the base.**

▪**The base region is very thin and lightly doped.**

▪**Most of the current carriers injected into the base pass on to the collector.**

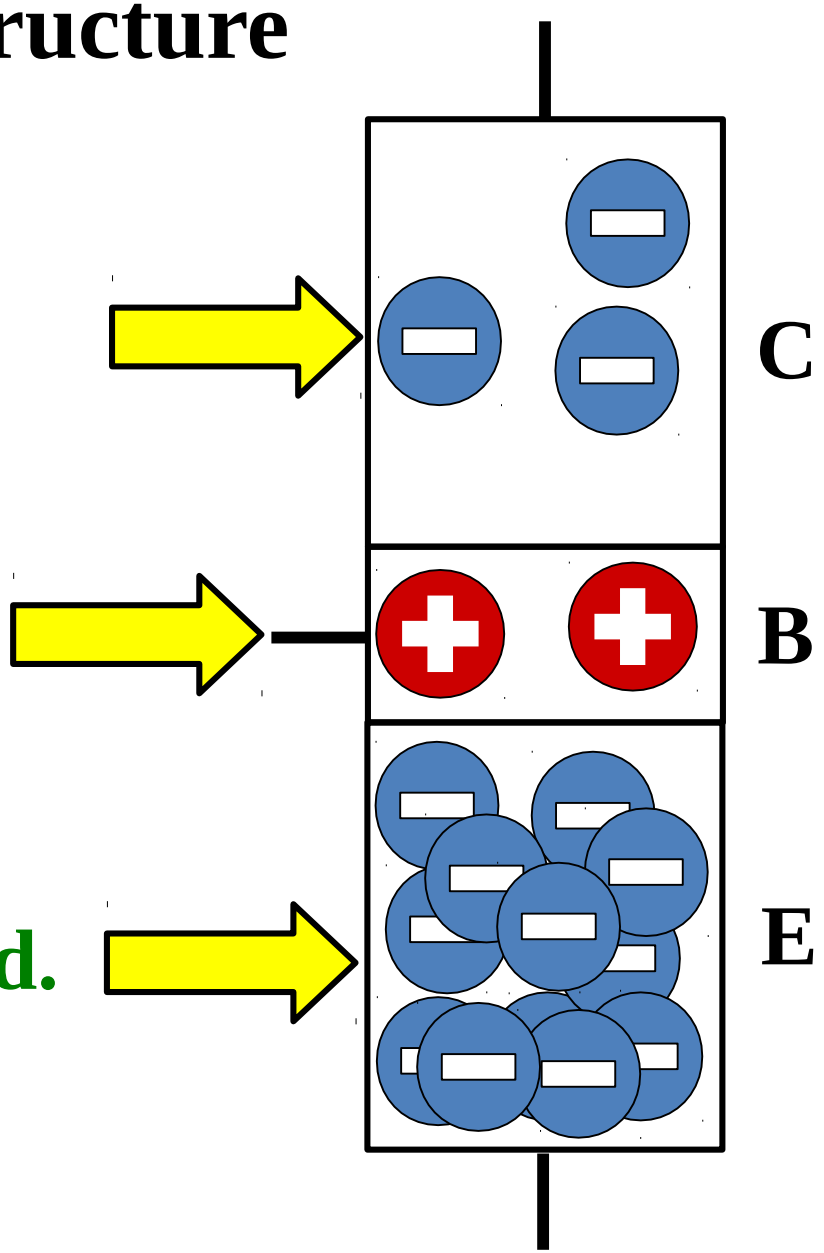
▪**The collector region is moderately doped and is the largest of all three regions.**

NPN Transistor Structure

The collector is Moderately doped.

The base is thin and is lightly doped.

The emitter is heavily doped.



Transistor configuration

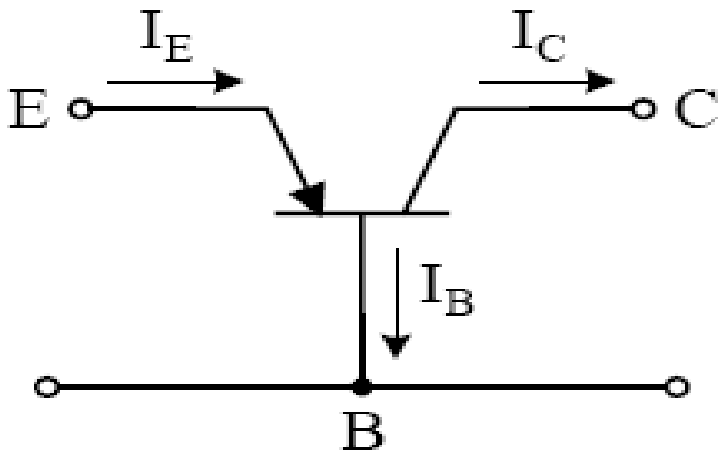
Transistor configuration –is a connection of transistor to get variety operation.

3 types of configuration:

- *Common Base*
- *Common Emitter*
- *Common Collector*

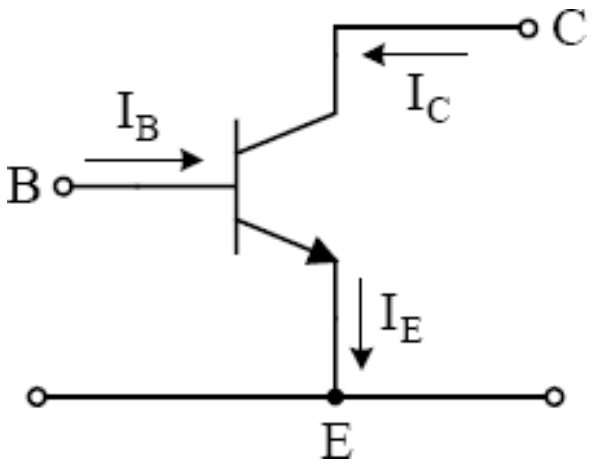
Common-Base Configuration

- Base terminal is a common point for input and output.
- Input – EB
- Output – CB
- Not applicable as an amplifier because the relation between input current gain (I_E) and output current gain (I_C) is approximately 1



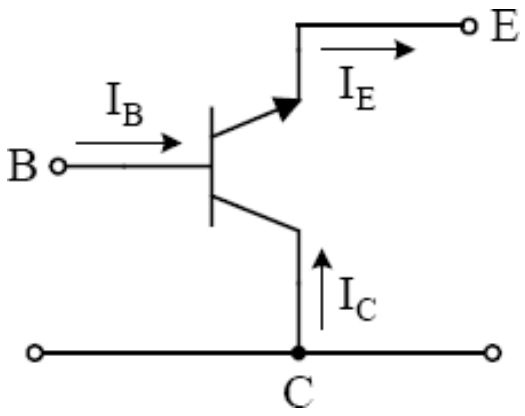
Common-Emitter Configuration

- Emitter terminal is common for input and output circuit
- Input – BE
- Output – CE
- Mostly applied in practical amplifier circuits, since it provides good voltage, current and power gain



Common-Collector Configuration

- The input signal is applied to the base terminal and the output is taken from the emitter terminal.
- Collector terminal is common to the input and output of the circuit
- Input – BC
- Output – EC

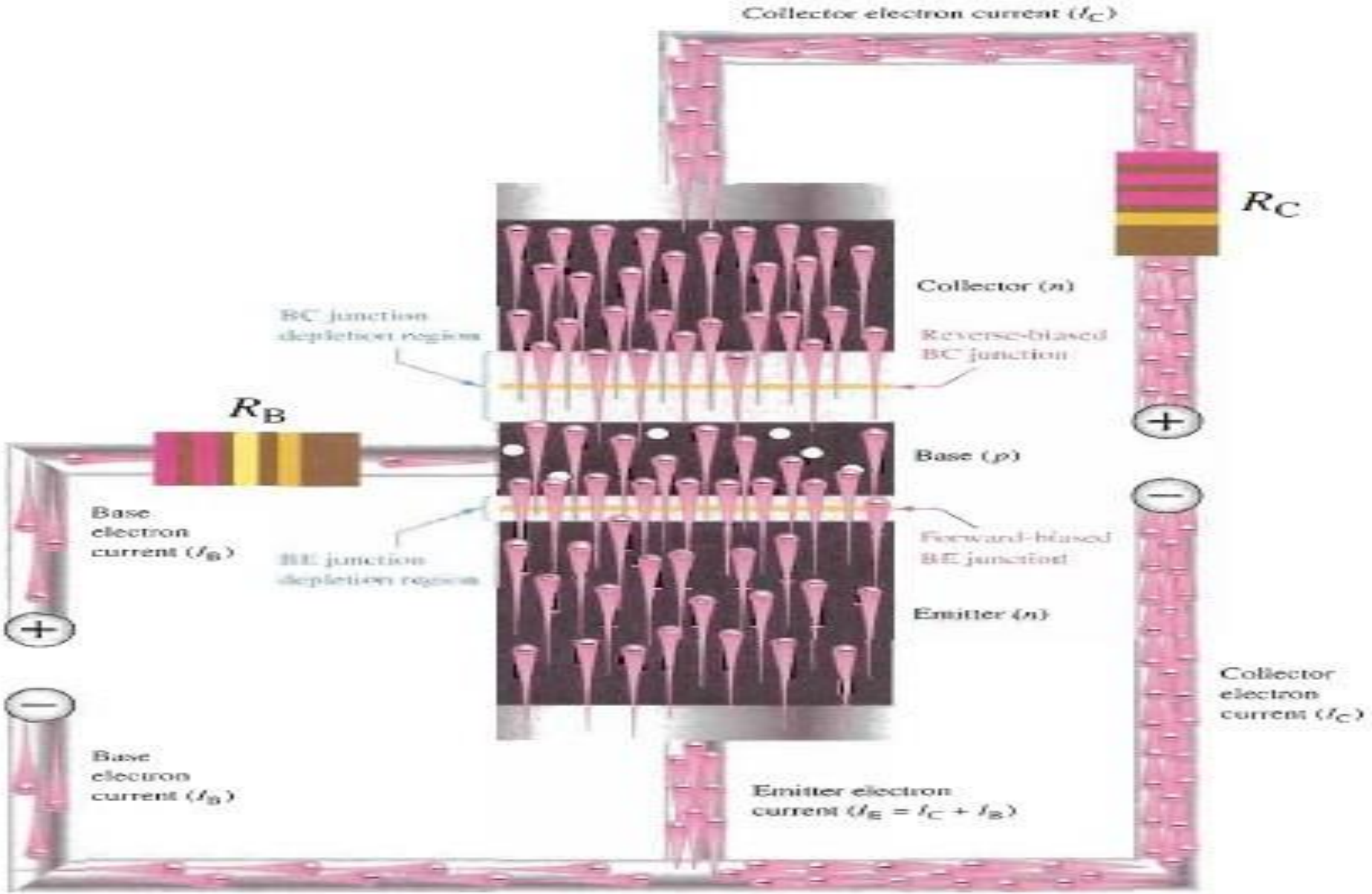


Current Relationships

- Relations between I_C and I_E:
  - $\alpha = \frac{I_C}{I_E}$
- Value of α usually 0.9998 to 0.9999, $\alpha \approx 1$
- Relations between I_C and I_B:
  - $I_C = \beta I_B$
- Value of β usually in range of 50 to 400
- The equation, $I_E = I_C + I_B$ can also written in β
  - $I_C = \beta I_B$
  - $I_E = \beta I_B + I_B \Rightarrow I_E = (\beta + 1) I_B$
- The current gain factor , α and β is:

$$\alpha = \frac{\beta}{\beta + 1} \quad @ \quad \beta = \frac{\alpha}{\alpha - 1}$$

Transistor operation

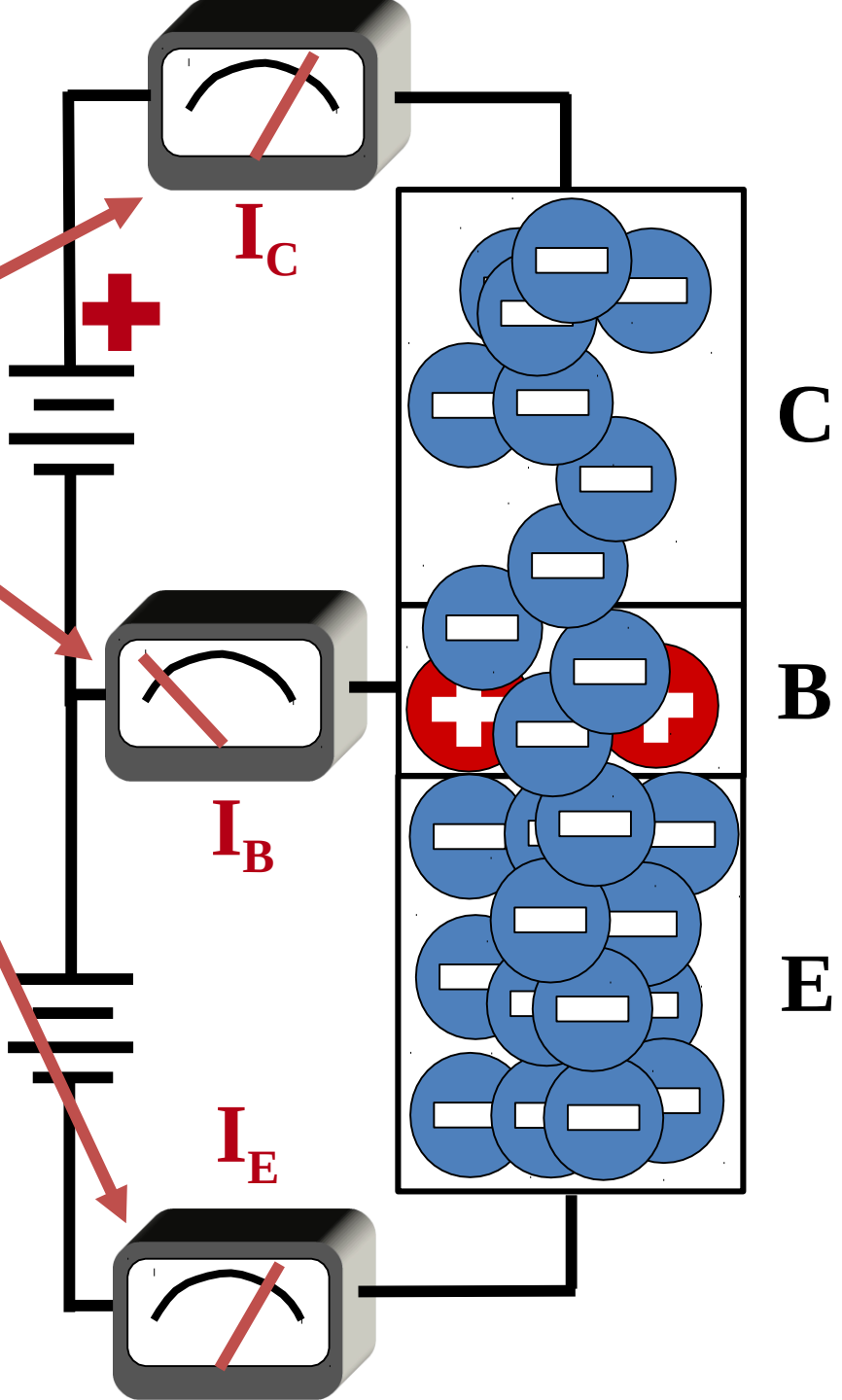


NPN Transistor Bias

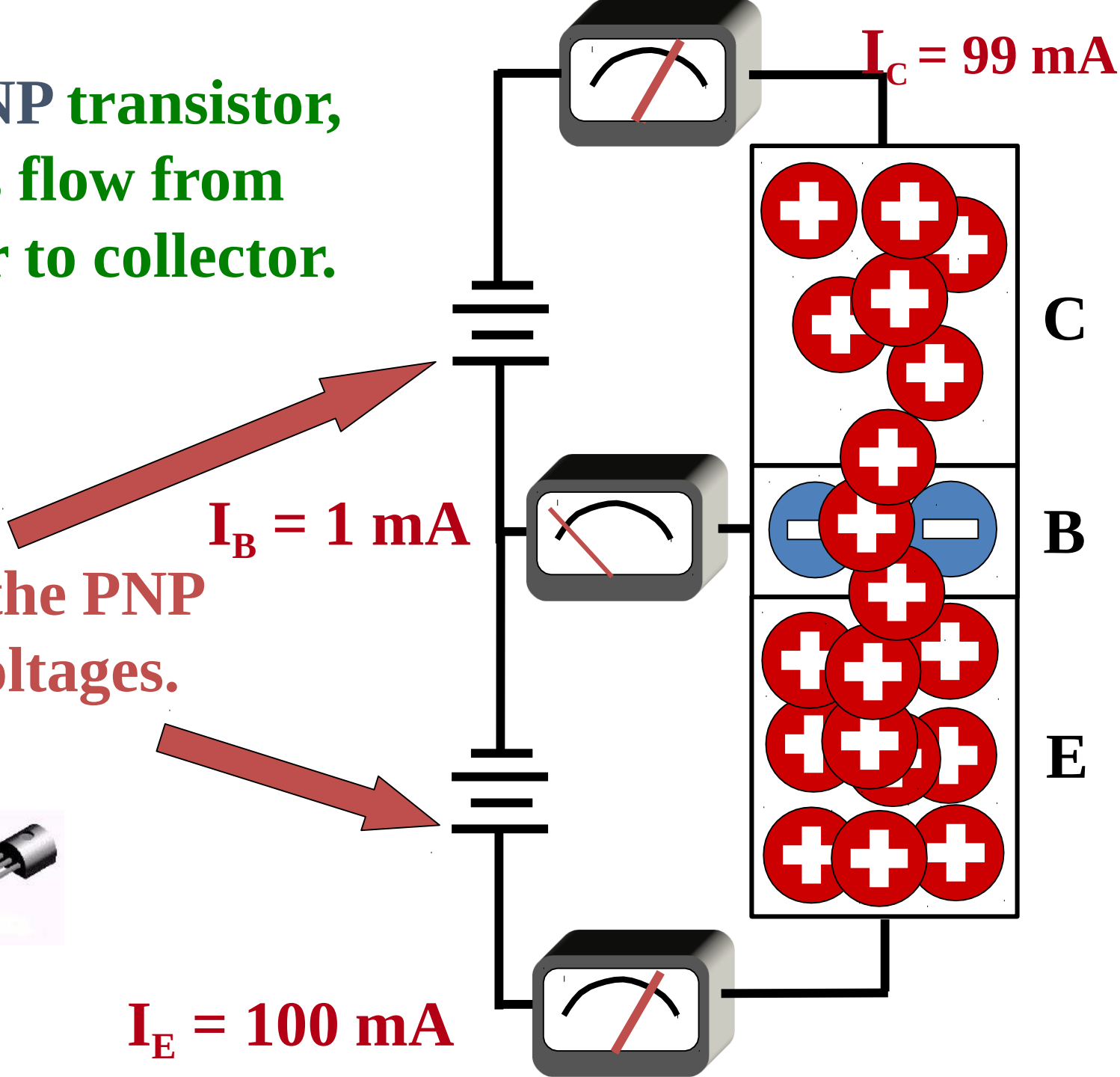
Current flows everywhere.

When both junctions are biased....

Note that I_B is smaller than I_E or I_C.



In a PNP transistor, holes flow from emitter to collector.



Notice the PNP bias voltages.

MCQ

A transistor has ……

1.one pn junction
2.two pn junctions
3.three pn junctions
4.four pn junctions

MCQ

- **The number of depletion layers in a transistor is ……**

(a) Four

(b) Three

(c) One

(d) two

MCQ

- **The element that has the biggest size in a transistor is ……..**

(a) Collector

(b) Base

(c) Emitter

(d) collector-base-junction

MCQ

- **In a npn transistor, ……. are the minority carriers**

(a) free electrons

(b) Holes

(c) donor ions

(d) acceptor ions

MCQ

- **The emitter of a transistor is …… doped**

(a) Lightly
(b) Heavily
(c) Moderately
(d) none of the above

MCQ

- **In a transistor …….**

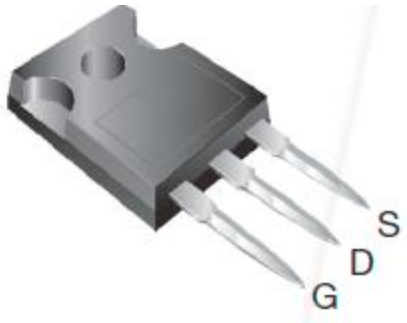
(a) $I_C = I_E + I_B$

(b) $I_B = I_C + I_E$

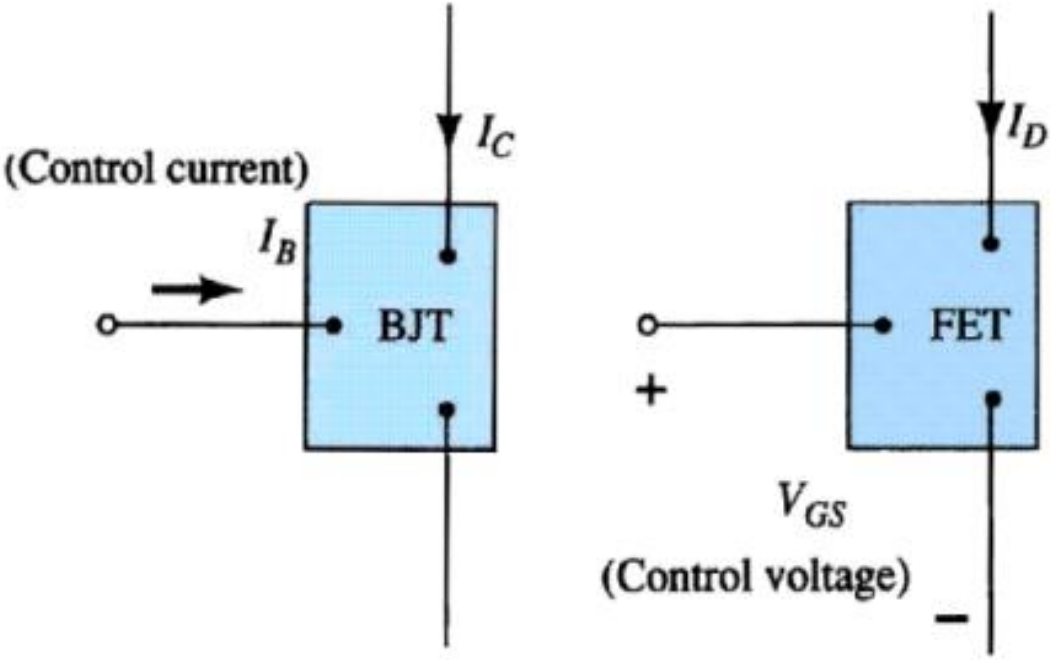
(c) $I_E = I_C - I_B$

(d) $I_E = I_C + I_B$

MOSFET’s (metal–oxide–semiconductor field-effect transistor)



Current Controlled vs Voltage Controlled Devices

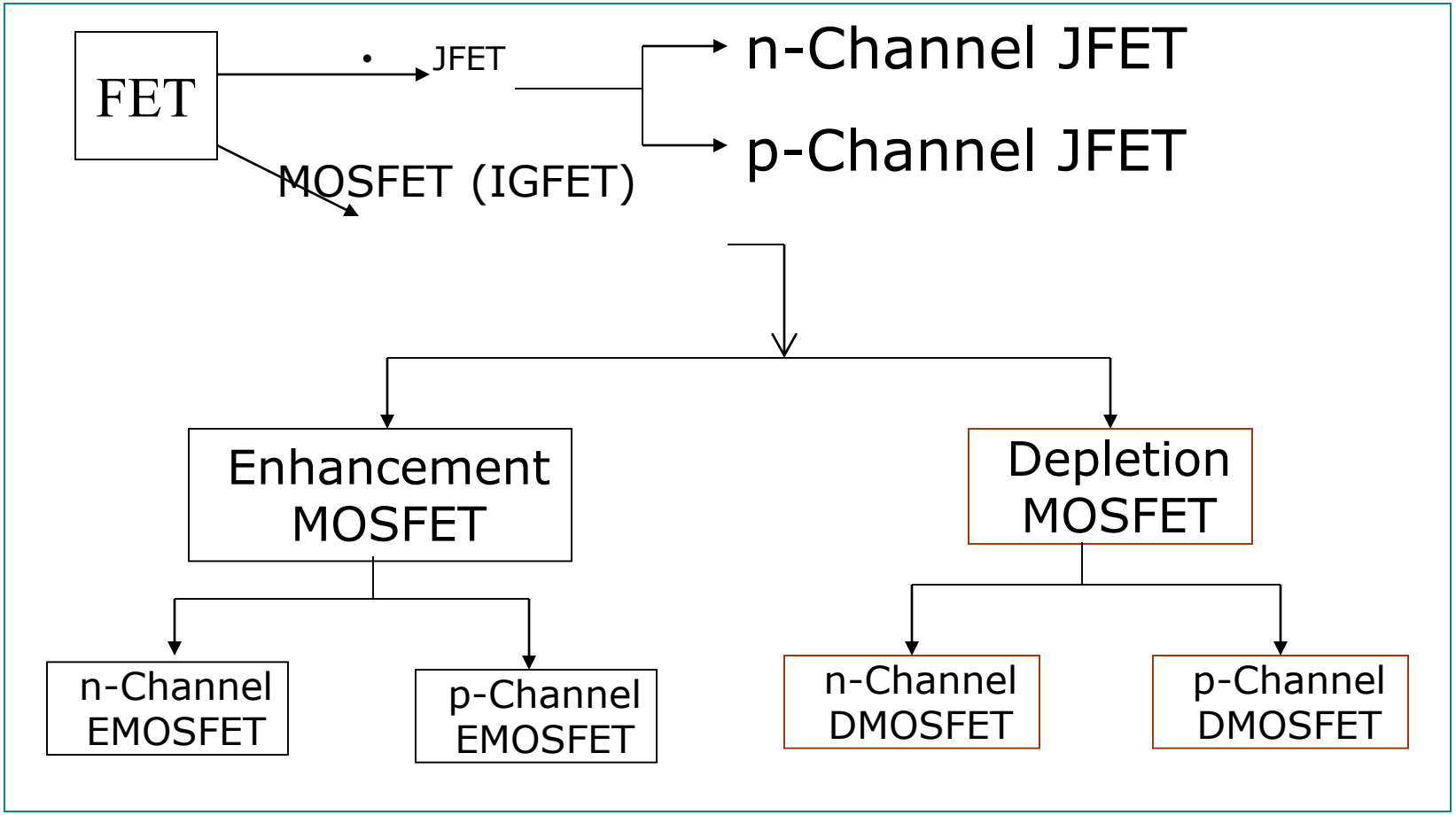


FET (Field Effect Transistor)

Few important advantages of FET over conventional Transistors

1. Unipolar device i. e. operation depends on only one type of charge carriers (*h* or *e)*
2. Voltage controlled Device (gate voltage controls drain current)
3. Very high input impedance ($\approx 10^9$-$10^{12}\,\Omega$)
4. Low Voltage Low Current Operation is possible (Low-power consumption)
5. Less Noisy as Compared to BJT
6. Very small in size, occupies very small space in Ics
7. Low voltage low current operation is possible in MOSFETS

Types of Field Effect Transistors (The Classification)

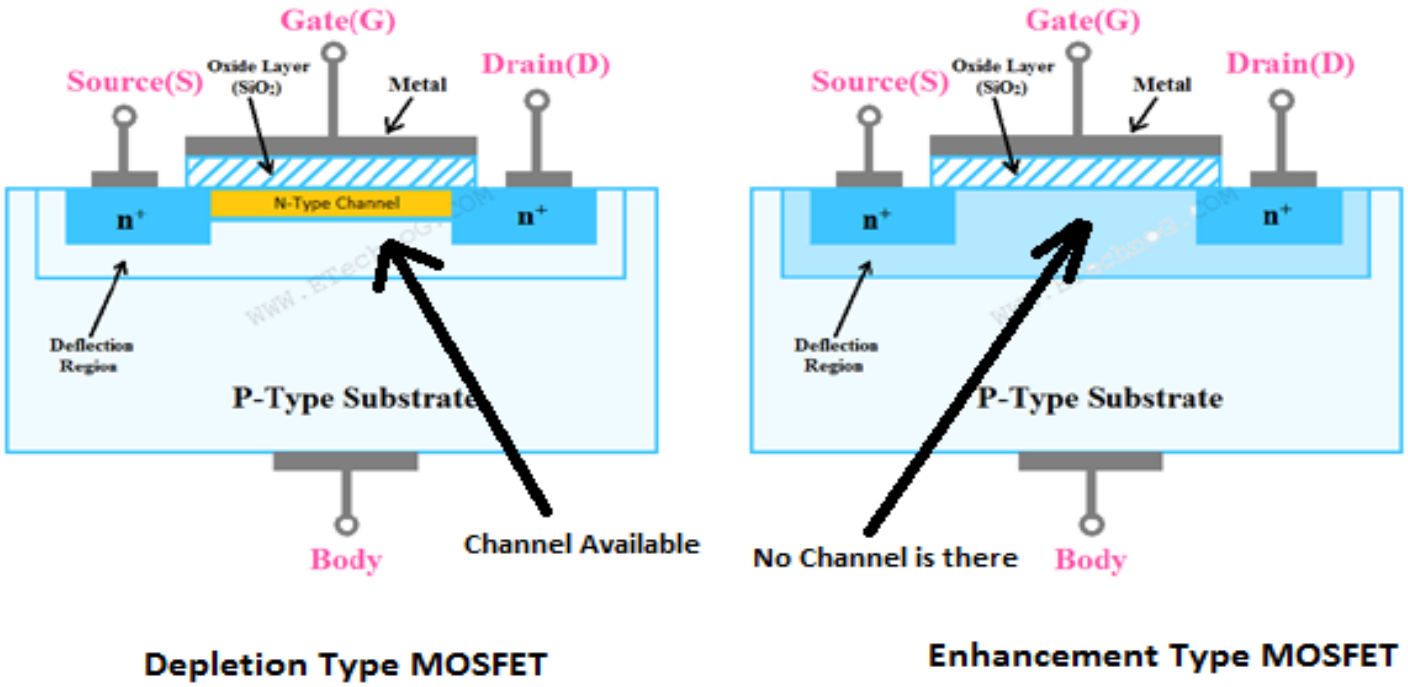


MOSFETs

MOSFETs have characteristics similar to JFETs and additional characteristics that make them very useful.

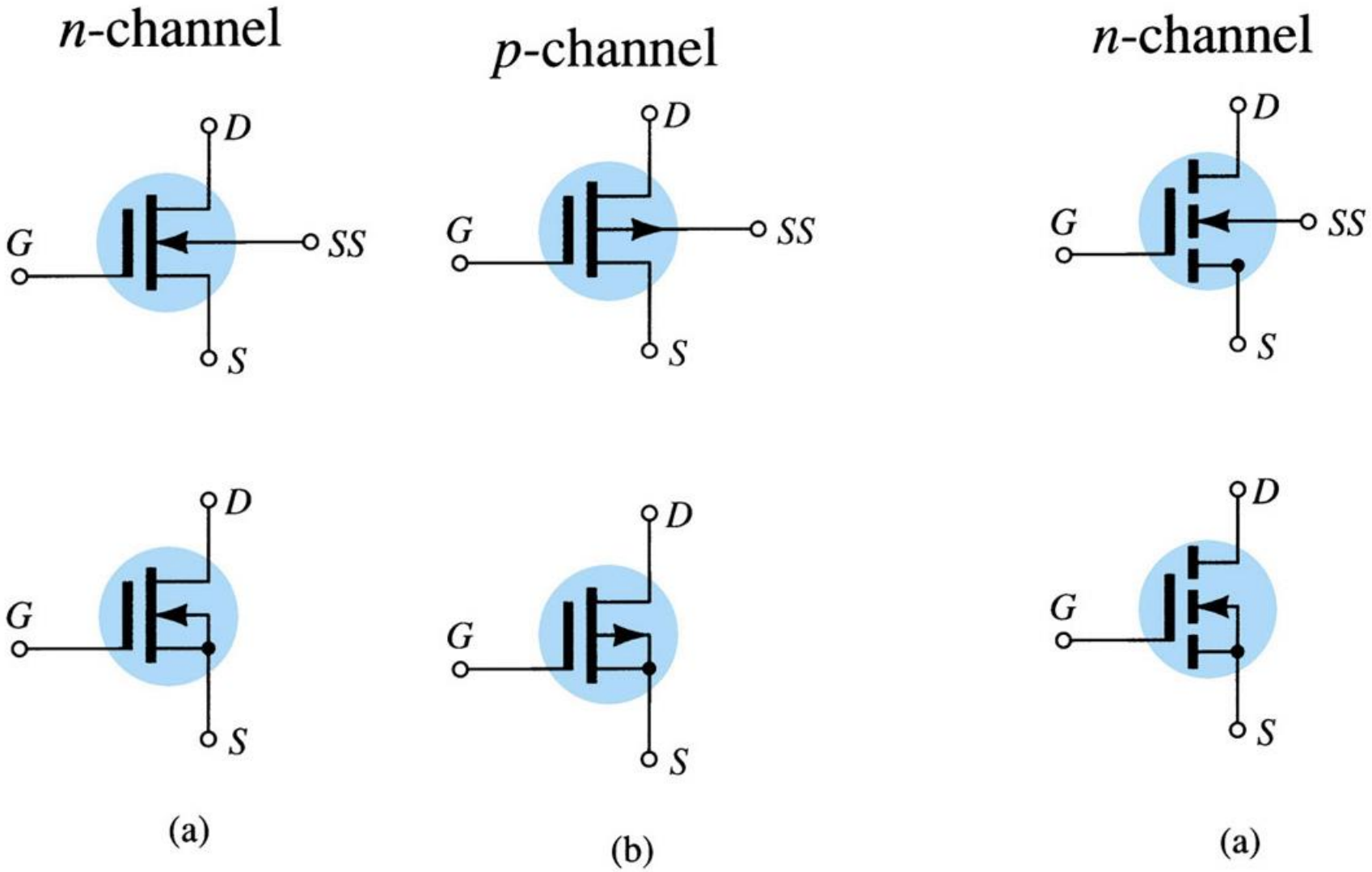
There are 2 types of MOSFET's:

- Depletion mode MOSFET (D-MOSFET)
- Enhancement Mode MOSFET (E-MOSFET)

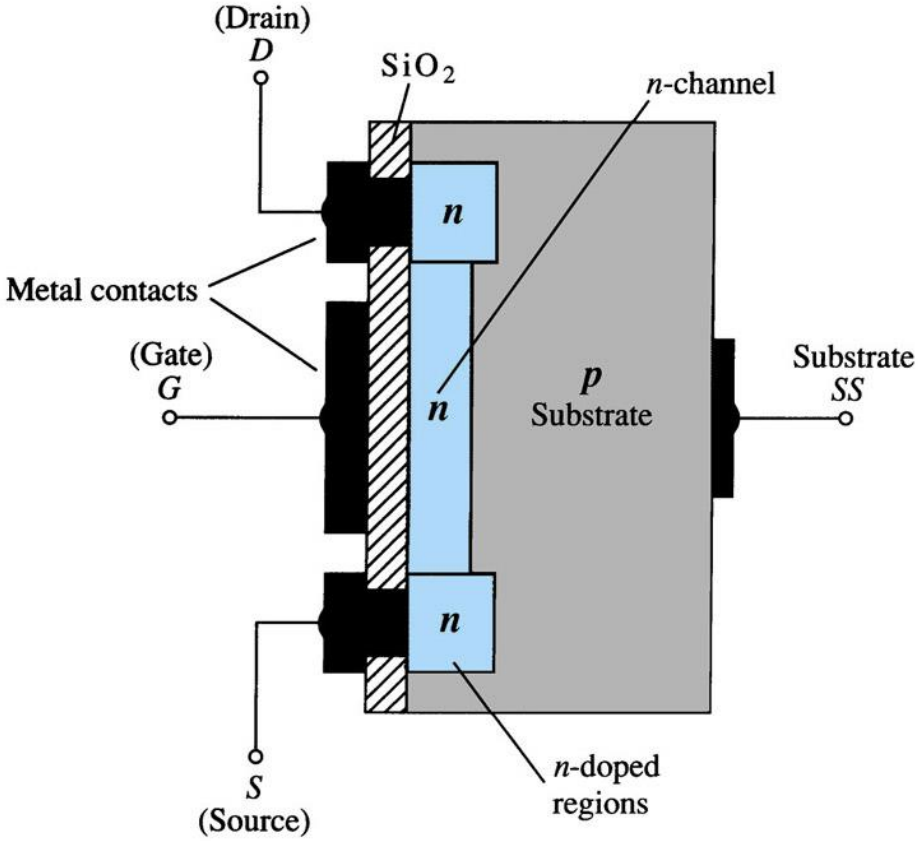


D-MOSFET Symbols

E-MOSFET Symbols

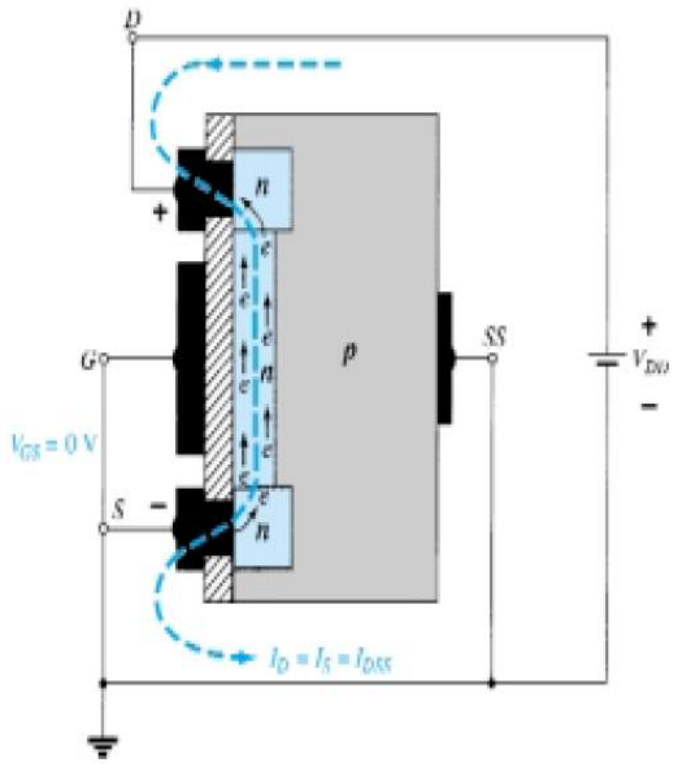


Depletion Mode MOSFET Construction

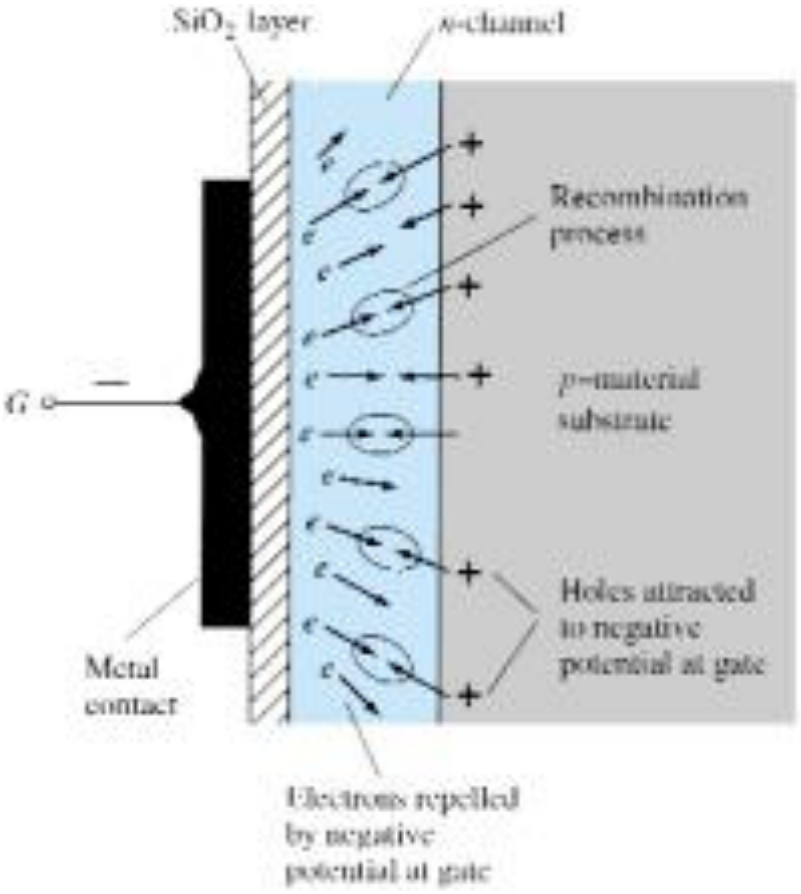


The Drain (D) and Source (S) leads connect to the to n-doped regions
These N-doped regions are connected via an n-channel
This n-channel is connected to the Gate (G) via a thin insulating layer of SiO_2
The n-doped material lies on a p-doped substrate that may have an additional terminal connection called SS

Basics Operation

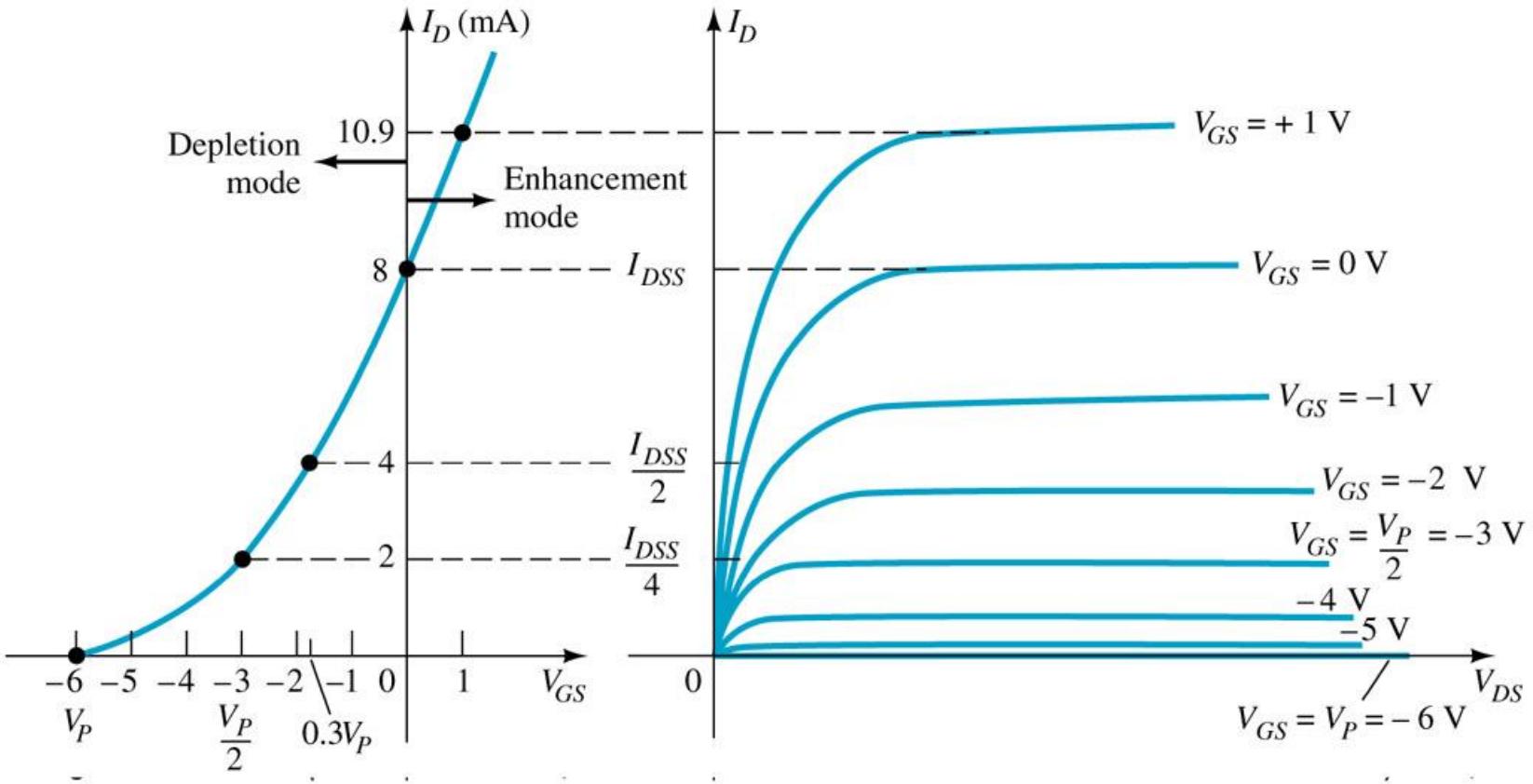


n-Channel depletion-type MOSFET with V_{GS} = 0 V and an applied

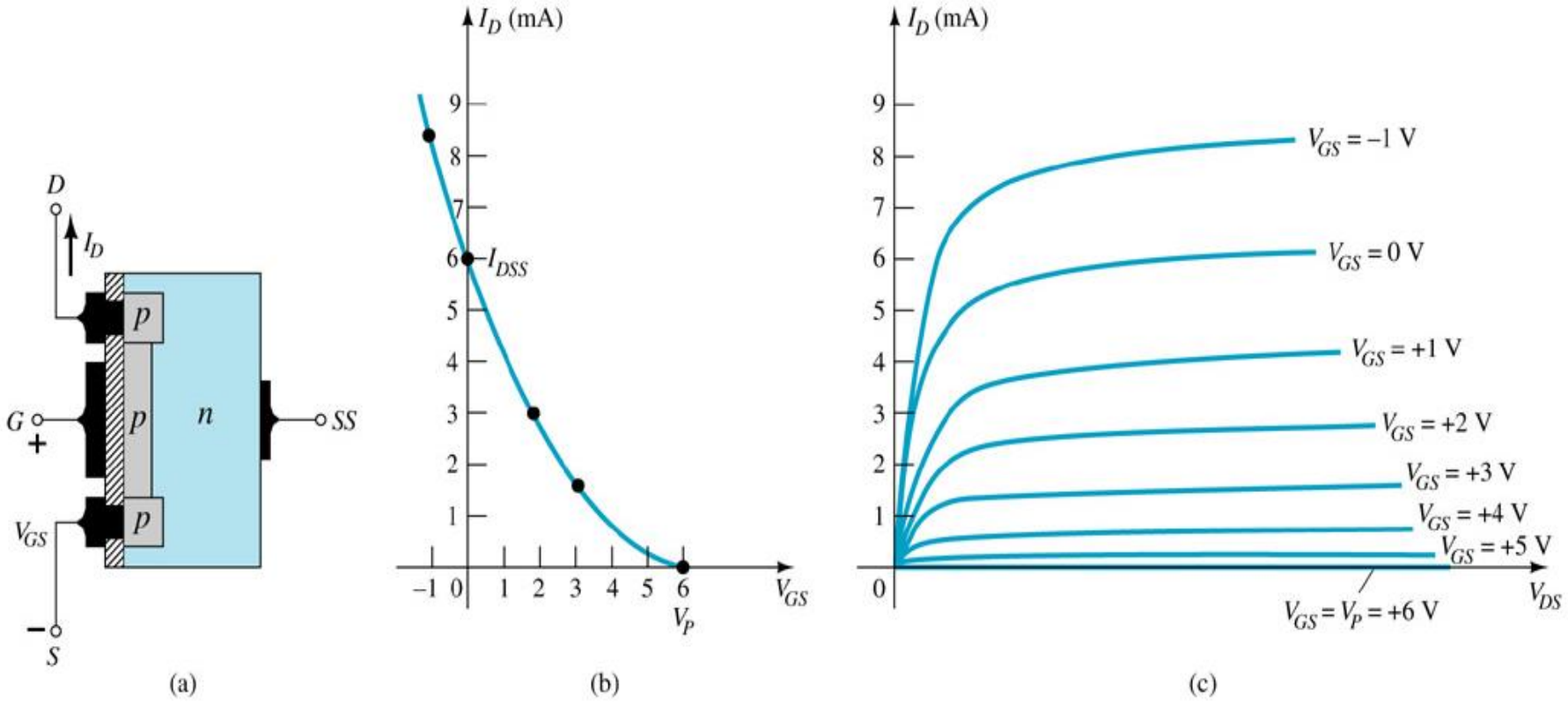


Basic Operation

A D-MOSFET may be biased to operate in two modes:
the **Depletion** mode or the **Enhancement** mode



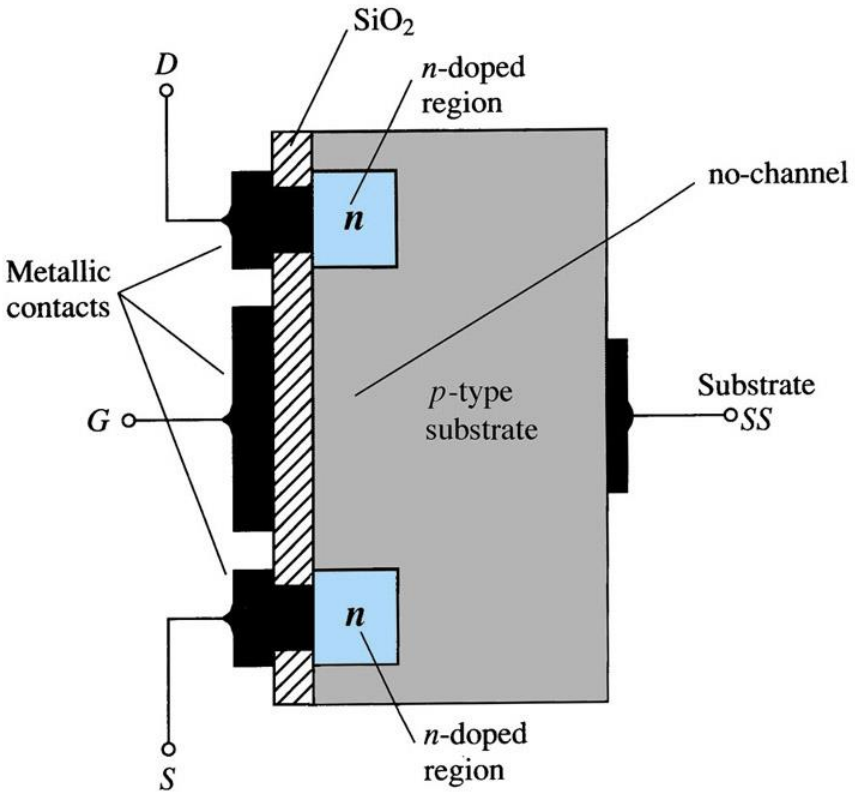
p-Channel Depletion Mode MOSFET



The p-channel Depletion mode MOSFET is similar to the n-channel except that the voltage polarities and current directions are reversed

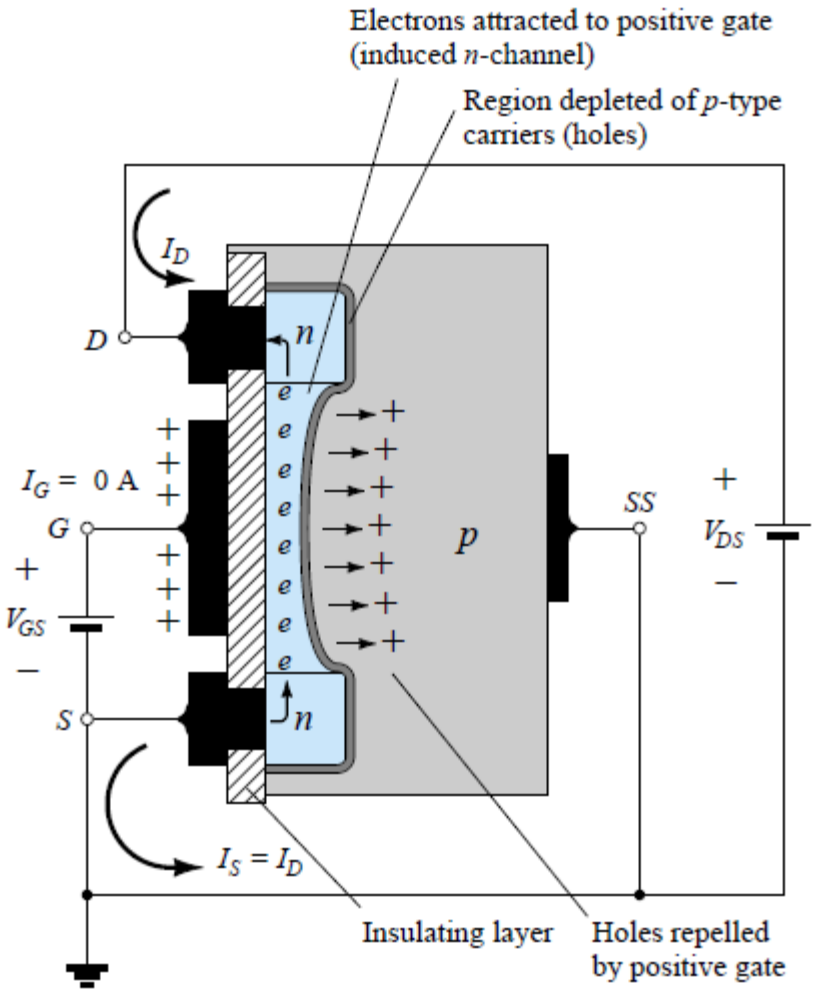
Enhancement Mode MOSFET's

Enhancement Mode MOSFET Construction



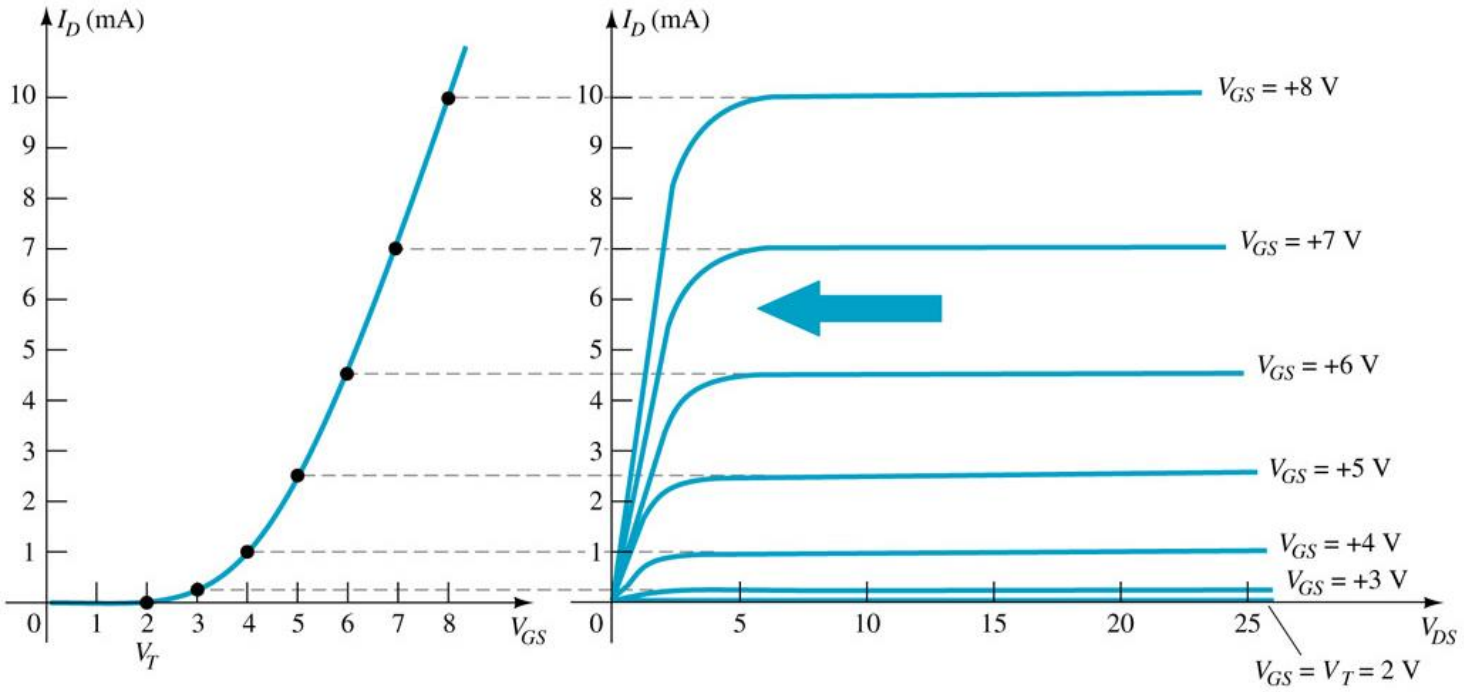
The Drain (D) and Source (S) connect to the to n-doped regions
These n-doped regions are not connected via an n-channel without an external voltage
The Gate (G) connects to the p-doped substrate via a thin insulating layer of SiO_2
The n-doped material lies on a p-doped substrate that may have an additional terminal connection called SS

Basics operation



Basic Operation

The Enhancement mode MOSFET only operates in the enhancement mode.



V_{GS} is always positive

$I_{DSS} = 0$ when $V_{GS} < V_T$

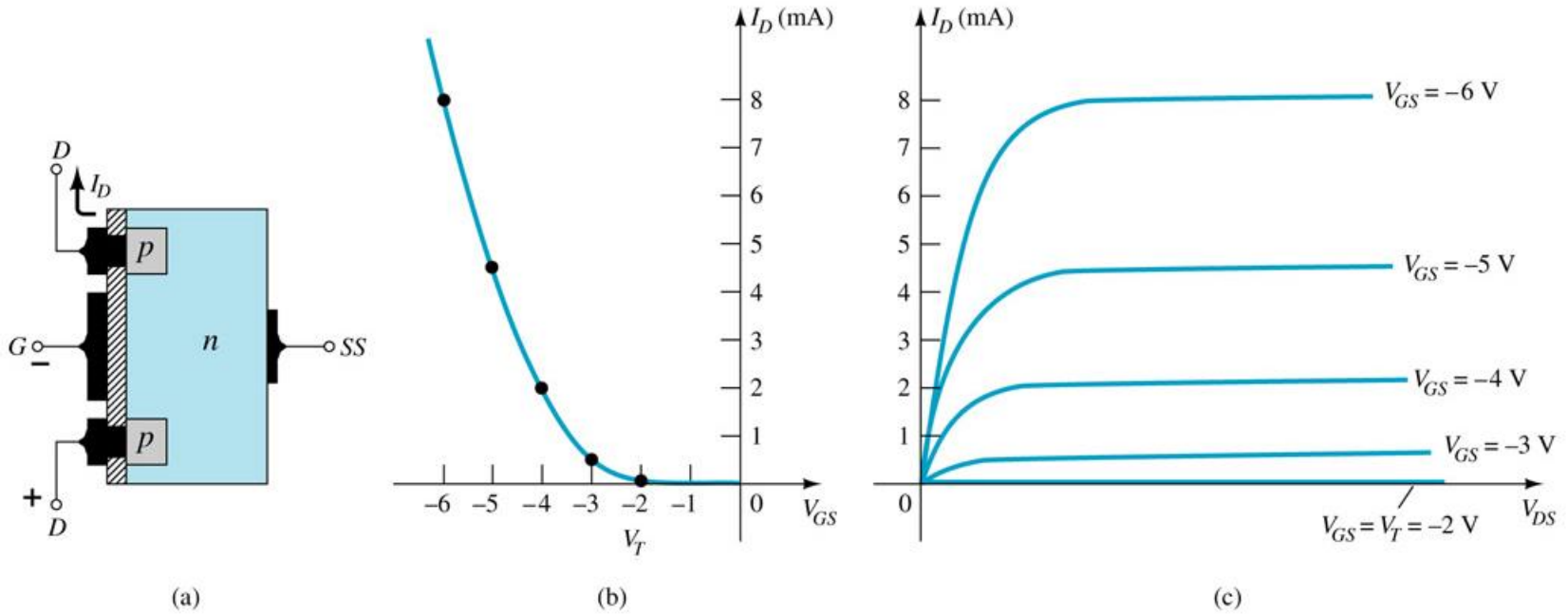
As V_{GS} increases above V_T, I_D increases

If V_{GS} is kept constant and V_{DS} is increased, then I_D saturates (I_{DSS})

The saturation level, V_{DSsat} is reached.

p-Channel Enhancement Mode MOSFETs

The p-channel Enhancement mode MOSFET is similar to the n-channel except that the voltage polarities and current directions are reversed.



MCQ

A JFET has three terminals, namely ……

(A) cathode, anode, grid

(B) emitter, base, collector

(C) source, gate, drain

(D) none of the above

MCQ

A MOSFET is a …… driven device

(A) current

(B) voltage

(C) both current and voltage

(D) none of the above

MCQ

A MOSFET can be operated with …….

(A) negative gate voltage only

(B) positive gate voltage only

(C) positive as well as negative gate voltage

(C) none of the above

MCQ

The input control parameter of a MOSFET is ……

(A) gate voltage

(B) source voltage

(c) drain voltage

(D) gate current

MCQ

The input impedance of a MOSFET is of the order of …….

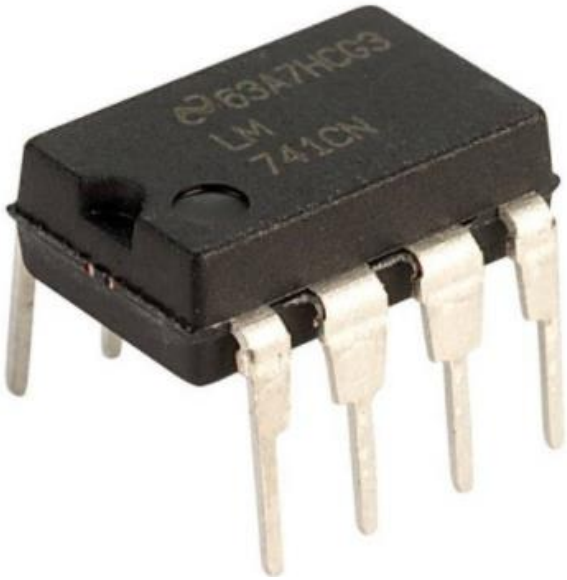
(A) 1 Ω

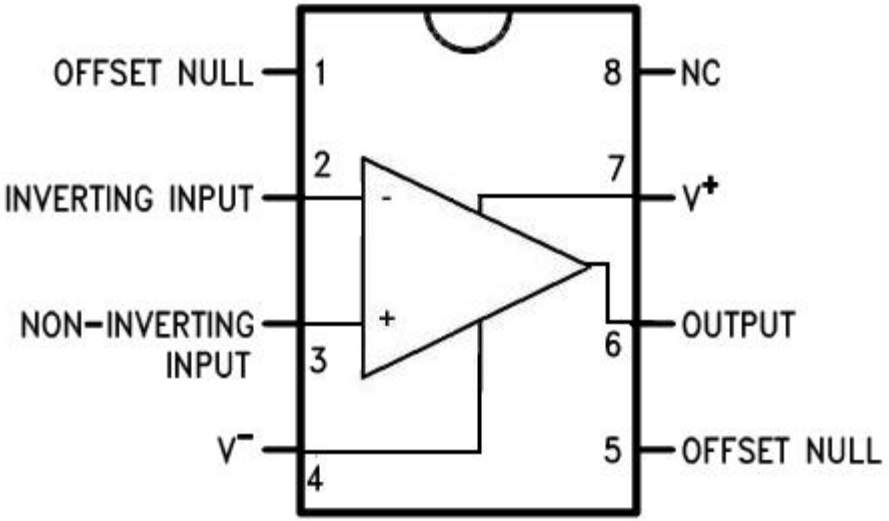
(B) a few hundred Ω

(C) kΩ

(D) several MΩ

OP-AMP
(Operational Amplifier)





MCQ

- In which of the following application op-amp is/are used?

(a) Integrator and Differentiator
(b) Voltage to Current Converter
(c) Adder or Summing Amplifier
(d) All of the above

Introduction

- OP-AMP is basically a multistage amplifier which uses a number of amplifier stages interconnected to each other.

- OP-AMP amplifies the difference between two signal and diminish common signal.

- The integrated op amp offers all the advantage of monolithic integrated circuit such as small size, high reliability, reduced cost, less power consumption.

MCQ

- **Op-Amp is abbreviated as _____.**

(a) Operational Amplifier

(b) Operand amplitude

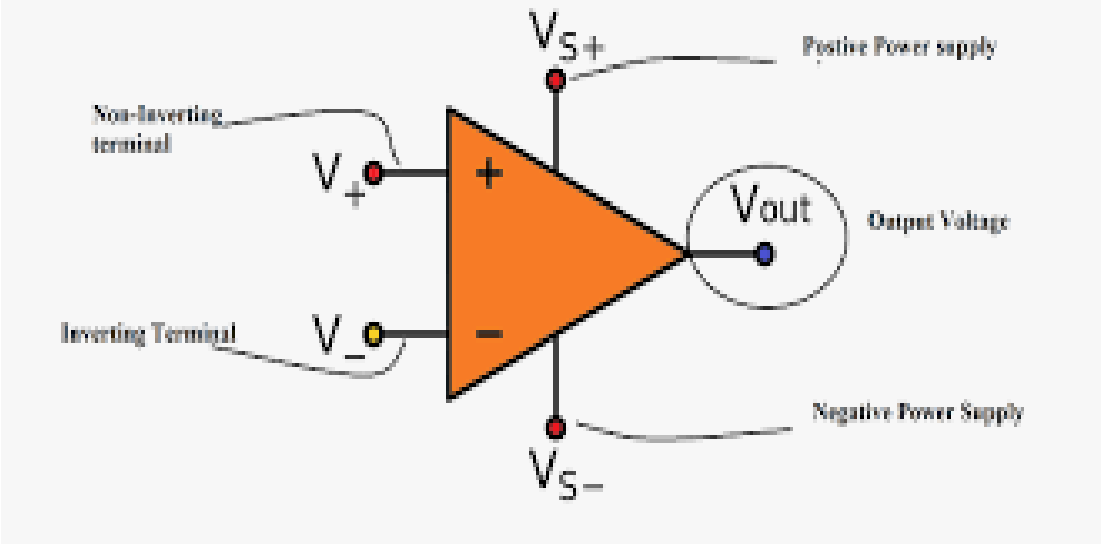
(c) Operational amplitude

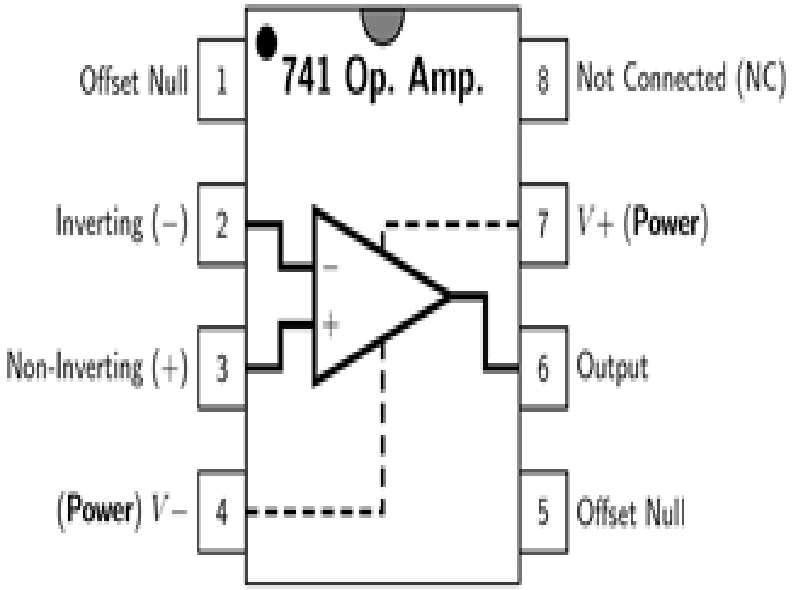
(d) None of the above

MCQ

- **The Op-amp can amplify**
- (a) a.c. signals only
- (b) d.c. signals only
- (c)both a.c. and d.c. signals
- (d) neither d.c. nor a.c. signals

Symbol and terminals





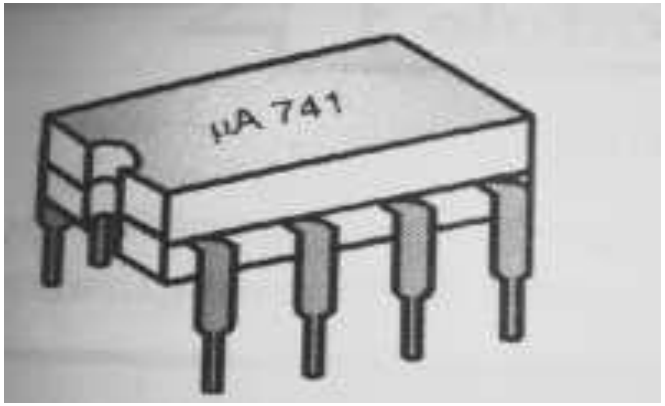
- An OP-AMP has a two input terminal, one output terminal and two supply voltage terminals.
- The input terminal marked with negative(-) sign is called as an inverting terminal .

If we connect the input signal to this terminal then the amplified output signal is 180º out of phase with respect to input.

- The input terminal marked with positive (+) sign is called as Non-Inverting terminal.

If the input is applied to this pin then the amplified output is in phase with the input.

- Offset null is used to nullify the offset voltage and pin no 8 is dummy pin.

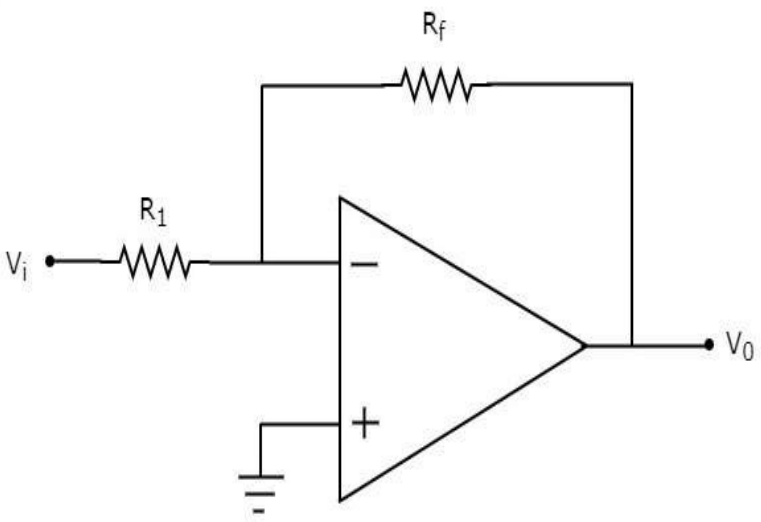


MCQ

- Op-Amp has _____ gain.

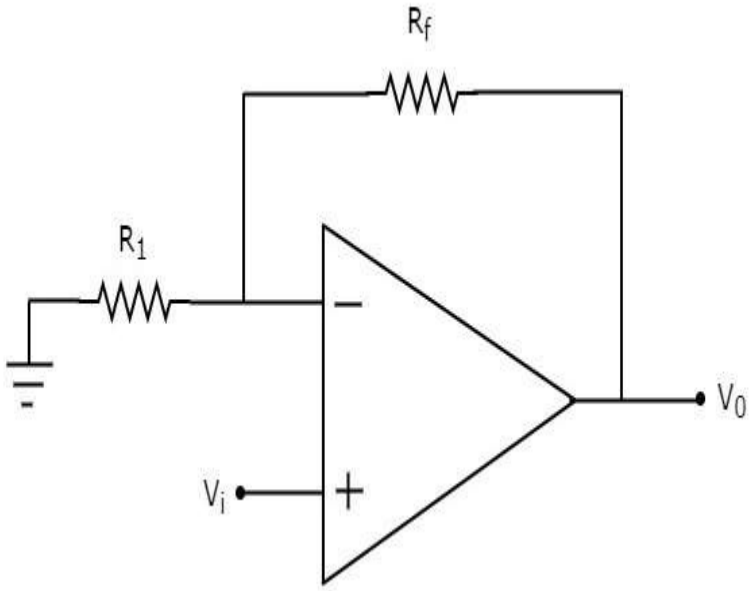
(a) Low
(b) High
(c) Zero
(d) Infinity

Inverting Amplifier



$$\frac{V_0}{V_i} = \frac{-R_f}{R_1}$$

Non- Inverting Amplifier



$$\frac{V_0}{V_i} = 1 + \frac{R_f}{R_1}$$

Characteristics of an OP-AMP

- Characteristics are important because, we can use them to compare the performance of various op amp ICs and select the best suitable from them for the required application.

characteristics	Practical value	Ideal value
Voltage gain	2×10^5	∞
Input resistance	2MΩ	∞
Output resistance	75Ω	0
Bandwidth	1 MHz	∞
CMRR	90 dB	∞
Slew rates	0.5V/μs	∞
PSRR	150μV/V	0

MCQ

- Which one of the following characteristics is true for ideal op-amp?

(a) Ri=0

(b) Ro= ∞

(c) B.W.= 0

(d) CMRR= ∞

MCQ

- Which one of the following characteristics is not true for ideal op-amp?

(a) Ri= ∞

(b) Ro= 0

(c) B.W.= 0

(d) Gain= ∞

MCQ

- Which one of the following combination for op-amp characteristics is true ?

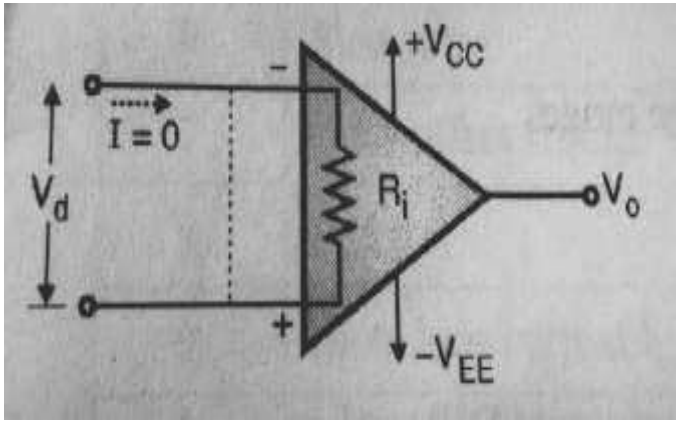
(a) Ri= ∞, Voltage gain= 0

(b) Ro= 0, CMRR= ∞

(c) B.W.= 0, Voltage Gain= 0

(d) Gain= ∞, Slew Rate = 0

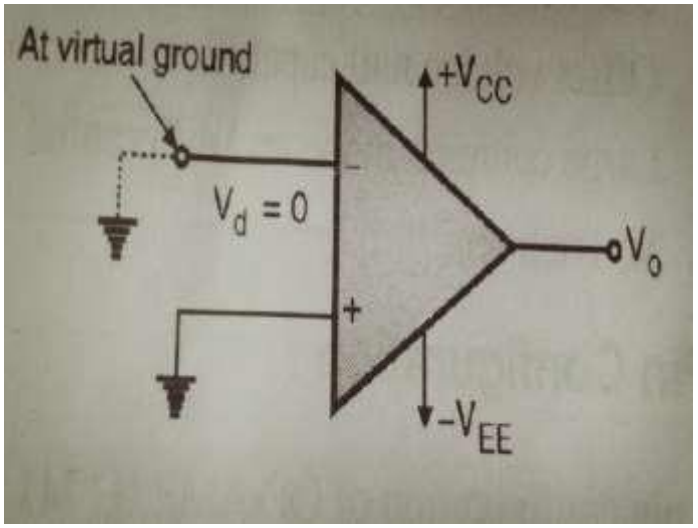
Concept of virtual short



- The input impedance of an OP-AMP is ideally infinite. Hence current flowing from one input terminal to the other will be zero.
- Thus the voltage drop across Ri will be zero and both the terminals will be at the same potential.
- Means they are virtually shorted to each other

Virtual Ground

If one of the terminal of OP-AMP is connected to ground then due to the virtual short existing between the other input terminal, the other terminal is said to be at ground potential.



Any Queries