**FSM**

**TESTBENCH:**

TEST BENCH:

module tb\_gray\_fsm;

reg clk;

reg reset;

wire [1:0] state;

// Instantiate the FSM module

gray\_fsm uut (

.clk(clk),

.reset(reset),

.state(state)

);

// Clock generation

always #5 clk = ~clk; // 10-time units period

initial begin

// Initialize signals

clk = 0;

reset = 1;

// Apply reset

#10 reset = 0;

// Allow the FSM to transition through states

#100;

// End simulation

$finish;

end

initial begin

// Monitor the state changes

$monitor("Time = %0t, State = %b", $time, state);

end

endmodule