**FSM**

**VERILOG CODE:**

module gray\_fsm (

input clk,

input reset,

output reg [1:0] state

);

// Gray code state encoding

parameter S0 = 2'b00, // Gray: 00

S1 = 2'b01, // Gray: 01

S2 = 2'b11, // Gray: 11

S3 = 2'b10; // Gray: 10

always @(posedge clk or posedge reset) begin

if (reset)

state <= S0;

else begin

case (state)

S0: state <= S1;

S1: state <= S2;

S2: state <= S3;

S3: state <= S0;

default: state <= S0;

endcase

end

end

endmodule