Academic Projects

RFIC design projects:

Impedance matching with smith chart on ADS

- Implemented matching network for various types like 50 ohms to complex load, complex source to complex load, complex source to 50 ohms load at 6 GHz.
- Simulations, components: S-parameters, Impedance vs Frequency, Smith chart utility tool.

Design of high directivity directional coupler *(HFSS)*

- Designed a coupler that has Coupling factor=-19 dB, Directivity = -50 dB and Reflection coefficient = -40 dB at 2.2 GHz by taking S parameter plots in HFSS.
- Designed a matched network for coupled lines with Z_{line} = 54.48 and $\theta = 61.26^0$ (physical parameter.
- Additionally decreased size to an extent, high directivity (-30 dB → -50 dB) to produce a compact device with coupled line and matching network.

Low Noise Amplifier in 65nm (*Cadence Virtuoso)*

- Implemented LNA that has gain = 10dB, noise figure = 1.8 dB, input return loss = -8.2 dB, IIP3 = -10 dBm.
- Characterization of MOSFET with g_m= 20ms, I_{bias} =1mA, parameters like WL, C_{gs} to obtain L_{ext} for matching.

Analog IC design projects:

Low Dropout Regulator *(Cadence Virtuoso)*

- Designed LDO to provide constant regulated voltage of 2.7 V with a supply voltage of 3V. This LDO can tolerate 1mA-40mA load current variation for CL = 200pF.
- Performed necessary hand calculations to design error amplifier with the gain = 45.5 dB, Phase Margin = 62 dB, Bandwidth = 1.28MHz. Performed DC analysis to check the operating point of all the transistors for meeting gain and phase margin spec.
- Performed AC, stb analysis to find loop gain, unity gain bandwidth and phase margin of the system at different load current (1mA, 10mA, 40mA) and transient analysis to verify line regulation for step input (3V – 3.2V).

CMOS based Voltage Reference for low power applications *(Cadence Virtuoso)*

- Implemented a PTAT circuit that replaces diodes used in traditional PTAT generator and observed how current and size ratios determine PTAT voltage and compared with traditional bandgap circuits.
- Designed a voltage reference circuit that consists of PTAT, CTAT, current bias circuit and analysed with different process corners as the function of temperature and found reference voltage varies with the PVT variation.

Design and layout of fully differential telescopic cascode amplifier with CMFB *(Cadence Virtuoso)*

- Designed differential telescopic opamp for the Gain = 72 dB, differential output swing = 3V, power dissipation = 10mW, Gain-Bandwidth product: 122MHz, supply = 3V.
- Obtained device dimensions form required output swing, bias current, overdrive voltages and increased PMOS devices width for higher gain.
- Obtained bias voltages from input CM level, Performed DC analysis to check the operating point of all the transistors, AC, stb analysis to find loop gain, stability requirements.
- Located poles of the opamp and increased output capacitance for meeting the bandwidth and phase margin requirements.

Designed Bandgap reference circuit *(Cadence Virtuoso)*

- Designed CTAT circuit with a diode (BJT), PTAT with the series of diodes (BJT) and simulated respective voltages in reference to temperature.
- Observed PTAT slope is lesser than CTAT, used ratio of resistors to scale the PTAT with CTAT.
- Obtained reference voltage as 1.2 V and simulated the bandgap circuit in various process corners.
- Achieved low temperature coefficients of 150ppm/C across temperature range of -20^{o}C to 120^{o}C by efficient slope cancellation of PTAT and CTAT currents.

Process corner analysis and Monte Carlo analysis *(Cadence Virtuoso)*

- Analyzed variation of β_{eff} and V_{th} variation of four diode connected MOSFET's under different process corners by setting the environment in ADEXL (Process-Mismatch statistical variation in Montecarlo).
- Understood process corners like strong, weak, typical and respective V_{th} and current variation by doing DC analysis on four transistors.

Digital design:

RTL Design and Verification of Flip Flop and Multiplier *(System Verilog, UVM)*

- Designed data flip flop and combinational multiplier using RTL design code and created interface. Implemented sequencer, driver, monitor, agent and environment in verification environment.
- Verified the functionality of the UVM test bench and analysed the results using the scoreboard.

Data Convertors:

Design of Flash ADC *(Cadence Virtuoso)*

- This project involves design of a 4-bit Flash ADC with power consumption less than 1.5mW and sampling frequency 20MHz.
- A fully differential dynamic comparator is used so that input offset is contributed by differential pair.
- Studied and analysed performance metrics like kickback noise, offset, regeneration time.

Design of a sampling network and switch capacitor circuit (*Cadence Virtuoso, Simulink***)**

- Designed a sampling network to generate the FFT spectrum for 13/1024 and 499/1024 input frequencies and explored different switches to produce SFDR = 60 dB, compared the SFDR metric between ideal switch, Tgate and bootstrap switch.
- Designed a parasitic insensitive integrator with the sampling network and a folded cascode opamp to achieve open loop gain – 65 dB, phase margin- 62^0, closed loop gain- 2 dB which achieved a settling time of 40ns. Understood concept of parasitic capacitances, charge injection, bottomplate sampling.

Power Electronics:

Feedback Control System for a 75 W Buck Converter (*Simulink)*

- Designed a buck converter and its feedback control loop using a PID controller to obtain a phase margin of 30 degrees.
- Simulated the model on MATLAB to collect phase margin and observed time domain response at different input voltages.