Academic Projects

RFIC design projects:

Design of high directivity directional coupler *(HFSS)*

- Designed a coupler that has Coupling factor=-19 dB, Directivity = -50 dB and Reflection coefficient = -40 dB at 2.2 GHz by taking S parameter plots in HFSS.
- Designed a matched network for coupled lines with Z_{line} = 54.48 and θ = 61.26^0 (physical parameter.
- Additionally decreased size to an extent, high directivity (-30 dB → -50 dB) to produce a compact device with coupled line and matching network.

Low Noise Amplifier in 65nm (*Cadence Virtuoso)*

- Implemented LNA that has gain = 10dB, noise figure = 1.8 dB, input return loss = -8.2 dB, IIP3 = -10 dBm.
- Characterization of MOSFET with g_m= 20ms, I_{bias} =1mA, parameters like WL, C_{gs} to obtain L_{ext} for matching.

Analog IC design projects:

Design and layout of fully differential telescopic cascode amplifier with CMFB *(Cadence Virtuoso)*

- Designed differential telescopic opamp for the Gain = 72 dB, differential output swing = 3V, power dissipation = 10mW, Gain-Bandwidth product: 122MHz, supply = 3V.
- Obtained device dimensions form required output swing, bias current, overdrive voltages and increased PMOS devices width for higher gain.
- Obtained bias voltages from input CM level, Performed DC analysis to check the operating point of all the transistors, AC, stb analysis to find loop gain, stability requirements.
- Located poles of the opamp and increased output capacitance for meeting the bandwidth and phase margin requirements.

Designed Bandgap reference circuit *(Cadence Virtuoso)*

- Designed CTAT circuit with a diode (BJT), PTAT with the series of diodes (BJT) and simulated respective voltages in reference to temperature.
- Observed PTAT slope is lesser than CTAT, used ratio of resistors to scale the PTAT with CTAT.
- Obtained reference voltage as 1.2 V and simulated the bandgap circuit in various process corners.
- Achieved low temperature coefficients of 150ppm/C across temperature range of -20°C to 120°C by efficient slope cancellation of PTAT and CTAT currents.

Process corner analysis and Monte Carlo analysis *(Cadence Virtuoso)*

- Analyzed variation of β_{eff} and V_{th} variation of four diode connected MOSFET's under different process corners by setting the environment in ADEXL (Process-Mismatch statistical variation in Montecarlo).
- Understood process corners like strong, weak, typical and respective V_{th} and current variation by doing DC analysis on four transistors.

Data Convertors:

Design of Flash ADC *(Cadence Virtuoso)*

- This project involves design of a 4-bit Flash ADC with power consumption less than 1.5mW and sampling frequency 20MHz.
- A fully differential dynamic comparator is used so that input offset is contributed by differential pair.
- Studied and analysed performance metrics like kickback noise, offset, regeneration time.

Design of a sampling network and switch capacitor circuit (*Cadence Virtuoso, Simulink***)**

- Designed a sampling network to generate the FFT spectrum for 13/1024 and 499/1024 input frequencies and explored different switches to produce SFDR = 60 dB, compared the SFDR metric between ideal switch, Tgate and bootstrap switch.
- Designed a parasitic insensitive integrator with the sampling network and a folded cascode opamp to achieve open loop gain – 65 dB, phase margin- 62^0, closed loop gain- 2 dB which achieved a settling time of 40ns. Understood concept of parasitic capacitances, charge injection, bottomplate sampling.

Design of 1.5-bit MDAC for pipelined ADC *(Cadence Virtuoso)*

- Designed a switched capacitor residue amplifier based on folded cascode structure which provides a 10-bit settling and 10-bit DC gain, performed 1024-point FFT on the output to get SNR (58.4 dB), ENOB (9.8 bits).
- Designed a differential dynamic comparator which is used in Sub-ADC and reduced the input referred offset to 4.3 mV from 10 mV by using offset cancellation at second stage.
- Compared SFDR metric between ideal switch, T-gate, and bootstrap switch to provide required SFDR of 60 dB by taking a FFT spectrum, analysed trade-off between (W/L), R_{on} and parasitic capacitances in the circuit.

Power Electronics:

Feedback Control System for a 75 W Buck Converter (*Simulink)*

- Designed a buck converter and its feedback control loop using a PID controller to obtain a phase margin of 30 degrees.
- Simulated the model on MATLAB to collect phase margin and observed time domain response at different input voltages.