AASISH ARUMILLI

aasisharumilli@ufl.edu | +1 352-709-9076 | https://github.com/AasishArumilli

EDUCATION:

Master of Science in Electrical and Computer Engineering, University of Florida, Gainesville, FL ***Aug 2022 -June 2024***

- Coursework: Analog Integrated Circuit design, Power Electronics, Data Convertors, Intro to RF circuits, Digital Circuits and Systems, VLSI circuits and technology, Computer Architecture (***GPA – 3.3***)

Bachelor of Technology in Electronics and Communication, JNTU, Hyderabad, India ***May 2020***

SKILLS:

- **Programming Languages:** C, Python
- **Hardware Description Languages:** VHDL, Verilog
- **Design Tools:** Cadence Virtuoso, Matlab, Simulink, Ansys HFSS, Simplis.

EXPERIENCE:

ANALOG IC DESIGN INTERN (Texas Instruments – Dallas, Texas) ***May 2023 – Aug 2023***

- Worked with medium voltage buck converter team to redesign a 1.8V LDO (Low Dropout voltage regulator) for a nominal input of 4.5V.
- Analysed three subcircuits of the LDO: Soft Starter circuit, PMOS LDO and current limiting circuit
- Examined the no load, full load conditions and conducted stability analysis, Ran Monte Carlo simulations and PVT across 5 corners and three temperatures: -55C, 27C and 150C.

ACADEMIC PROJECTS:

Low Dropout Regulator *(Cadence Virtuoso)* ***Dec 2023 – Jan 2024***

- Designed LDO to provide constant regulated voltage of 2.7 V with a supply voltage of 3V. This LDO can tolerate 1mA-40mA load current variation for CL = 200pF.
- Performed necessary hand calculations to design error amplifier with the gain = 45.5 dB, Phase Margin = 62 dB, Bandwidth = 1.28MHz. Performed DC analysis to check the operating point of all the transistors for meeting gain and phase margin spec.
- Performed AC, stb analysis to find loop gain, unity gain bandwidth and phase margin of the system at different load current (1mA, 10mA, 40mA) and transient analysis to verify line regulation for step input (3V – 3.2V).
- Located Pole-zero locations and experimented with frequency compensation techniques (miller, cascode) and understood their drawbacks.
- Implemented a buffer at the o/p of EA which lowers i/p capacitance, o/p resistance of EA to make LDO output pole dominant.

CMOS based Voltage Reference for low power applications *(Cadence Virtuoso)* ***Sep 2023 – Oct 2023***

- Implemented a PTAT circuit that replaces diodes used in traditional PTAT generator and observed how current and size ratios determine PTAT voltage and compared with traditional bandgap circuits.
- Designed a voltage reference circuit that consists of PTAT, CTAT, current bias circuit and analysed with different process corners as the function of temperature and found reference voltage varies with the PVT variation.
- Designed a nano-ampere current multiplier (PTAT) that is resistant to PVT variation where all PVT parameters are compensated with each other. Performed PVT variation, Monte Carlo for choosing aspect ratio of transistors.

Design and simulation of 2-stage operational amplifier with frequency compensation (*Cadence Virtuoso)* ***Nov 2022***

- This project involved designing a 2-stage amplifier where differential amplifier is the first stage and cascode amplifier as the second stage, miller compensation for improving stability.
- Performed hand calculations for transistor sizing according to current mirror biasing, gain, UGBW and phase margin requirements. Used miller cap, compensation res for pole splitting and eliminating zero to achieve phase margin.

Design of high directivity directional coupler *(RFIC design – HFSS)* ***Oct 2023***

- Designed a coupler that have high directivity - -50dB, coupling factor- -19dB, reflection coefficient- -40dB, took S-para plots.
- Additionally decreased size, improved directivity (-30dB→-50dB) and designed matching N/W for four ports.

Design of Low noise amplifier in 65nm *(RFIC design- Cadence Virtuoso)* ***Nov 2023***

- Implemented LNA that has gain = 10dB, noise figure = 1.8 dB, input return loss = -8.2 dB, IIP3 = -10 dBm.
- Characterization of MOSFET with g_m= 20ms, I_{bias} =1mA, parameters like WL, C_{gs} to obtain L_{ext} for matching.