

# Academic Projects

## Feedback Control System for a 75 W Buck Converter (*Simulink*)

- Designed a buck converter and its feedback control loop using a PID controller to obtain a phase margin of 30 degrees.
- Simulated the model on MATLAB to collect phase margin and observed time domain response at different input voltages.

## Design and layout of fully differential telescopic cascode amplifier with CMFB (*Cadence Virtuoso*)

- Designed differential telescopic opamp for the Gain = 72 dB, differential output swing = 3V, power dissipation = 10mW, Gain-Bandwidth product: 122MHz, supply = 3V.
- Obtained device dimensions from required output swing, bias current, overdrive voltages and increased PMOS devices width for higher gain.
- Obtained bias voltages from input CM level, Performed DC analysis to check the operating point of all the transistors, AC, stb analysis to find loop gain, stability requirements.
- Located poles of the opamp and increased output capacitance for meeting the bandwidth and phase margin requirements.

## Low Noise Amplifier (*Cadence Virtuoso*)

- Implemented a low noise amplifier using a cascade configuration.
- The power gain of the amplifier was 11.4dB at frequencies between 3.3Ghz and 3.4Ghz.
- The noise figure was 1.8dB and the voltage standing wave ratio at the input and output was 1.14 and 1.04 respectively.

## Design of voltage-controlled oscillator and frequency divider at 2.4GHz (*Cadence Virtuoso*)

- Designed an LC VCO with operating frequency of 2.4GHz and a Phase noise of -122dBc/Hz.
- Technologies used: Cadence Spectre

## Process corner analysis and Monte Carlo analysis (*Cadence Virtuoso*)

- Analyzed variation of  $\beta_{\text{eff}}$  and  $V_{\text{th}}$  variation of four diode connected MOSFET's under different process corners by setting the environment in ADEXL (Process-Mismatch statistical variation in Montecarlo).
- Understood process corners like strong, weak, typical and respective  $V_{\text{th}}$  and current variation by doing DC analysis on four transistors.

### **Designed Bandgap reference circuit** (*Cadence Virtuoso*)

- Designed CTAT circuit with a diode (BJT), PTAT with the series of diodes (BJT) and simulated respective voltages in reference to temperature.
- Observed PTAT slope is lesser than CTAT, used ratio of resistors to scale the PTAT with CTAT.
- Obtained reference voltage as 1.2 V and simulated the bandgap circuit in various process corners.
- Achieved low temperature coefficients of 150ppm/C across temperature range of -20°C to 120°C by efficient slope cancellation of PTAT and CTAT currents.

### **Design of Flash ADC** (*Cadence Virtuoso*)

- This project involves design of a 4-bit Flash ADC with power consumption less than 1.5mW and sampling frequency 20MHz.
- A fully differential dynamic comparator is used so that input offset is contributed by differential pair.
- Studied and analysed performance metrics like kickback noise, offset, regeneration time.