

COL215 HW Assignment 1

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In this assignment we were supposed design and implement a circuit that takes a 4-digit decimal/hexadecimal number (so each number is 4-bit) from switches in the Basys3 board and displays it on the 4-seven segment displays on the board. We then had to use the on-board clock and create a timing circuit to drive all the displays.

To implement the hexadecimal seven segment display with 4 input and seven output, we made a truth table corresponding to each output and made a k map out of it. Using k map, we found formula for each output we required.

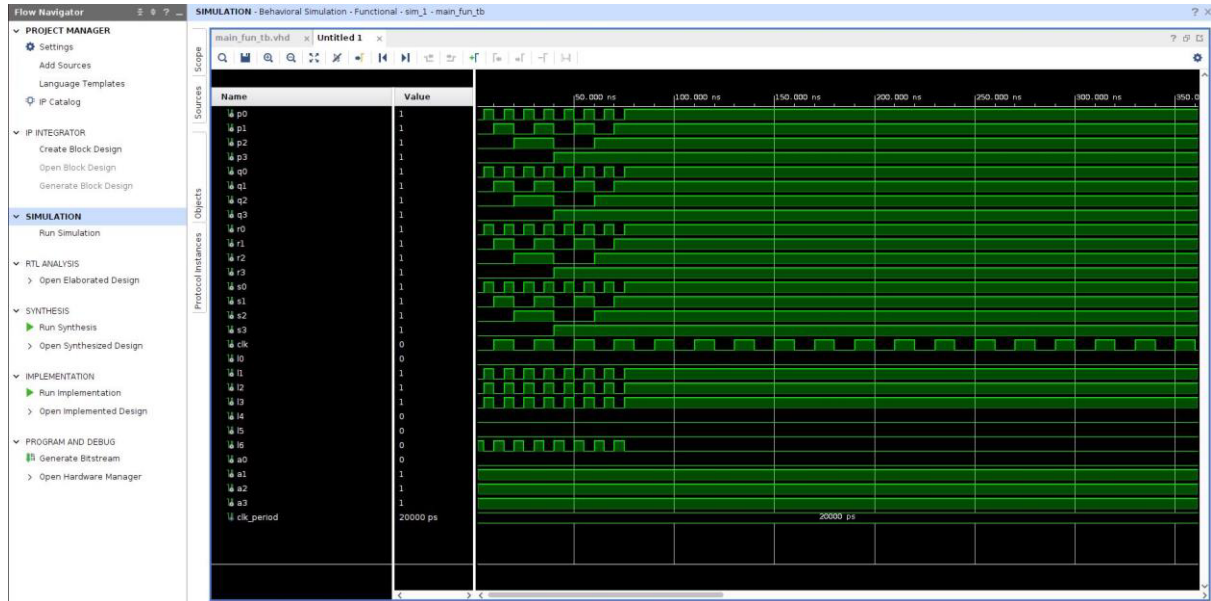
Now, to create timing circuit, we have used inbuilt clock, seven segment and mux implementation. We basically had to lower the frequency of inbuilt clock such that our eye does not detect flickering, is visible while allowing user's input.

To do so, we have first made two clocks, clock_1, clock_2 and decreased frequency of clock-1 such that its time period is increased by 500000 times and that of clock_2 by 250000 times. The inbuilt frequency of clock of basys board is 100MHz and time period is 10^{-8} sec. We cannot give input at such a fast frequency hence we need to lower this to around 100Hz (Our time period should be between 0 to 16 milli-seconds corresponding to our eye's persistence of image). To bring it to 100Hz we want our 1 cycle to accommodate 10^6 cycles of inbuilt clock.

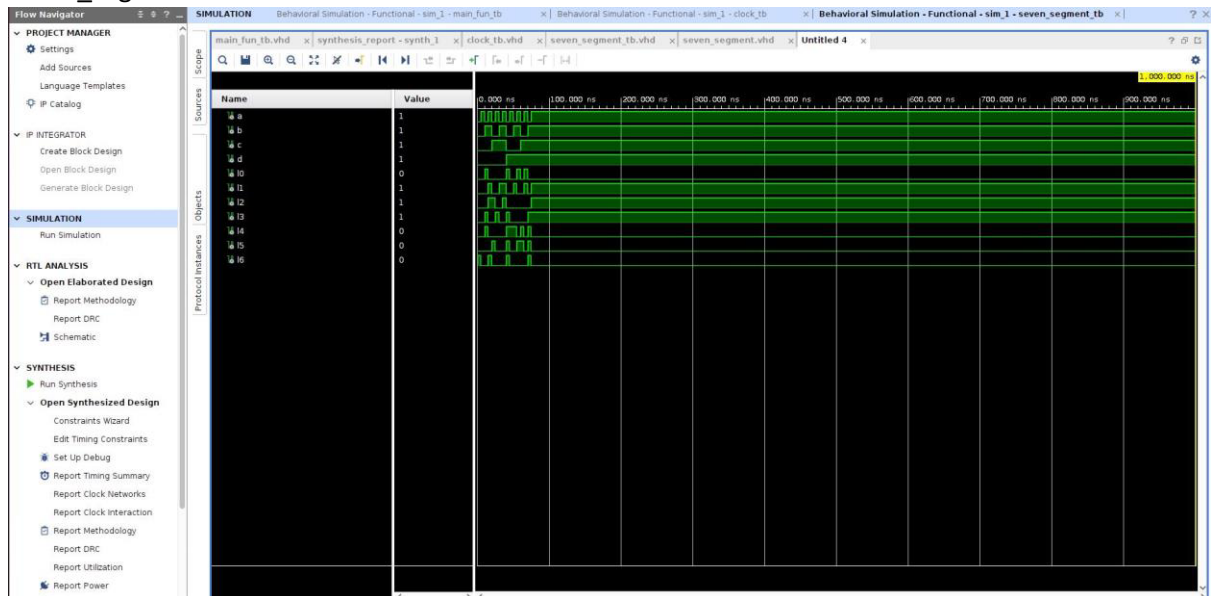
clock_1 and clock_2 corresponds to waveforms of selector lines of the multiplexer. To each pair of value of (clock_1, clock_2) we have to set it to an anode pin (four possible pairs). To make all 4 pairs we divide 10^6 cycles to 2 parts. For 5×10^5 cycles, waveform of clock_1 would be 1 and for rest, it would be 0. Now these 5×10^5 cycles are further divided by 2 for clock_2 to be 1 for half part and 0 for rest.

We have now made a new behavioural file named main_fun where we have imported seven_segment file and clock file. This function takes 16-bit inputs (4 corresponding to each anode). Our clock function gives 4 outputs for anode pins and 2 for selector lines. Using these selector lines, we have implemented a 4:1 mux. this mux takes 16 inputs in sets of four each and outputs single set of four bits. These 4 bits will be input for seven_segment. This seven_segment runs for each anode pin sequentially for each anode with gap of 2.5 milli-seconds (refresh rate). Vision of our eye persist for 16 milli-seconds. For our function, refresh rate is 2.5, so all four pins will display in 10 milli-seconds. Our eye will there-fore not be able to detect flickering.

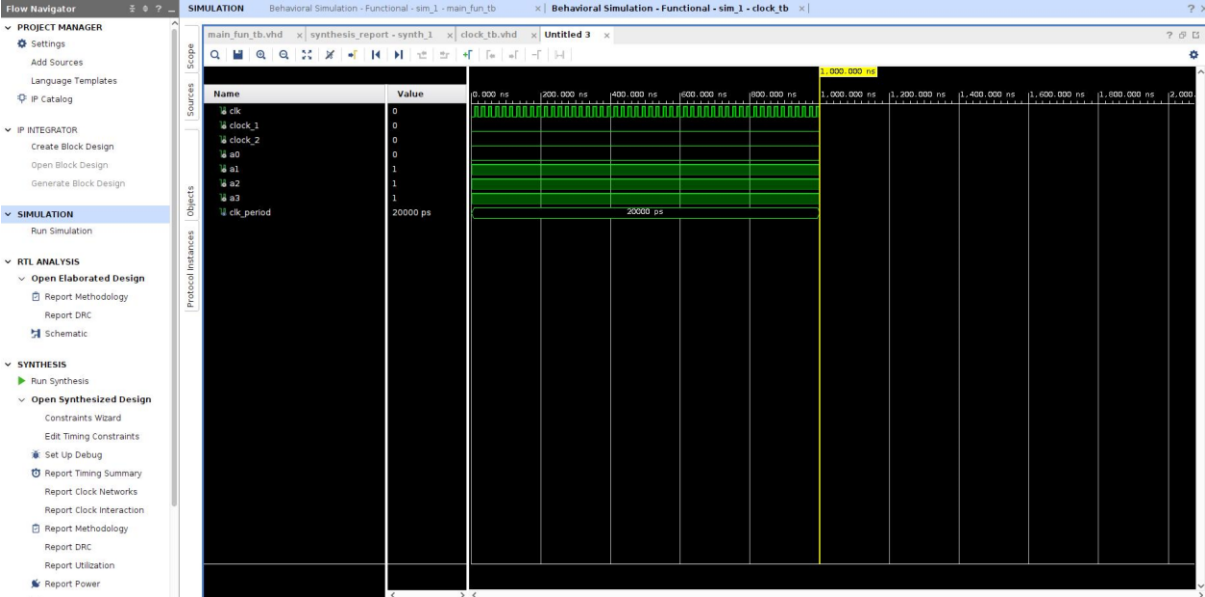
main_fun simulation



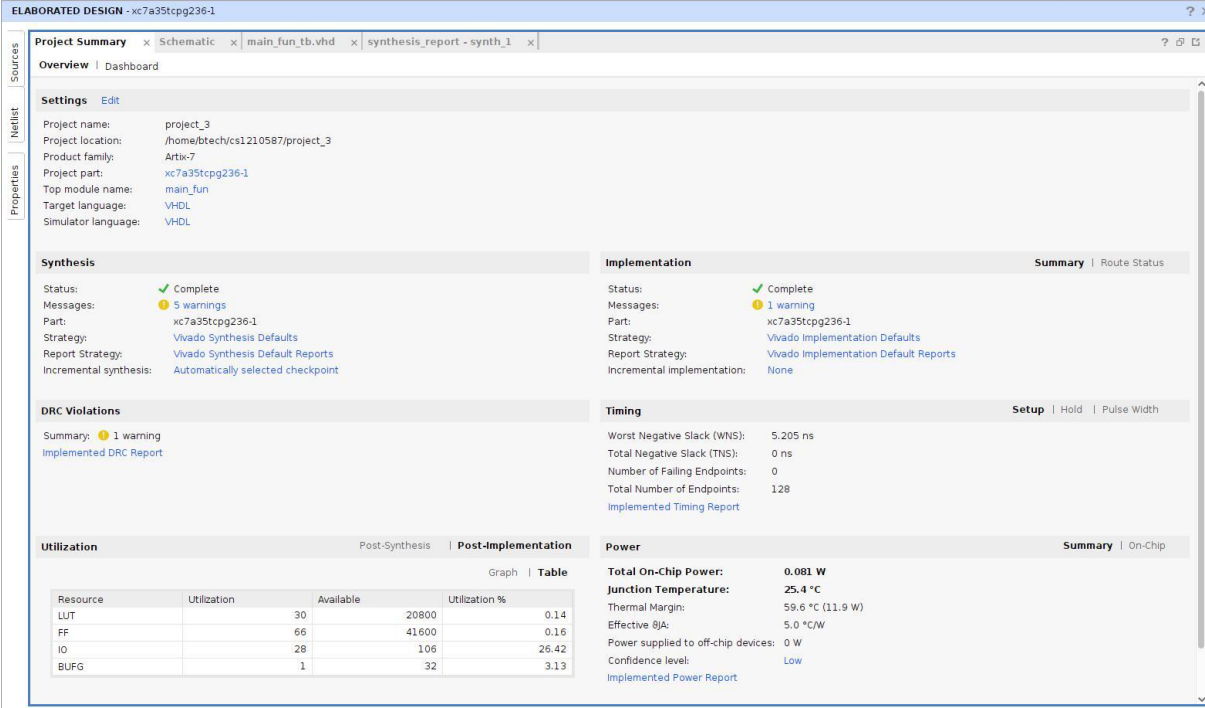
seven_segment simulation



clock simulation



synthesis report



Utilization

Post-Synthesis

| **Post-Implementation**

Graph

| **Table**

Resource	Utilization	Available	Utilization %
LUT	30	20800	0.14
FF	66	41600	0.16
IO	28	106	26.42
BUFG	1	32	3.13

BRAM,DSP

```
main_fun_tb.vhd x synthesis_report - synth_1 x clock_tb.vhd x seven_segment_tb.vhd x seven_segment.vhd x Untitled 4 x
/home/btech/cs1210587/project_3/project_3.runs/synth_1/main_fun.vds
Q [Icons] [Navigation] [Find] [Read-only] [Settings]
BRAM [Next] [Previous] [Highlight] [Match Case] [Whole Words] 1 Match(es)
73: Finished Constraint Validation : Time (s): cpu = 00:00:06 ; elapsed = 00:00:06 ; Memory (MB): peak = 2675.047 ; gain = 64.031 ; free physical = 24343 ; free virtual = 42675
74: .....
75: .....
76: Start Loading Part and Timing Information
77: .....
78: Loading part: xc7a35tcp236-1
79: .....
80: Finished Loading Part and Timing Information : Time (s): cpu = 00:00:06 ; elapsed = 00:00:06 ; Memory (MB): peak = 2675.047 ; gain = 64.031 ; free physical = 24343 ; free virtual = 42675
81: .....
82: .....
83: Start Applying 'set_property' XDC Constraints
84: .....
85: .....
86: Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:06 ; elapsed = 00:00:06 ; Memory (MB): peak = 2675.047 ; gain = 64.031 ; free physical = 24343 ; free virtual = 42675
87: .....
88: .....
89: Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:06 ; elapsed = 00:00:06 ; Memory (MB): peak = 2675.047 ; gain = 64.031 ; free physical = 24335 ; free virtual = 42668
90: .....
91: .....
92: Start RTL Component Statistics
93: .....
94: Detailed RTL Component Info :
95: +---Adders :
96: 2 Input 32 Bit Adders := 2
97: +---Registers :
98: 32 Bit Registers := 2
99: 1 Bit Registers := 2
100: +---Muxes :
101: 2 Input 32 Bit Muxes := 2
102: 2 Input 1 Bit Muxes := 4
103: .....
104: Finished RTL Component Statistics
105: .....
106: .....
107: Start Part Resource Summary
108: .....
109: Part Resources:
110: DSPs: 90 (col length:60)
111: BRAMs: 100 (col length: RAMB18 60 RAMB36 30)
112: .....
113: Finished Part Resource Summary
114: .....
115: .....
116: Start Cross Boundary and Area Optimization
117: .....
118: WARNING: [Synth 8-7080] Parallel synthesis criteria is not met
119: .....
120: Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:07 ; elapsed = 00:00:07 ; Memory (MB): peak = 2675.047 ; gain = 64.031 ; free physical = 24320 ; free virtual = 42656
121: .....
122: .....
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Schematic diagram

