COL HARDWARE ASSIGNMENT 2

STOPWATCH

Ashish Arora (2021CS10069) & Aaveg Jain (2021CS10073)

Problem Description

Display format of the clock will be (M:SS:T): minutes (M) on one LED display, seconds (SS) on two LED displays and tenth of second (T) on one LED display. Refer to the format above. The task is to design and implement the following modules: 1. Use the 4-digit seven segment display created in the last assignment as a component (modify incrementally if required) 2. Create a stopwatch and display it on the board

Stopwatch

In order to divide the onboard 100Mhz clock we make two counter signals, “counter” and “counter2”

- counter2 is updated on each rising edge of the clock
- counter is updated whenever counter2 reaches 10000000, essentially counter is updated at every one tenth of a second

Now using the counter signal we determine the time in the required format. Let’s denote m as minutes, s1*10 + s2 as the seconds and t as tenth of a second

We calculated the value of these output as follows:

```
temp <= counter mod 600;
m  <= std_logic_vector(to_unsigned(counter/600, 4));
temp1 <= counter mod 600;
t <= std_logic_vector(to_unsigned(temp1 mod 10, 4));
temp2 <= temp1/10;
s2 <= std_logic_vector(to_unsigned(temp2 mod 10, 4));
temp3 <= temp2/10;
s1 <= std_logic_vector(to_unsigned(temp3 mod 10, 4));
end process;
```

where temp1, temp2, temp3 are signals to store temporary values

The watch is controlled using four switches on the board. These are implemented using a process on start, pause, continue and reset

```
process(start, pause, continue,reset)

begin


    if (start = '1' ) then
        enable_watch <= '1';


    end if ;
```

```
    if ( pause = '1') then

            ispause <= '1';

    end if;

    if ( continue = '1') then

                ispause <= '0';

    end if;

    if (reset = '1' and reset_watch ='1') then

    enable_watch <= '0' ;
    ispause <= '0' ;
    end if ;


end process;
```

On switching start on, enable_watch is set to 1 and the clock starts. On switching pause on, is_pause is set to 1 and the clock stops (refer the condition for clock increment below). On switching continue on, is_pause is set to 0 again and the clock starts again. Note that switching start on again wont start the clock as enable_watch will still be 1, but is_pause will still be 1.

On switching reset on, clock is reset to 0 by setting counter = 0, and reset_watch is set to 1. The above process on start,pause,continue,reset is called as reset changes, and then enable_watch and is_pause are both set to 0. Thus reset dominates all the other switches. This stops the clock. When reset is switched down, then reset_watch is set to 0 so that next time the clock can be reset again. After switching reset on, to start the clock again we have to switch start on again so that enable_watch is set to 1. Thus our design meets the assignment specifications.

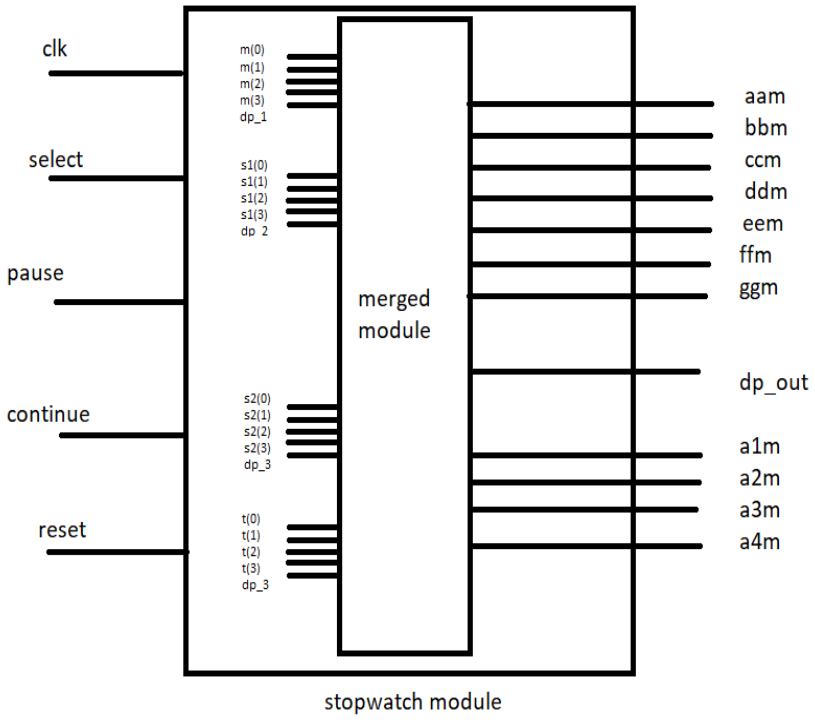
C:/Users/Ashu Jain/Downloads/stopwatch.vhd

```
160 process(clk, reset)
161 begin
162
163
164     if (clk'event and clk = '1' and enable_watch = '1' and ispause = '0' ) then
165     counter2 <= counter2 + 1;
166     if counter2 = 10000000 then
167         counter <= counter + 1;
168         counter2 <= 0;
169     end if;
170     end if;
171     if (reset = '1' and reset_watch = '0') then
172         counter <= 0;
173         reset_watch <= '1';
174
175     end if;
176     if (reset = '0' and reset_watch = '1') then
177         reset_watch <= '0';
178     end if;
179
180 end process;
181
```

This mainly concludes the working of our stopwatch module. After this we connect this to our assignment1 module(after modifying it a bit to display the decimal points also) called merged to output the display of our stopwatch on the 7 segment display. The way we do this is by importing merged of assignment1 as a component inside our stopwatch module and mapping the corresponding ports.

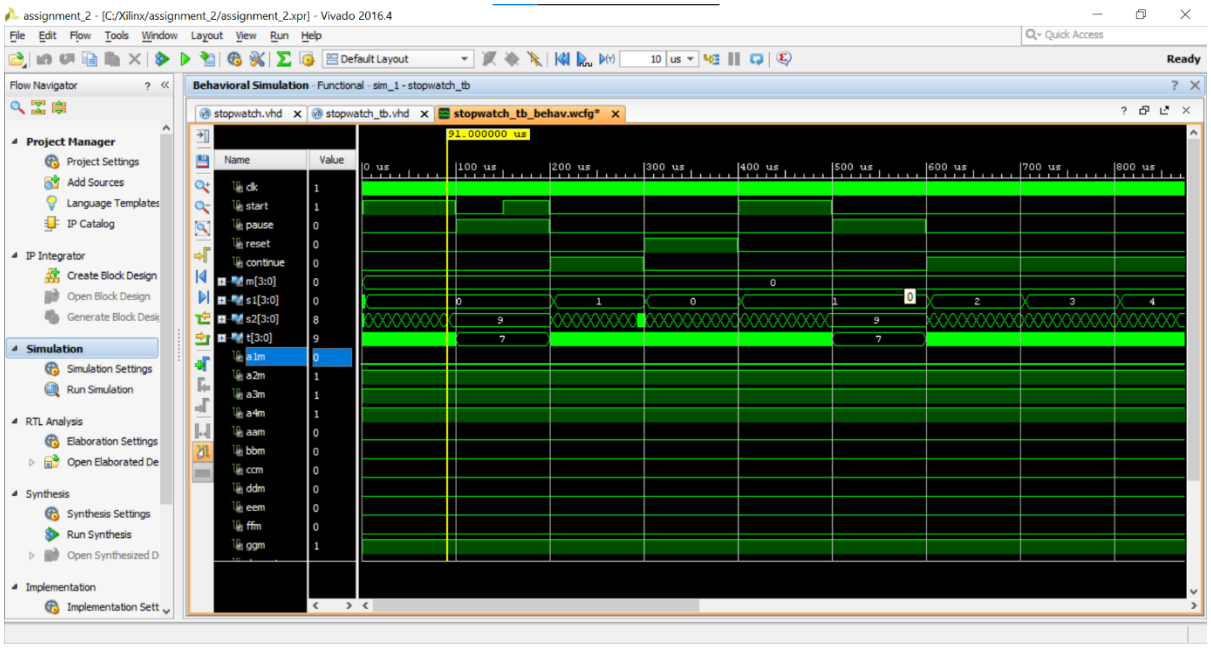
The block diagram of the modules in our code is as follows:

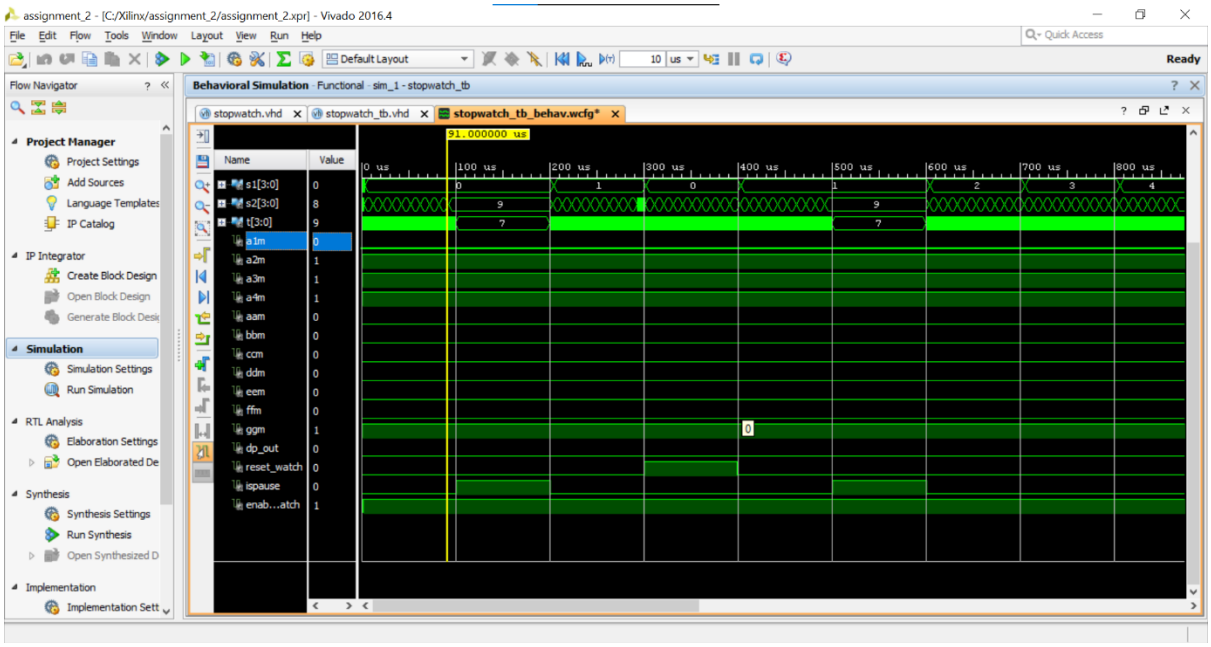
Here t,s2,s1,m are std_logic vectors referring to tenth of a second, second, ten second and minute digits of the stopwatch respectively. aam, bbm,ccm,ddm,eem,ffm,ggm are the cathode output signals and a1m,a2m,a3m,a4m are the output anode signals. dp_1,dp_2,dp_3,dp_4 are the decimal point inputs to the merged module. dp_out is the decimal point output signal. clk is the inbuilt clock input to the stopwatch module, and it is also an input to the merged module(not shown in block diagram). Finally, start, continue, pause, reset are the switch inputs as specified in the problem statement.

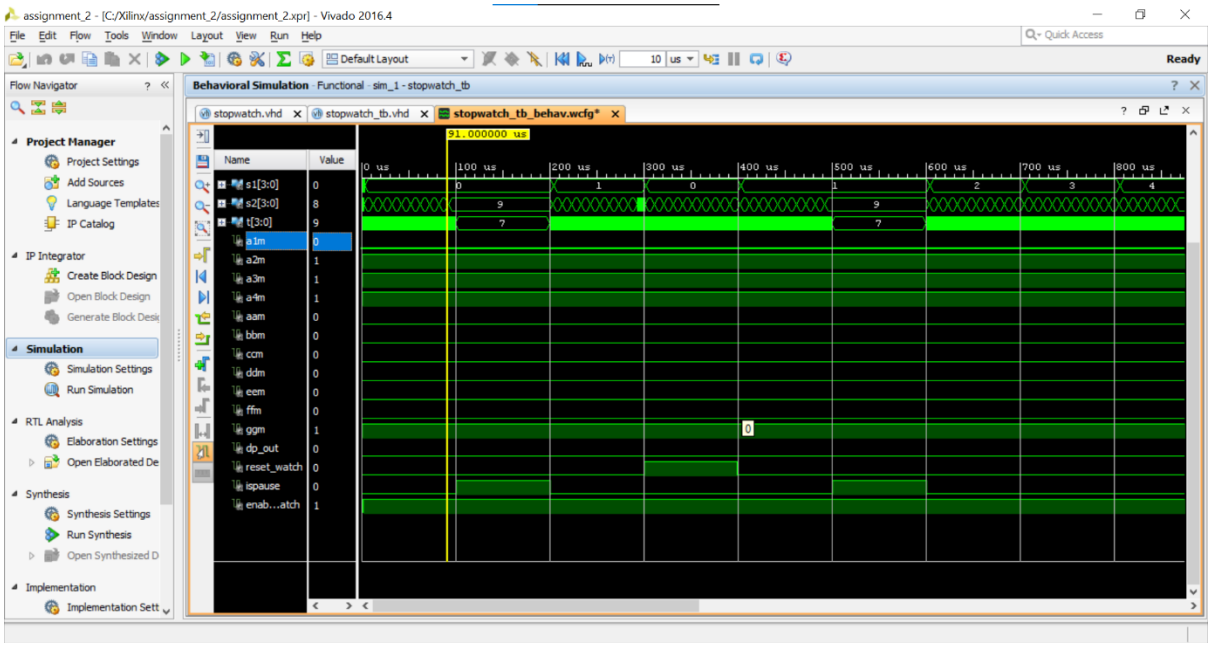


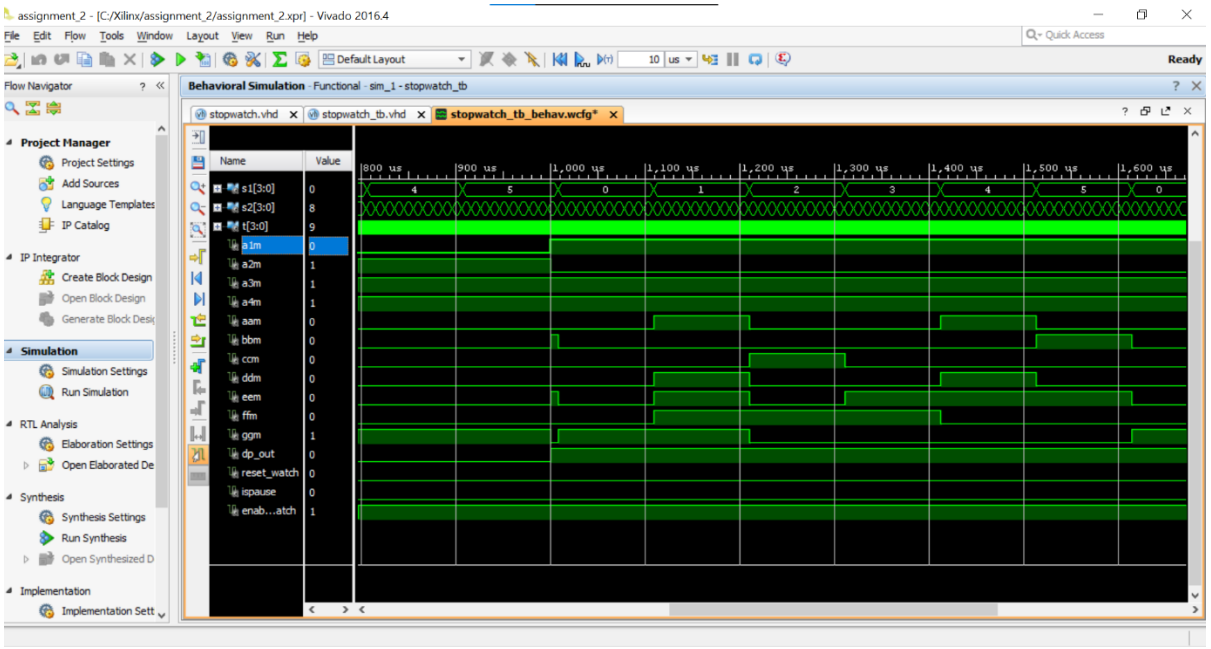
Simulation

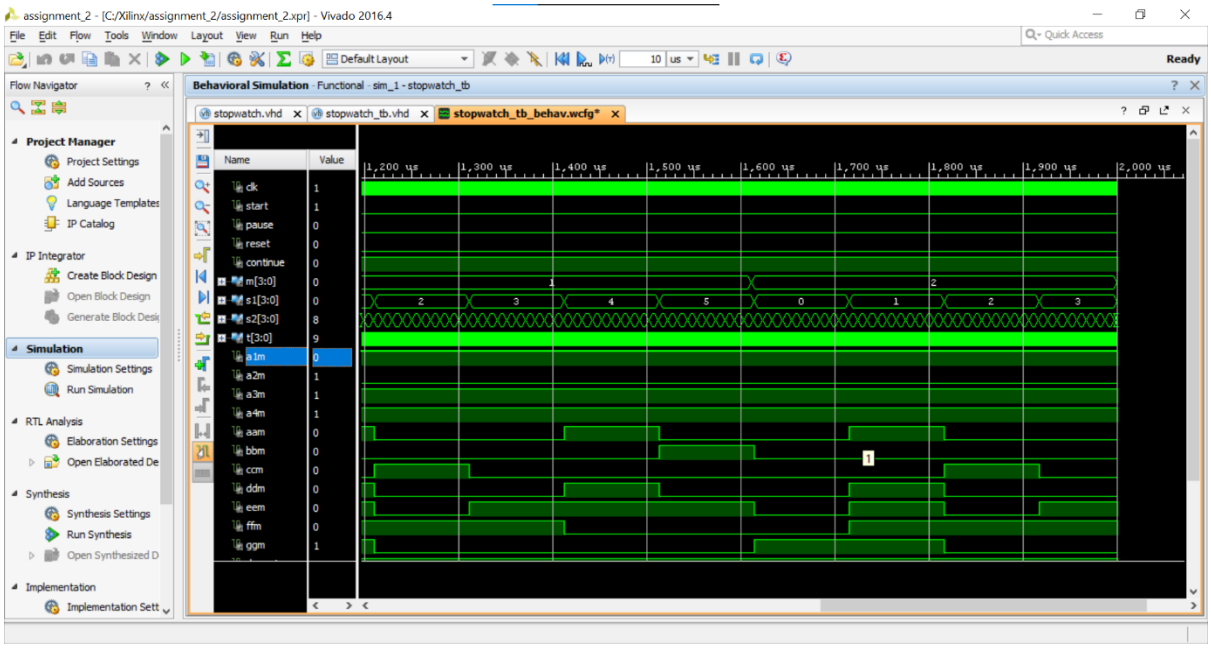
For the purpose of simulation we have scaled down the frequency with which counter updates to 100 from 10000000

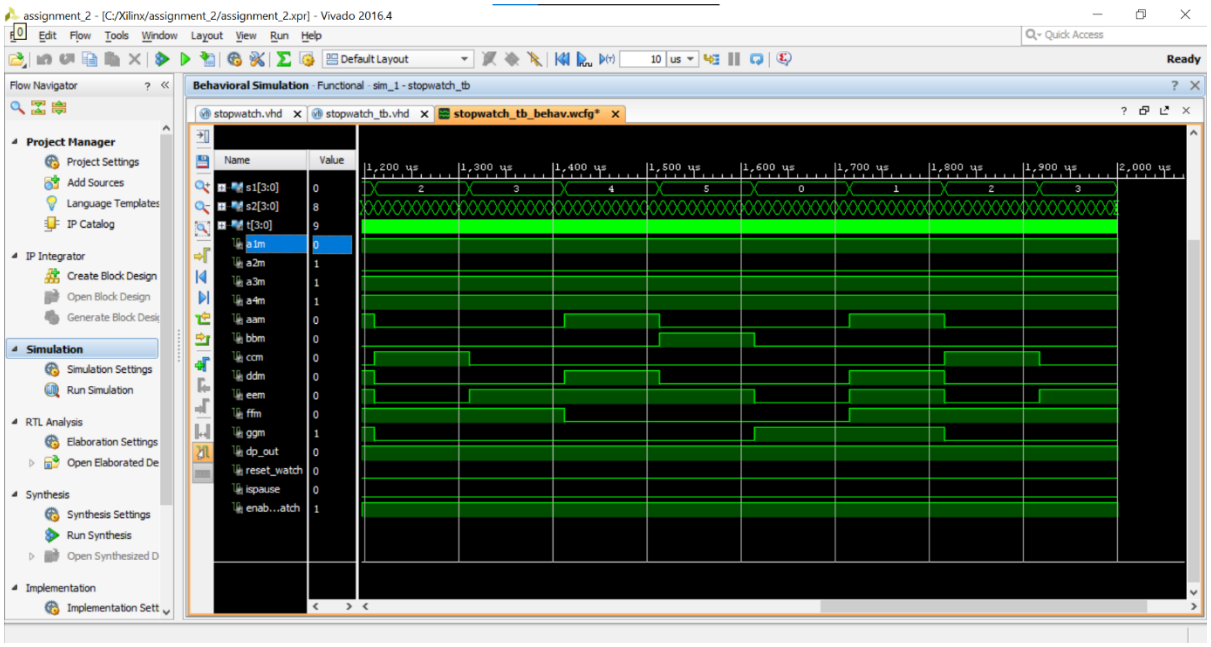

assignment_2 - [C:/Xilinx/assignment_2/assignment_2.xpr] - Vivado 2016.4
File Edit Flow Tools Window Layout View Run Help
Quick Access
Default Layout
Ready
Flow Navigator
Project Manager
Project Settings
Add Sources
Language Templates
IP Catalog
IP Integrator
Create Block Design
Open Block Design
Generate Block Desi
Simulation
Simulation Settings
Run Simulation
RTL Analysis
Elaboration Settings
Open Elaborated De
Synthesis
Synthesis Settings
Run Synthesis
Open Synthesized D
Implementation
Implementation Sett
Behavioral Simulation - Functional - sim_1 - stopwatch_tb
stopwatch.vhd
stopwatch_tb.vhd
stopwatch_tb_behav.wcfg*
91.000000 us
Name
Value
clk
start
pause
reset
continue
m[3:0]
s1[3:0]
s2[3:0]
t[3:0]
a1m
a2m
a3m
a4m
aam
bbm
ccm
ddm
eem
ffm
ggm
0 us
100 us
200 us
300 us
400 us
500 us
600 us
700 us
800 us


assignment_2 - [C:/Xilinx/assignment_2/assignment_2.xpr] - Vivado 2016.4
File Edit Flow Tools Window Layout View Run Help
Quick Access
Default Layout
Ready
Flow Navigator
Project Manager
Project Settings
Add Sources
Language Templates
IP Catalog
IP Integrator
Create Block Design
Open Block Design
Generate Block Desi
Simulation
Simulation Settings
Run Simulation
RTL Analysis
Elaboration Settings
Open Elaborated De
Synthesis
Synthesis Settings
Run Synthesis
Open Synthesized D
Implementation
Implementation Sett
Behavioral Simulation - Functional - sim_1 - stopwatch_tb
stopwatch.vhd
stopwatch_tb.vhd
stopwatch_tb_behav.wcfg*
91.000000 us
Name
Value
s1[3:0]
s2[3:0]
t[3:0]
a1m
a2m
a3m
a4m
aam
bbm
ccm
ddm
eem
ffm
ggm
dp_out
reset_watch
ispause
enab...atch
0 us
100 us
200 us
300 us
400 us
500 us
600 us
700 us
800 us


assignment_2 - [C:/Xilinx/assignment_2/assignment_2.xpr] - Vivado 2016.4
File Edit Flow Tools Window Layout View Run Help
Quick Access
Default Layout
Ready
Flow Navigator
Project Manager
Project Settings
Add Sources
Language Templates
IP Catalog
IP Integrator
Create Block Design
Open Block Design
Simulation
Simulation Settings
Run Simulation
RTL Analysis
Elaboration Settings
Synthesis
Synthesis Settings
Run Synthesis
Implementation
Implementation Sett
Behavioral Simulation - Functional - sim_1 - stopwatch_tb
stopwatch.vhd
stopwatch_tb.vhd
stopwatch_tb_behav.wcfg*
91.000000 us
Name
Value
s1[3:0]
s2[3:0]
t[3:0]
a1m
a2m
a3m
a4m
aam
bbm
ccm
ddm
eem
ffm
ggm
dp_out
reset_watch
ispause
enab...atch
0 us
100 us
200 us
300 us
400 us
500 us
600 us
700 us
800 us


assignment_2 - [C:/Xilinx/assignment_2/assignment_2.xpr] - Vivado 2016.4
File Edit Flow Tools Window Layout View Run Help
Quick Access
Default Layout
Ready
Flow Navigator
Project Manager
Project Settings
Add Sources
Language Templates
IP Catalog
IP Integrator
Create Block Design
Open Block Design
Simulation
Simulation Settings
Run Simulation
RTL Analysis
Elaboration Settings
Synthesis
Synthesis Settings
Run Synthesis
Implementation
Implementation Sett
Behavioral Simulation - Functional - sim_1 - stopwatch_tb
stopwatch.vhd
stopwatch_tb.vhd
stopwatch_tb_behav.wcfg*
Name
Value
s1[3:0]
s2[3:0]
t[3:0]
a1m
a2m
a3m
a4m
aam
bbm
ccm
ddm
eem
ffm
ggm
dp_out
reset_watch
ispause
enab...atch
800 us
900 us
1,000 us
1,100 us
1,200 us
1,300 us
1,400 us
1,500 us
1,600 us





Synthesis Report

Synthesis(utilization) report (BRAM, LUT, DSP, Flip flops highlighted on next page)

```
Copyright 1986-2016 Xilinx, Inc. All Rights Reserved.
----------------------------------------------------------------------------------
| Tool Version : Vivado v.2016.4 (win64) Build 1756540 Mon Jan 23 19:11:23
MST 2017
| Date         : Sun Oct 30 17:12:53 2022
| Host         : LAPTOP-867JO11Q running 64-bit major release  (build 9200)
| Command      : report_utilization -file stopwatch_utilization_synth.rpt -
pb stopwatch_utilization_synth.pb
```

| Design : stopwatch
| Device : 7a35tcpg236-1
| Design State : Synthesized

Utilization Design Information

Table of Contents
----

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	2494	0	20800	11.99
LUT as Logic	2494	0	20800	11.99
LUT as Memory	0	0	9600	0.00
Slice Registers	137	0	41600	0.33
Register as Flip Flop	128	0	41600	0.31
Register as Latch	9	0	41600	0.02
F7 Muxes	0	0	16300	0.00
F8 Muxes	0	0	8150	0.00

* Warning! The Final LUT count, after physical optimizations and full implementation, is typically lower. Run opt_design after synthesis, if not already completed, for a more realistic count.

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
3	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
2	Yes	-	Set
36	Yes	-	Reset
0	Yes	Set	-
96	Yes	Reset	-

2. Memory

Site Type	Used	Fixed	Available	Util%
Block RAM Tile	0	0	50	0.00
RAMB36/FIFO*	0	0	50	0.00
RAMB18	0	0	100	0.00

* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E1

3. DSP

Site Type	Used	Fixed	Available	Util%
DSPs	0	0	90	0.00

4. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	17	0	106	16.04
Bonded IPADs	0	0	10	0.00
Bonded OPADs	0	0	4	0.00
PHY_CONTROL	0	0	5	0.00
PHASER_REF	0	0	5	0.00
OUT_FIFO	0	0	20	0.00
IN_FIFO	0	0	20	0.00
IDELAYCTRL	0	0	5	0.00
IBUFDS	0	0	104	0.00
GTPE2_CHANNEL	0	0	2	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	20	0.00
PHASER_IN/PHASER_IN_PHY	0	0	20	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	250	0.00
IBUFDS_GTE2	0	0	2	0.00
ILOGIC	0	0	106	0.00
OLOGIC	0	0	106	0.00

5. Clocking

Site Type	Used	Fixed	Available	Util%
BUFGCTRL	4	0	32	12.50
BUFIO	0	0	20	0.00
MMCME2_ADV	0	0	5	0.00
PLLE2_ADV	0	0	5	0.00
BUFMRCE	0	0	10	0.00
BUFHCE	0	0	72	0.00

BUFR	0	0	20	0.00

6. Specific Feature

Site Type	Used	Fixed	Available	Util%
BSCANE2	0	0	4	0.00
CAPTUREE2	0	0	1	0.00
DNA_PORT	0	0	1	0.00
EFUSE_USR	0	0	1	0.00
FRAME_ECCE2	0	0	1	0.00
ICAPE2	0	0	2	0.00
PCIE_2_1	0	0	1	0.00
STARTUPE2	0	0	1	0.00
XADC	0	0	1	0.00

7. Primitives

Ref Name	Used	Functional Category
LUT6	804	LUT
LUT3	670	LUT
LUT4	487	LUT
LUT5	452	LUT
CARRY4	447	CarryLogic
LUT2	324	LUT
LUT1	262	LUT
FDRE	96	Flop & Latch
FDCE	32	Flop & Latch
OBUF	12	IO
LDCE	7	Flop & Latch
IBUF	5	IO
BUFG	4	Clock
LDPE	2	Flop & Latch

8. Black Boxes

Ref Name	Used

9. Instantiated Netlists

Ref Name	Used

Complete Vivado synthesis report

```
#-----------------------------------------------------------
# Vivado v2016.4 (64-bit)
# SW Build 1756540 on Mon Jan 23 19:11:23 MST 2017
# IP Build 1755317 on Mon Jan 23 20:30:07 MST 2017
# Start of session at: Sun Oct 30 17:12:13 2022
# Process ID: 4208
# Current directory: C:/Xilinx/assignment_2/assignment_2.runs/synth_1
# Command line: vivado.exe -log stopwatch.vds -product Vivado -mode batch -
messageDb vivado.pb -notrace -source stopwatch.tcl
# Log file: C:/Xilinx/assignment_2/assignment_2.runs/synth_1/stopwatch.vds
# Journal file: C:/Xilinx/assignment_2/assignment_2.runs/synth_1\vivado.jou
#-----------------------------------------------------------
source stopwatch.tcl -notrace
Command: synth_design -top stopwatch -part xc7a35tcpg236-1
Starting synth_design
Attempting to get a license for feature 'Synthesis' and/or device 'xc7a35t'
INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device
'xc7a35t'
INFO: Launching helper process for spawning children vivado processes
INFO: Helper process launched with PID 29392
---------------------------------------------------------------------------
------
Starting RTL Elaboration : Time (s): cpu = 00:00:03 ; elapsed = 00:00:09 .
Memory (MB): peak = 282.836 ; gain = 73.348
---------------------------------------------------------------------------
------
INFO: [Synth 8-638] synthesizing module 'stopwatch' [C:/Users/Ashu
Jain/Downloads/stopwatch.vhd:62]
INFO: [Synth 8-3491] module 'merged' declared at 'C:/Users/Ashu
Jain/Downloads/merged.vhd:34' bound to instance 'uut' of component 'merged'
[C:/Users/Ashu Jain/Downloads/stopwatch.vhd:123]
INFO: [Synth 8-638] synthesizing module 'merged' [C:/Users/Ashu
Jain/Downloads/merged.vhd:77]
INFO: [Synth 8-3491] module 'clock_divider' declared at 'C:/Users/Ashu
Jain/Downloads/clock_divider.vhd:34' bound to instance 'u0' of component
'clock_divider' [C:/Users/Ashu Jain/Downloads/merged.vhd:163]
INFO: [Synth 8-638] synthesizing module 'clock_divider' [C:/Users/Ashu
Jain/Downloads/clock_divider.vhd:46]
INFO: [Synth 8-256] done synthesizing module 'clock_divider' (1#1)
[C:/Users/Ashu Jain/Downloads/clock_divider.vhd:46]
INFO: [Synth 8-3491] module 'MUX' declared at 'C:/Users/Ashu
Jain/Downloads/MUX.vhd:34' bound to instance 'u1' of component 'MUX'
[C:/Users/Ashu Jain/Downloads/merged.vhd:175]
INFO: [Synth 8-638] synthesizing module 'MUX' [C:/Users/Ashu
Jain/Downloads/MUX.vhd:73]
INFO: [Synth 8-256] done synthesizing module 'MUX' (2#1) [C:/Users/Ashu
Jain/Downloads/MUX.vhd:73]
INFO: [Synth 8-3491] module 'decoder' declared at 'C:/Users/Ashu
Jain/Downloads/decoder.vhd:42' bound to instance 'u2' of component
'decoder' [C:/Users/Ashu Jain/Downloads/merged.vhd:213]
INFO: [Synth 8-638] synthesizing module 'decoder' [C:/Users/Ashu
Jain/Downloads/decoder.vhd:66]
INFO: [Synth 8-256] done synthesizing module 'decoder' (3#1) [C:/Users/Ashu
Jain/Downloads/decoder.vhd:66]
INFO: [Synth 8-256] done synthesizing module 'merged' (4#1) [C:/Users/Ashu
Jain/Downloads/merged.vhd:77]
WARNING: [Synth 8-614] signal 'reset_watch' is read in the process but is
not in the sensitivity list [C:/Users/Ashu
Jain/Downloads/stopwatch.vhd:132]
```

```
WARNING: [Synth 8-614] signal 'ispause' is read in the process but is not
in the sensitivity list [C:/Users/Ashu Jain/Downloads/stopwatch.vhd:160]
WARNING: [Synth 8-614] signal 'enable_watch' is read in the process but is
not in the sensitivity list [C:/Users/Ashu
Jain/Downloads/stopwatch.vhd:160]
WARNING: [Synth 8-614] signal 'reset_watch' is read in the process but is
not in the sensitivity list [C:/Users/Ashu
Jain/Downloads/stopwatch.vhd:160]
WARNING: [Synth 8-614] signal 'temp1' is read in the process but is not in
the sensitivity list [C:/Users/Ashu Jain/Downloads/stopwatch.vhd:189]
WARNING: [Synth 8-614] signal 'temp2' is read in the process but is not in
the sensitivity list [C:/Users/Ashu Jain/Downloads/stopwatch.vhd:189]
WARNING: [Synth 8-614] signal 'temp3' is read in the process but is not in
the sensitivity list [C:/Users/Ashu Jain/Downloads/stopwatch.vhd:189]
INFO: [Synth 8-256] done synthesizing module 'stopwatch' (5#1)
[C:/Users/Ashu Jain/Downloads/stopwatch.vhd:62]
---------------------------------------------------------------------------
------
Finished RTL Elaboration : Time (s): cpu = 00:00:04 ; elapsed = 00:00:10 .
Memory (MB): peak = 320.219 ; gain = 110.730
---------------------------------------------------------------------------
------

Report Check Netlist:
+------+------------------+-------+---------+-------+------------------+
|      |Item              |Errors |Warnings |Status |Description       |
+------+------------------+-------+---------+-------+------------------+
|1     |multi_driven_nets |      0|        0|Passed |Multi driven nets |
+------+------------------+-------+---------+-------+------------------+
---------------------------------------------------------------------------
------
Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:04 ; elapsed =
00:00:10 . Memory (MB): peak = 320.219 ; gain = 110.730
---------------------------------------------------------------------------
------
INFO: [Device 21-403] Loading part xc7a35tcpg236-1
INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints
Initializing timing engine
Parsing XDC File [C:/Users/Ashu Jain/Downloads/basys3.xdc]
WARNING: [Vivado 12-507] No nets matched 'start_IBUF'. [C:/Users/Ashu
Jain/Downloads/basys3.xdc:11]
CRITICAL WARNING: [Common 17-55] 'set_property' expects at least one
object. [C:/Users/Ashu Jain/Downloads/basys3.xdc:11]
Resolution: If [get_<value>] was used to populate the object, check to make
sure this command returns at least one valid object.
WARNING: [Vivado 12-507] No nets matched 'pause_IBUF'. [C:/Users/Ashu
Jain/Downloads/basys3.xdc:12]
CRITICAL WARNING: [Common 17-55] 'set_property' expects at least one
object. [C:/Users/Ashu Jain/Downloads/basys3.xdc:12]
Resolution: If [get_<value>] was used to populate the object, check to make
sure this command returns at least one valid object.
WARNING: [Vivado 12-507] No nets matched 'continue_IBUF'. [C:/Users/Ashu
Jain/Downloads/basys3.xdc:13]
CRITICAL WARNING: [Common 17-55] 'set_property' expects at least one
object. [C:/Users/Ashu Jain/Downloads/basys3.xdc:13]
Resolution: If [get_<value>] was used to populate the object, check to make
sure this command returns at least one valid object.
WARNING: [Vivado 12-507] No nets matched 'reset_IBUF'. [C:/Users/Ashu
Jain/Downloads/basys3.xdc:14]
```

```
CRITICAL WARNING: [Common 17-55] 'set_property' expects at least one
object. [C:/Users/Ashu Jain/Downloads/basys3.xdc:14]
Resolution: If [get_<value>] was used to populate the object, check to make
sure this command returns at least one valid object.
Finished Parsing XDC File [C:/Users/Ashu Jain/Downloads/basys3.xdc]
INFO: [Project 1-236] Implementation specific constraints were found while
reading constraint file [C:/Users/Ashu Jain/Downloads/basys3.xdc]. These
constraints will be ignored for synthesis but will be used in
implementation. Impacted constraints are listed in the file
[.Xil/stopwatch_propImpl.xdc].
Resolution: To avoid this warning, move constraints listed in
[.Xil/stopwatch_propImpl.xdc] to another XDC file and exclude this new file
from synthesis with the used_in_synthesis property (File Properties dialog
in GUI) and re-run elaboration/synthesis.
Completed Processing XDC Constraints

INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed =
00:00:00.003 . Memory (MB): peak = 618.090 ; gain = 0.000
-----------------------------------------------------------------------
------
Finished Constraint Validation : Time (s): cpu = 00:00:10 ; elapsed =
00:00:18 . Memory (MB): peak = 618.090 ; gain = 408.602
-----------------------------------------------------------------------
------
-----------------------------------------------------------------------
------
Start Loading Part and Timing Information
-----------------------------------------------------------------------
------
Loading part: xc7a35tcpg236-1
-----------------------------------------------------------------------
------
Finished Loading Part and Timing Information : Time (s): cpu = 00:00:10 ;
elapsed = 00:00:18 . Memory (MB): peak = 618.090 ; gain = 408.602
-----------------------------------------------------------------------
------
-----------------------------------------------------------------------
------
Start Applying 'set_property' XDC Constraints
-----------------------------------------------------------------------
------
-----------------------------------------------------------------------
------
Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:11
; elapsed = 00:00:18 . Memory (MB): peak = 618.090 ; gain = 408.602
-----------------------------------------------------------------------
------
INFO: [Synth 8-5545] ROM "s1" won't be mapped to RAM because address size
(32) is larger than maximum supported(25)
INFO: [Synth 8-5545] ROM "s1" won't be mapped to RAM because address size
(32) is larger than maximum supported(25)
INFO: [Synth 8-5545] ROM "s2" won't be mapped to RAM because address size
(32) is larger than maximum supported(25)
INFO: [Synth 8-5545] ROM "a1" won't be mapped to RAM because address size
(32) is larger than maximum supported(25)
INFO: [Synth 8-5545] ROM "a2" won't be mapped to RAM because address size
(32) is larger than maximum supported(25)
```

```
INFO: [Synth 8-5545] ROM "a4" won't be mapped to RAM because address size
(32) is larger than maximum supported(25)
INFO: [Synth 8-5545] ROM "i5m1" won't be mapped to RAM because address size
(32) is larger than maximum supported(25)
INFO: [Synth 8-5545] ROM "temp11" won't be mapped to RAM because address
size (32) is larger than maximum supported(25)
INFO: [Synth 8-5545] ROM "i9m1" won't be mapped to RAM because address size
(32) is larger than maximum supported(25)
INFO: [Synth 8-5545] ROM "i13m1" won't be mapped to RAM because address
size (32) is larger than maximum supported(25)
INFO: [Synth 8-5545] ROM "counter2" won't be mapped to RAM because address
size (32) is larger than maximum supported(25)
INFO: [Synth 8-5545] ROM "counter" won't be mapped to RAM because address
size (32) is larger than maximum supported(25)
WARNING: [Synth 8-327] inferring latch for variable 's1_reg' [C:/Users/Ashu
Jain/Downloads/clock_divider.vhd:55]
WARNING: [Synth 8-327] inferring latch for variable 's2_reg' [C:/Users/Ashu
Jain/Downloads/clock_divider.vhd:56]
WARNING: [Synth 8-327] inferring latch for variable 'a1_reg' [C:/Users/Ashu
Jain/Downloads/clock_divider.vhd:57]
WARNING: [Synth 8-327] inferring latch for variable 'a2_reg' [C:/Users/Ashu
Jain/Downloads/clock_divider.vhd:57]
WARNING: [Synth 8-327] inferring latch for variable 'a3_reg' [C:/Users/Ashu
Jain/Downloads/clock_divider.vhd:57]
WARNING: [Synth 8-327] inferring latch for variable 'a4_reg' [C:/Users/Ashu
Jain/Downloads/clock_divider.vhd:57]
WARNING: [Synth 8-327] inferring latch for variable 'ispause_reg'
[C:/Users/Ashu Jain/Downloads/stopwatch.vhd:143]
WARNING: [Synth 8-327] inferring latch for variable 'enable_watch_reg'
[C:/Users/Ashu Jain/Downloads/stopwatch.vhd:139]
WARNING: [Synth 8-327] inferring latch for variable 'reset_watch_reg'
[C:/Users/Ashu Jain/Downloads/stopwatch.vhd:176]
---------------------------------------------------------------------------
------
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:11 ; elapsed =
00:00:19 . Memory (MB): peak = 618.090 ; gain = 408.602
---------------------------------------------------------------------------
------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------
------
Start RTL Component Statistics
---------------------------------------------------------------------------
------
Detailed RTL Component Info :
+---Adders :
           2 Input     32 Bit       Adders := 3
           2 Input     31 Bit       Adders := 4
           2 Input     11 Bit       Adders := 1
           2 Input      4 Bit       Adders := 4
+---Registers :
                       32 Bit    Registers := 1
+---Muxes :
           2 Input     32 Bit        Muxes := 3
           2 Input     31 Bit        Muxes := 4
           2 Input     11 Bit        Muxes := 2
```

```
           2 Input      4 Bit        Muxes := 7
           2 Input      1 Bit        Muxes := 8
           3 Input      1 Bit        Muxes := 3
------------------------------------------------------------------------------
------
Finished RTL Component Statistics
------------------------------------------------------------------------------
------
------------------------------------------------------------------------------
------
Start RTL Hierarchical Component Statistics
------------------------------------------------------------------------------
------
Hierarchical RTL Component report
Module stopwatch
Detailed RTL Component Info :
+---Adders :
           2 Input     32 Bit       Adders := 3
           2 Input     31 Bit       Adders := 4
           2 Input     11 Bit       Adders := 1
           2 Input      4 Bit       Adders := 4
+---Registers :
                      32 Bit    Registers := 1
+---Muxes :
           2 Input     32 Bit        Muxes := 3
           2 Input     31 Bit        Muxes := 4
           2 Input     11 Bit        Muxes := 2
           2 Input      4 Bit        Muxes := 7
           2 Input      1 Bit        Muxes := 2
Module clock_divider
Detailed RTL Component Info :
+---Muxes :
           2 Input      1 Bit        Muxes := 6
           3 Input      1 Bit        Muxes := 3
------------------------------------------------------------------------------
------
Finished RTL Hierarchical Component Statistics
------------------------------------------------------------------------------
------
------------------------------------------------------------------------------
------
Start Part Resource Summary
------------------------------------------------------------------------------
------
Part Resources:
DSPs: 90 (col length:60)
BRAMs: 100 (col length: RAMB18 60 RAMB36 30)
------------------------------------------------------------------------------
------
Finished Part Resource Summary
------------------------------------------------------------------------------
------
------------------------------------------------------------------------------
------
Start Cross Boundary and Area Optimization
------------------------------------------------------------------------------
------
INFO: [Synth 8-5545] ROM "u0/s1" won't be mapped to RAM because address
size (32) is larger than maximum supported(25)
INFO: [Synth 8-5545] ROM "AS0" won't be mapped to RAM because address size
(32) is larger than maximum supported(25)
```

```
INFO: [Synth 8-5545] ROM "u0/s1" won't be mapped to RAM because address
size (32) is larger than maximum supported(25)
INFO: [Synth 8-5545] ROM "O30" won't be mapped to RAM because address size
(32) is larger than maximum supported(25)
INFO: [Synth 8-5545] ROM "u0/s2" won't be mapped to RAM because address
size (32) is larger than maximum supported(25)
INFO: [Synth 8-5545] ROM "u0/a1" won't be mapped to RAM because address
size (32) is larger than maximum supported(25)
INFO: [Synth 8-5545] ROM "u0/a2" won't be mapped to RAM because address
size (32) is larger than maximum supported(25)
INFO: [Synth 8-5545] ROM "u0/a4" won't be mapped to RAM because address
size (32) is larger than maximum supported(25)
INFO: [Synth 8-5545] ROM "counter2" won't be mapped to RAM because address
size (32) is larger than maximum supported(25)
INFO: [Synth 8-5545] ROM "counter" won't be mapped to RAM because address
size (32) is larger than maximum supported(25)
INFO: [Synth 8-5545] ROM "temp11" won't be mapped to RAM because address
size (32) is larger than maximum supported(25)
INFO: [Synth 8-5545] ROM "i5m1" won't be mapped to RAM because address size
(32) is larger than maximum supported(25)
INFO: [Synth 8-5545] ROM "i9m1" won't be mapped to RAM because address size
(32) is larger than maximum supported(25)
INFO: [Synth 8-5545] ROM "i13m1" won't be mapped to RAM because address
size (32) is larger than maximum supported(25)
------------------------------------------------------------------------
------
Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:18 ;
elapsed = 00:00:25 . Memory (MB): peak = 618.090 ; gain = 408.602
------------------------------------------------------------------------
------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
------------------------------------------------------------------------
------
Start Timing Optimization
------------------------------------------------------------------------
------
------------------------------------------------------------------------
------
Start Applying XDC Timing Constraints
------------------------------------------------------------------------
------
------------------------------------------------------------------------
------
Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:25 ;
elapsed = 00:00:33 . Memory (MB): peak = 629.656 ; gain = 420.168
------------------------------------------------------------------------
------
------------------------------------------------------------------------
------
Finished Timing Optimization : Time (s): cpu = 00:00:25 ; elapsed =
00:00:34 . Memory (MB): peak = 642.629 ; gain = 433.141
------------------------------------------------------------------------
------

Report RTL Partitions:
+-+--------------+------------+----------+
```

```
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
-------------------------------------------------------------------------------
------
Start Technology Mapping
-------------------------------------------------------------------------------
------
-------------------------------------------------------------------------------
------
Finished Technology Mapping : Time (s): cpu = 00:00:26 ; elapsed = 00:00:35
. Memory (MB): peak = 712.438 ; gain = 502.949
-------------------------------------------------------------------------------
------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
-------------------------------------------------------------------------------
------
Start IO Insertion
-------------------------------------------------------------------------------
------
-------------------------------------------------------------------------------
------
Start Flattening Before IO Insertion
-------------------------------------------------------------------------------
------
-------------------------------------------------------------------------------
------
Finished Flattening Before IO Insertion
-------------------------------------------------------------------------------
------
-------------------------------------------------------------------------------
------
Start Final Netlist Cleanup
-------------------------------------------------------------------------------
------
-------------------------------------------------------------------------------
------
Finished Final Netlist Cleanup
-------------------------------------------------------------------------------
------
-------------------------------------------------------------------------------
------
Finished IO Insertion : Time (s): cpu = 00:00:27 ; elapsed = 00:00:35 .
Memory (MB): peak = 712.438 ; gain = 502.949
-------------------------------------------------------------------------------
------

Report Check Netlist:
+------+------------------+-------+---------+-------+------------------+
|      |Item              |Errors |Warnings |Status |Description       |
+------+------------------+-------+---------+-------+------------------+
|1     |multi_driven_nets |      0|        0|Passed |Multi driven nets |
+------+------------------+-------+---------+-------+------------------+
-------------------------------------------------------------------------------
------
Start Renaming Generated Instances
```

```
---------------------------------------------------------------------------
------
---------------------------------------------------------------------------
------
Finished Renaming Generated Instances : Time (s): cpu = 00:00:27 ; elapsed
= 00:00:35 . Memory (MB): peak = 712.438 ; gain = 502.949
---------------------------------------------------------------------------
------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------
------
Start Rebuilding User Hierarchy
---------------------------------------------------------------------------
------
---------------------------------------------------------------------------
------
Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:27 ; elapsed =
00:00:36 . Memory (MB): peak = 712.438 ; gain = 502.949
---------------------------------------------------------------------------
------
---------------------------------------------------------------------------
------
Start Renaming Generated Ports
---------------------------------------------------------------------------
------
---------------------------------------------------------------------------
------
Finished Renaming Generated Ports : Time (s): cpu = 00:00:27 ; elapsed =
00:00:36 . Memory (MB): peak = 712.438 ; gain = 502.949
---------------------------------------------------------------------------
------
---------------------------------------------------------------------------
------
Start Handling Custom Attributes
---------------------------------------------------------------------------
------
---------------------------------------------------------------------------
------
Finished Handling Custom Attributes : Time (s): cpu = 00:00:27 ; elapsed =
00:00:36 . Memory (MB): peak = 712.438 ; gain = 502.949
---------------------------------------------------------------------------
------
---------------------------------------------------------------------------
------
Start Renaming Generated Nets
---------------------------------------------------------------------------
------
---------------------------------------------------------------------------
------
Finished Renaming Generated Nets : Time (s): cpu = 00:00:27 ; elapsed =
00:00:36 . Memory (MB): peak = 712.438 ; gain = 502.949
---------------------------------------------------------------------------
------
---------------------------------------------------------------------------
------
Start Writing Synthesis Report
```

```
------------------------------------------------------------------------------
------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-------+------+
|      |Cell   |Count |
+------+-------+------+
|1     |BUFG   |     4|
|2     |CARRY4 |   447|
|3     |LUT1   |   262|
|4     |LUT2   |   324|
|5     |LUT3   |   664|
|6     |LUT4   |   487|
|7     |LUT5   |   452|
|8     |LUT6   |   804|
|9     |FDCE   |    32|
|10    |FDRE   |    96|
|11    |LDC    |     4|
|12    |LDCP   |     3|
|13    |LDP    |     2|
|14    |IBUF   |     5|
|15    |OBUF   |    12|
+------+-------+------+

Report Instance Areas:
+------+---------+--------------+------+
|      |Instance |Module        |Cells |
+------+---------+--------------+------+
|1     |top      |              |  3598|
|2     |  uut    |merged        |   235|
|3     |    u0   |clock_divider |   235|
+------+---------+--------------+------+
------------------------------------------------------------------------------
------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:27 ; elapsed =
00:00:36 . Memory (MB): peak = 712.438 ; gain = 502.949
------------------------------------------------------------------------------
------
Synthesis finished with 0 errors, 0 critical warnings and 9 warnings.
Synthesis Optimization Runtime : Time (s): cpu = 00:00:19 ; elapsed =
00:00:25 . Memory (MB): peak = 712.438 ; gain = 205.078
Synthesis Optimization Complete : Time (s): cpu = 00:00:27 ; elapsed =
00:00:36 . Memory (MB): peak = 712.438 ; gain = 502.949
INFO: [Project 1-571] Translating synthesized netlist
INFO: [Netlist 29-17] Analyzing 461 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
WARNING: [Netlist 29-101] Netlist 'stopwatch' is not ideal for
floorplanning, since the cellview 'stopwatch' contains a large number of
primitives.  Please consider enabling hierarchy in synthesis if you want to
do floorplanning.
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
  A total of 9 instances were transformed.
  LDC => LDCE: 4 instances
```

```
  LDCP => LDCP (GND, LUT3, LUT3, LDCE, VCC): 3 instances
  LDP => LDPE: 2 instances

INFO: [Common 17-83] Releasing license: Synthesis
57 Infos, 21 Warnings, 4 Critical Warnings and 0 Errors encountered.
synth_design completed successfully
synth_design: Time (s): cpu = 00:00:28 ; elapsed = 00:00:32 . Memory (MB):
peak = 712.438 ; gain = 502.949
INFO: [Common 17-1381] The checkpoint
'C:/Xilinx/assignment_2/assignment_2.runs/synth_1/stopwatch.dcp' has been
generated.
report_utilization: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.026 .
Memory (MB): peak = 712.438 ; gain = 0.000
INFO: [Common 17-206] Exiting Vivado at Sun Oct 30 17:12:53 2022...
```