2EC601CC24 VLSI Design

Special Assignment

Topic : 1-Bit Serial Adder

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Submitted to:

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Abstract

- This project presents the design of a 1-bit serial adder using CMOS technology in Microwind. The 1-bit serial adder processes binary addition for single pairs of bits sequentially, using XOR and AND gates for sum and carry calculations, along with a flip-flop for carry storage. The design is optimized for low power and minimal area, making it ideal for compact digital applications

Keywords

- Serial Adder,CMOS,Full Adder,Flip Flop

Introduction

- In digital systems, addition is one of the fundamental operations used in many applications, like processors and signal processing. A 1-bit serial adder is a simple circuit that adds two single bits along with a carry bit. Unlike a parallel adder, which adds multiple bits at once, a serial adder processes bits one at a time, making it smaller in size and using less power. This makes it ideal for applications where we need to save space and power, especially in systems that don't require very high speeds
- The parallel adder performs addition quickly by adding all bits at once, but it has the drawback of needing a large amount of logic circuits
- In contrast, the serial adder performs binary addition one bit at a time. It uses a full adder circuit along with a D flip-flop.
- The flip-flop stores the carry from the current bit addition, allowing it to be used in the next bit's calculation.

Block Diagram

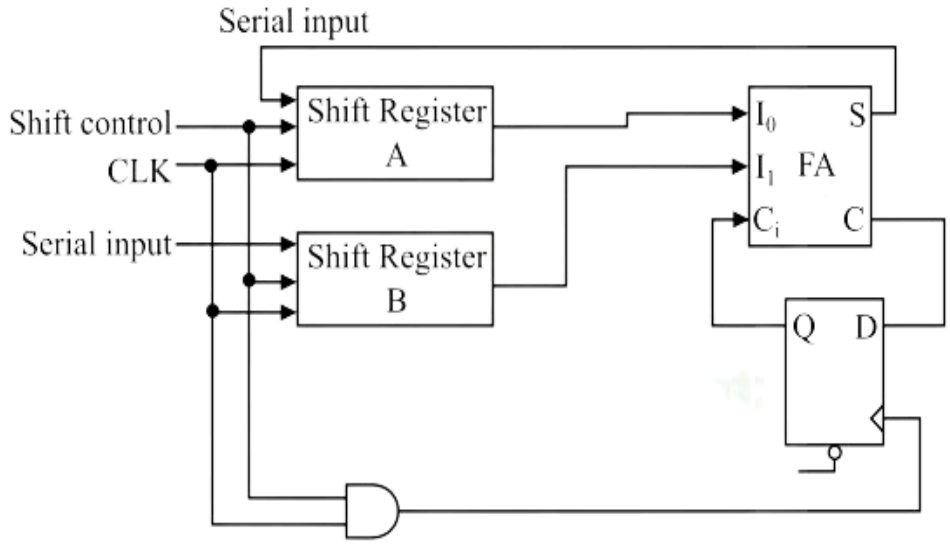


Figure 1 - Serial Binary Adder

- Shift Registers A and B: These registers hold the binary numbers to be added. Each clock cycle shifts one bit from each register to the full adder, allowing the addition to occur one bit at a time.
- Full Adder (FA): The full adder takes one bit from each register (A and B) and the carry bit from the previous addition cycle. It produces a sum (S) and a carry-out (C) bit.
- D Flip-Flop: The D flip-flop stores the carry-out from the full adder and feeds it back as the carry-in for the next bit addition. This ensures that the carry from each bit addition is passed to the next.
- Control Signals: The Shift Control and Clock (CLK) signals manage the timing of the shifts and additions, while the Clear signal resets the flip-flop, clearing the carry when needed.

Truth Table of Full Adder

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Truth Table of D Flip Flop

Input			Output	
D	reset	clock	Q	Q'
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	0	1
1	0	1	1	0
1	1	0	0	1
1	1	1	0	1

Truth Table of 1-bit Serial Adder

Suppose Serial Input is : 01011

Initially we give Reset : Sum=0 ,Carry =0

Input	Sum	Carry
0	0	0
1	1	0
0	1	0
1	0	1
1	0	1

Boolean Equation

$S=A \oplus B \oplus Cin$

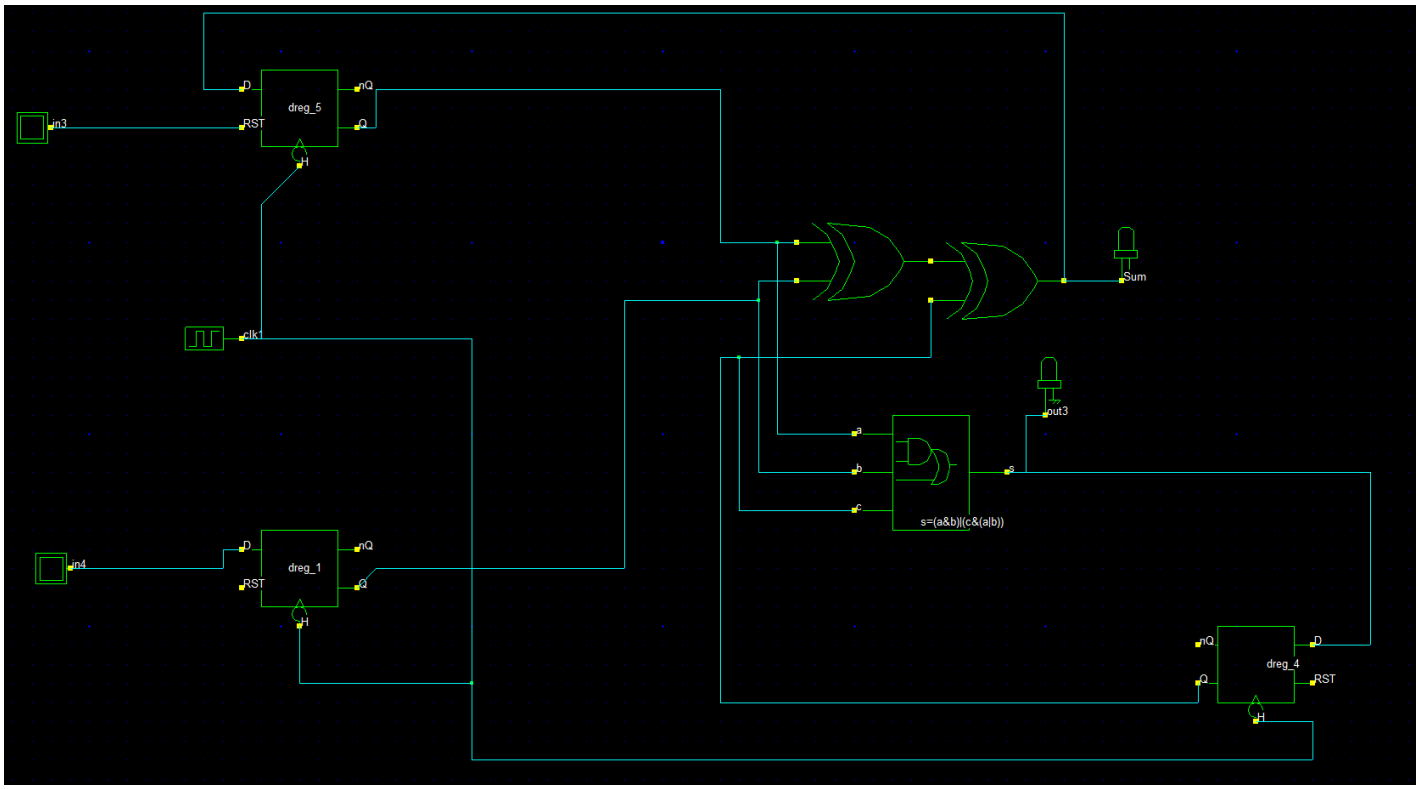
$Cout=(A \cdot B)+(B \cdot Cin)+(A \cdot Cin)$

Where A is Input Bit ,B is Previous Sum,Cin is Carry of Previous Addition

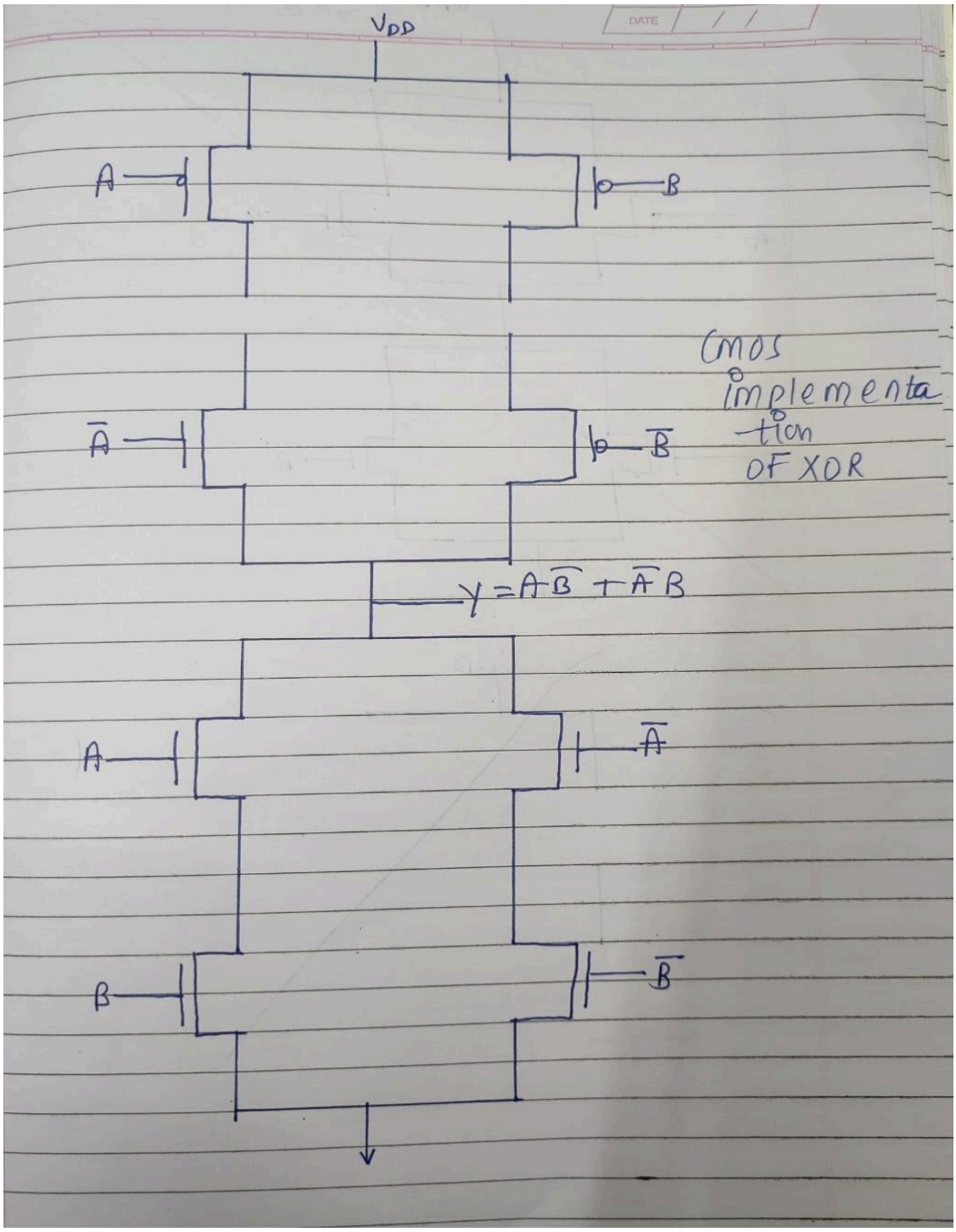
$D = Q(t+1)$

Boolean Expression of the D flip flop because the next value of Q is only dependent on the value of D, whereas there is delay of one clock pulse from input D to output

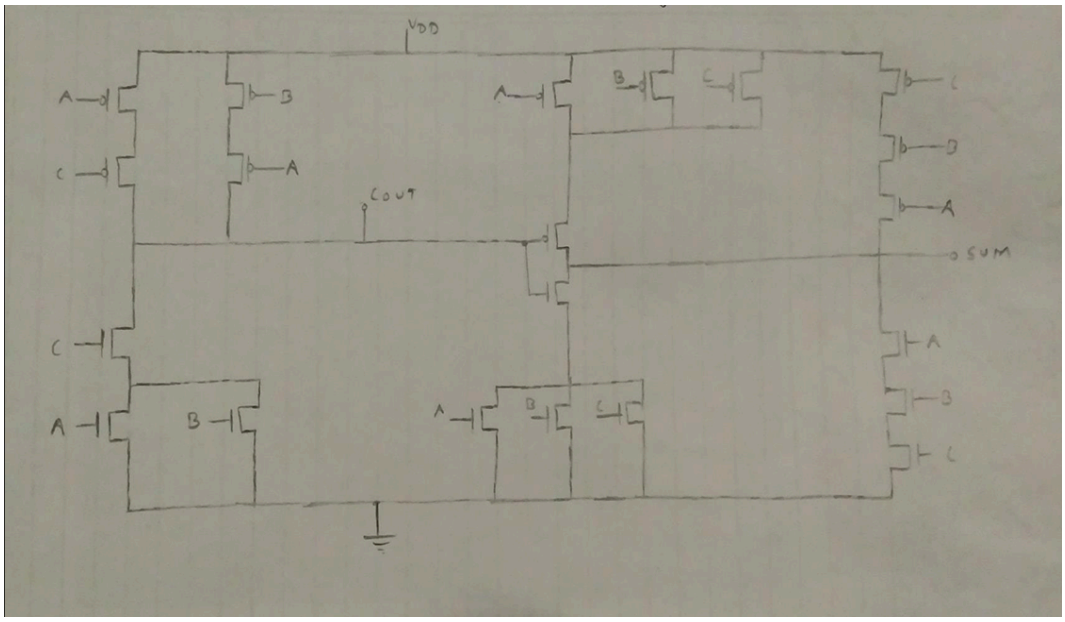
Gate Level Circuit Diagram



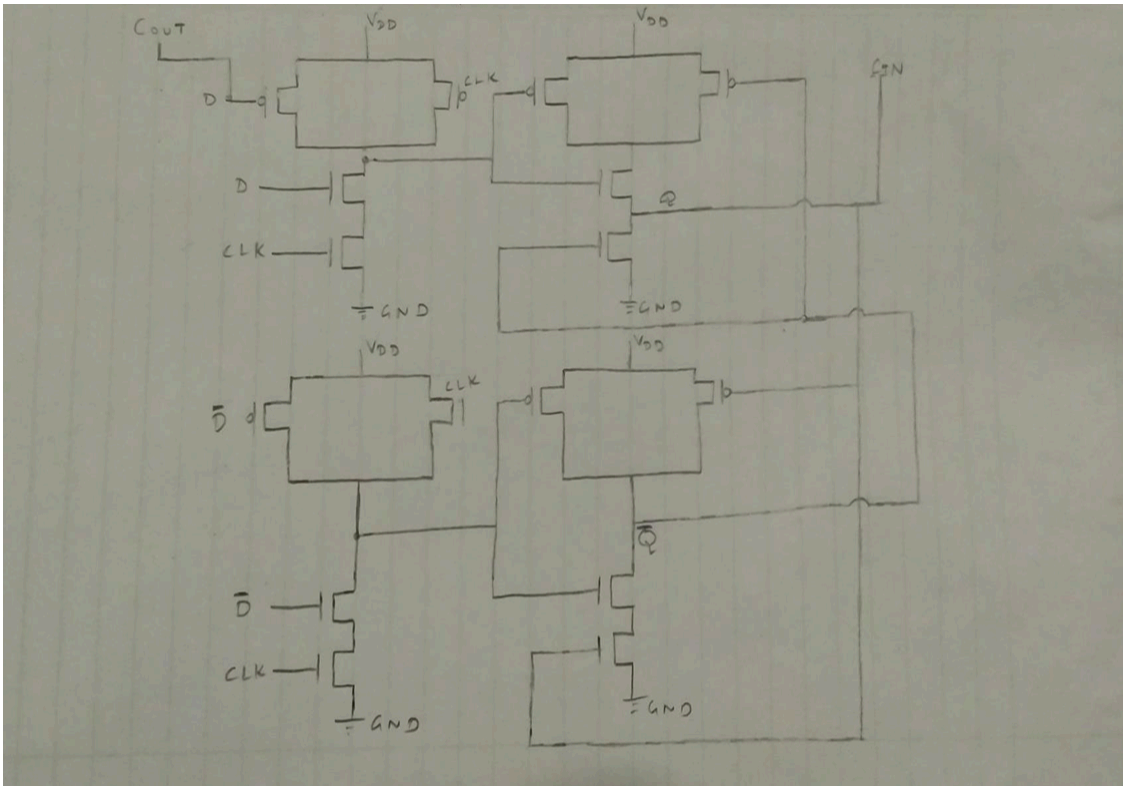
CMOS IMPLEMENTATION OF XOR GATE



CMOS Implementation of Full Adder

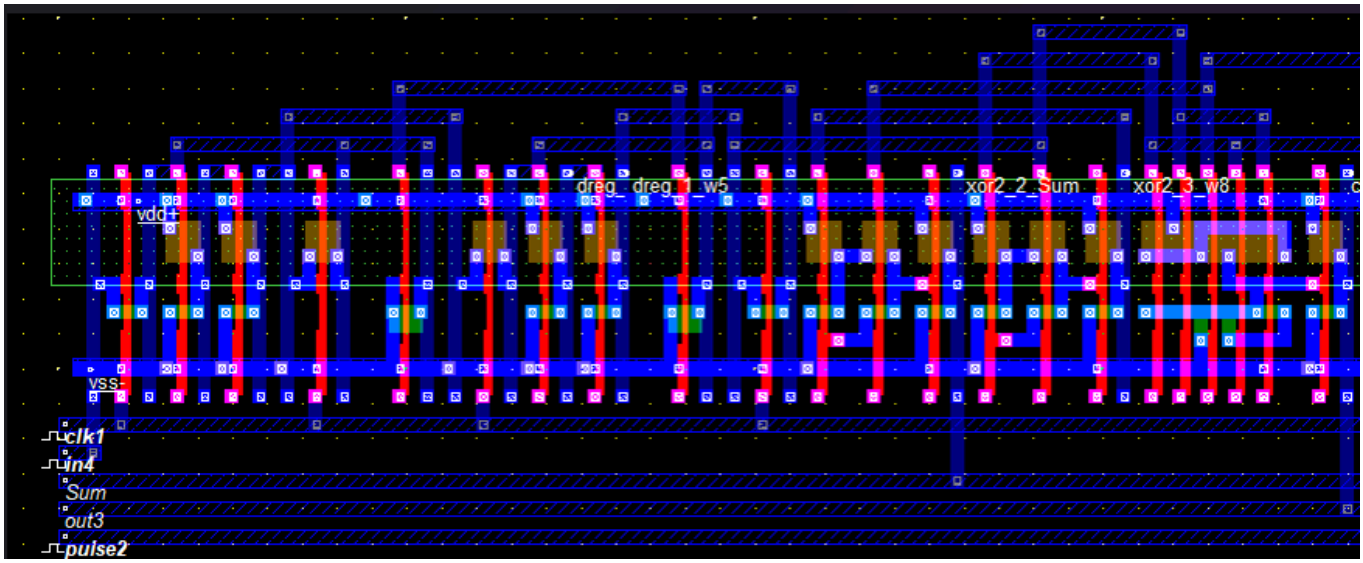


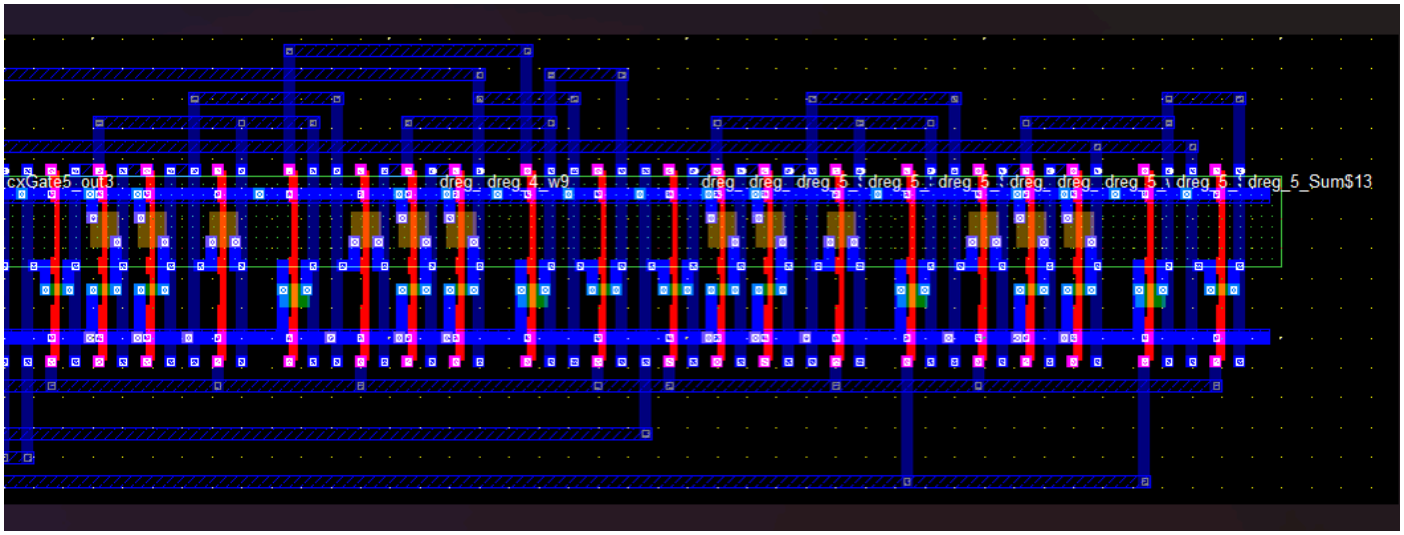
CMOS Implementation of D Flip FLop



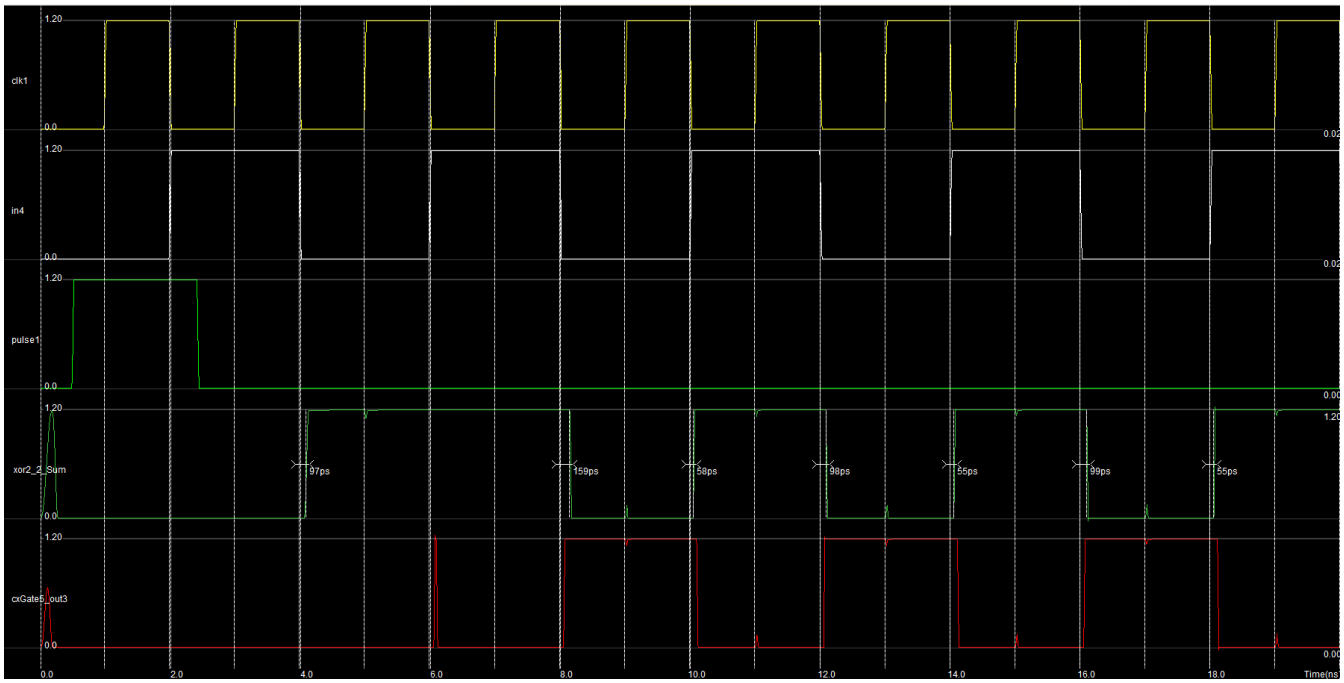
MICROWIND LAYOUT

The layout and its simulation results have been carried out: CMOS layout and its analysis have been performed for a1- bit Serial adder designed with 120 nm technology node in Microwind Design Tool





SIMULATION RESULT



- **Clock (clk1)**: The yellow waveform at the top represents the clock signal, which provides timing for the serial adder circuit. This clock signal controls when each bit is processed and ensures that the sum and carry are updated sequentially, bit by bit.
- **Reset Pulse (pulse2)**: The green waveform (labeled as "pulse2") acts as a reset signal. When this signal is high, it resets the circuit, clearing any previous carry and sum values. This is essential for initializing the adder to a known state before starting a new addition sequence.
- **Sum Output (xor2_Sum)**: The green waveform (labeled as "xor2_Sum") represents the sum output of the serial adder. This signal changes according to the bitwise addition of the input bits, based on the clock cycles. Each bit addition is performed in sync with the

clock pulses, showing that the sum is calculated one bit at a time.

- **Carry Output (xGate5_out3)**: The red waveform (labeled as "xGate5_out3") shows the carry output, which is generated by the full adder during each bit addition. The carry output is also synchronized with the clock pulses, as the carry from one bit addition is stored in the D flip-flop and used in the next cycle.

Measure the rise time, fall time, propagation delay and other parameter

Technology	120nm
VOH	1.2V
V0L	0V
Trise	97ps
T	159ps
Power	0.0252mw
Propagation Delay	128ps

Propagation delay = (τPHL + τPLH) / 2

=(97+159)/2 = 256/2=128

CONCLUSION

The 1-bit serial adder is a simple yet effective digital circuit that performs binary addition one bit at a time, using a full adder and a flip-flop for carry storage. This sequential processing approach allows the circuit to have a compact design with lower power consumption, making it suitable for applications where area and power efficiency are more important than speed.

Benefits over Parallel Adder:

1. Reduced Circuit Complexity

2. Lower Power Consumption
3. Smaller Area

Disadvantages:

1. Slower Speed: Unlike parallel adders that add all bits simultaneously, the serial adder processes bits one by one, making it slower, especially for larger binary numbers.
2. Increased Clock Cycles: Since each bit is processed in a separate clock cycle, the serial adder requires as many cycles as there are bits, which can lead to longer computation times.

Overall, the 1-bit serial adder is a good choice for low-power, space-constrained applications where high-speed performance is not critical. However, for applications requiring faster addition, a parallel adder would be more suitable despite its larger circuit size and higher power consumption.