“Combinational Circuit Simulator Development”

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Abstract

New technologies are constantly being developed that enable designers to build faster, more complex circuits.
Because analogue design typically involves numerous fundamental building block circuits, simulation is critical to fully comprehending the impact and potential of these circuits.,The code for the simulation part is slow and only simulates small circuits hence low accuracy.
We have come up with a code that simulates the large circuits in less time and with high accuracy requiring less amount of variables.
Different design concepts were compared, and one was chosen to be applied. Each module was developed independently. They were joined together to make the completed version after successful simulation and testing.

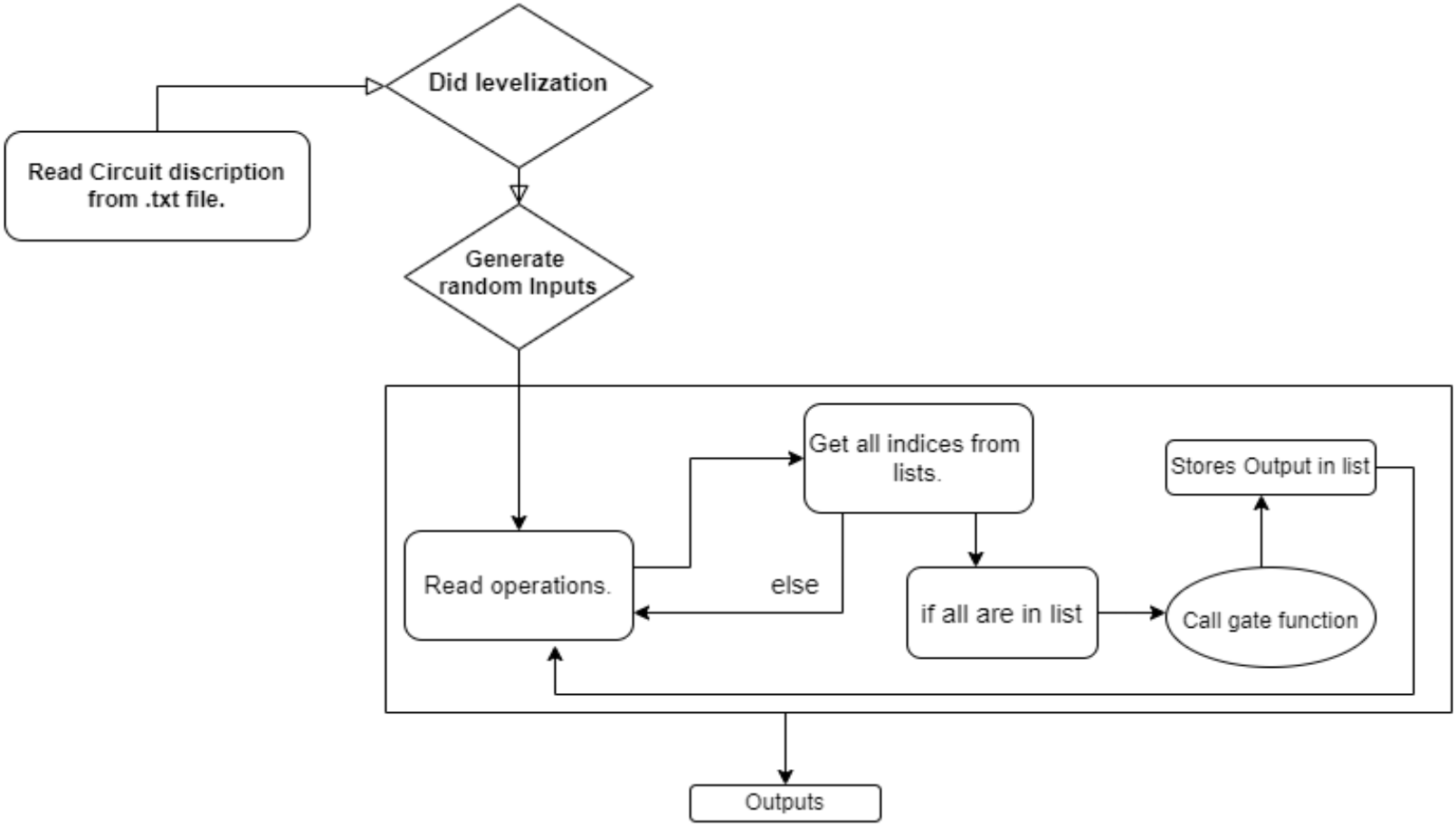
Introduction :

A Combinational Circuit is made up of logic gates whose outputs are determined only by the current combination of inputs at any one time, with no consideration for previous inputs. Combinational circuits include the adder, subtractor, converter, and encoder/decoder..
An emulator is a hardware simulator, while a software simulator is a computer programme. Simulation is used to validate logic, evaluate designs, and provide tests..

Design Problem Formulation

As technology advances, the number of gates operations in an circuit increases. Huge circuits are impractical to design manually .We get results from a faulty operation that are unsuitable for work and unanticipated..These incorrect outputs lead to incorrect evaluation and analysis. Also one cannot afford wasting so much of time and resources in finding silly faults caused by faulty computing. Thus, there is a need to develop a low cost and easy maintainable, user friendly simulator.

Methodology adopted for the project



Justification of the design choices

Simulation is used to ensure that the design and tests are correct.

It avoids building costly hardware ,huge reduction in time is required to create circuits manually(almost impractical to design).

Can assist in the debugging of a design in a variety of ways that real hardware cannot..

Better performance – mainly useful for higher frequency operation.

Fundamentally different approach - instead of manually interconnecting gates and inputs, a design code is used to specify higher level functionality and also involves less variables.

Results

S.No	Numbers of Inputs	Numbers of Outputs	Number of gates operations	Length of Input	Time of execution (s)
1	33	25	880	400	0.144796371459
2	157	65	1200	800	0.314556026458
3	1000	800	2000	1000	0.623652125346
4	1200	850	2500	800	0.815732111472
5	1500	1000	3000	1200	0.84621400399

Conclusions

The simulator was successfully designed and successfully run for circuits being placed in text files and gives results of required outputs in less execution time.

The model is simple to use and understand.. It reduces time to get outputs as we are testing it Compared to manual testing, which involves making multiple connections and applying inputsThe code can be changed. If any additional changes are required to meet the needs of the user, these can be made very easily. It saves lots of time and resources and thus is efficient for operations. It would be very valuable for for peoples involving in circuit designs.

References

We had taken circuits from
“http://www.pld.ttu.ee/~maksim/benchmarks/iscas85/bench/”.