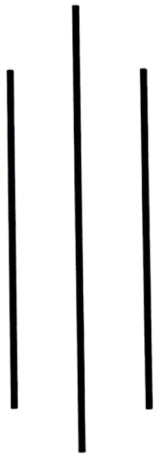
TRIBHUVAN UNIVERSITY

PATAN MULTIPLE CAMPUS

PATAN DHOKA, LALITPUR



DIGITAL LOGIC (BIT 103)

LAB ..8..

SUBMITTED BY

NAME: Suresh Dahal
CLASS: BIT-III
ROLL NO: 23
DATE: 2080/12/16

SUBMITTED TO

JYOTI PRAKASH CHAUDHARY

.....

CHECKED BY

TITLE:- REALIZE THE FLIP-FLOP CIRCUITS WITH LOGIC DIAGRAM, CHARACTERISTIC TABLE AND LOGIC FUNCTION.

i) CLOCKED SR FLIP-FLOP

a) OBJECTIVE

→ To realize SR flip-flop circuit with characteristic table, logic diagram and logic function

b) REQUIREMENT

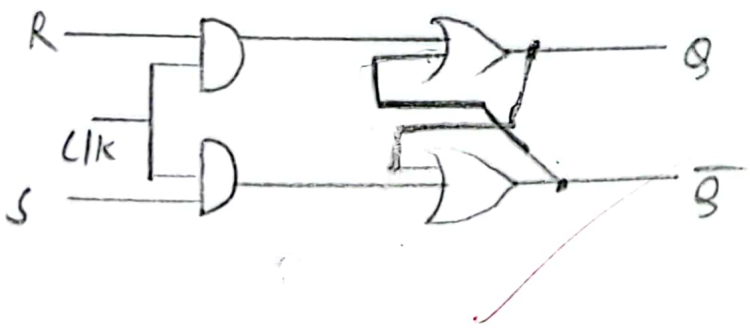
i) Digital logic kit and simulator
ii) 2 AND gates, 1 clock input, 2 NOR gates
iii) Connecting wires
iv) Interactive Isequence generator as input
v) LED as output

c) THEORY

1. INTRODUCTION

SR flip-flop has two inputs R and S and two outputs i.e. normal and complemented. It has two states set and reset. It should be given a clock pulse to change its state otherwise it doesnit change value regardless of inputs variation.

2. LOGIC DIAGRAM

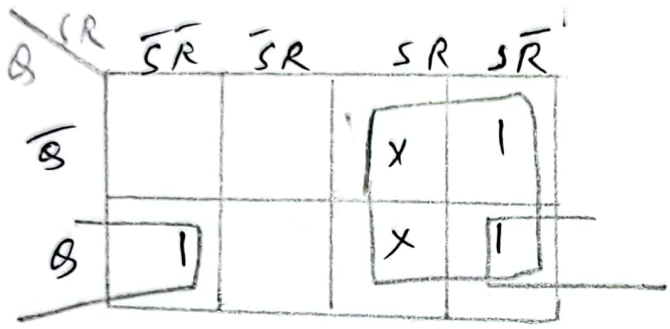


3. CHARACTERISTIC TABLE

Q	S	R	$Q(t+1)$
0	0	0	0 NC
0	0	1	0 Reset
0	1	0	1 set
0	1	1	Invalid cond"
1	0	0	1 NC
1	0	1	0 Reset
1	1	0	1 set
1	1	1	Invalid cond"

S	R	CLK	Q_{t+1}	Comments
0	0	X	Q_t	NC
0	1	↑	0	Reset
1	0	↑	1	set
1	1	↑	?	Invalid

4. CHARACTERSTIC EQUATION



$$Q(t+1) = S + R'Q$$

5) CONCLUSION

In this lab, we have realized the clocked RS flip-flop circuit with logic diagram, characteristic table and logic function.

ii) JK FLIP-FLOP

a) OBJECTIVE

→ To realize the JK flip flop with logic diagram, characteristic table and logic function

b) REQUIREMENT

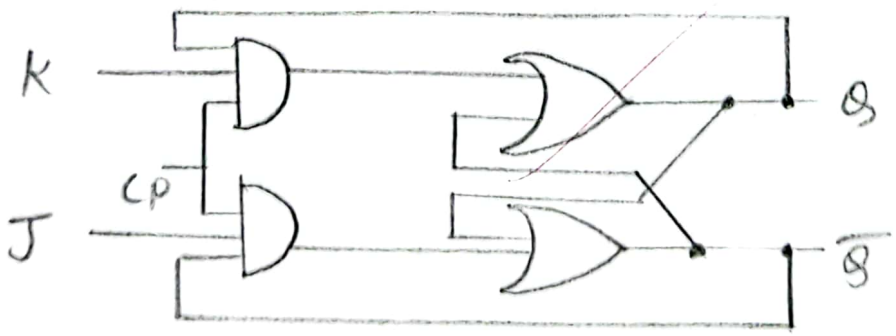
i) Digital logic kit and simulator
ii) 2 AND gates, 2 OR gates
iii) Connecting wires
iv) Interactive I/sequence generator as input
v) LED as output

c) THEORY

1. INTRODUCTION

JK is a refinement of the RS flip-flop to resolve invalid condition in RS flipflop. In JK, output Q is ANDed with K and CP inputs so that the flip-flop is cleared during a clock pulse only if Q was previously 1. Similarly Q' is ANDed with J and CP inputs.

2. LOGIC DIAGRAM

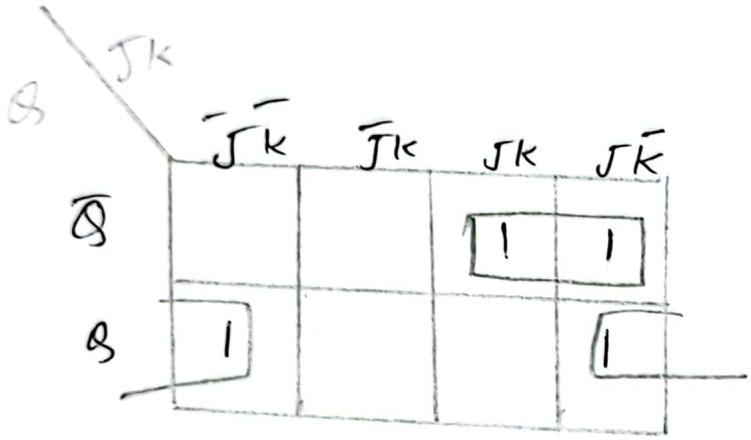


3. CHARACTERISTIC TABLE

Q	J	K	Q(t+1)	
0	0	0	0	NC
0	0	1	0	Reset
0	1	0	1	set
0	1	1	1	toggle
1	0	0	1	NC
1	0	1	0	Reset
1	1	0	1	set
1	1	1	0	toggle

J	K	Q(t+1)	
0	0	Qt	NC
0	1	0	Reset
1	0	1	set
1	1	Q't	toggle

4. CHARACTERISTIC EQUATION



$$Q(t+1) = JQ' + k'Q$$

d) CONCLUSION :-

In this Lab, we have realized Jk flipflop with logic diagram, characteristics table and equation.

iii) D-FLIP-FLOP

a) OBJECTIVE

→ To realize the D flip-flop circuit with logic circuit, characteristics table and logic expression.

b) REQUIREMENT

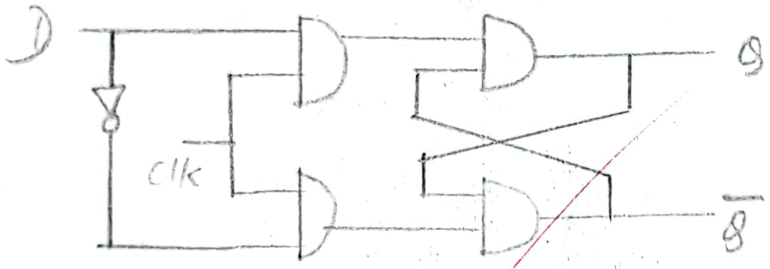
i) Digital logic kit and simulator
ii) 1 NOT gate, 4 NAND gates
iii) Connecting wires
iv) Interactive Isequence generator as input
v) LED as output

c.) THEORY

1. INTRODUCTION :-

D flip flop means delay flip flop. It delays the output and gives input as output. It has only one input D.

2. LOGIC DIAGRAM :-

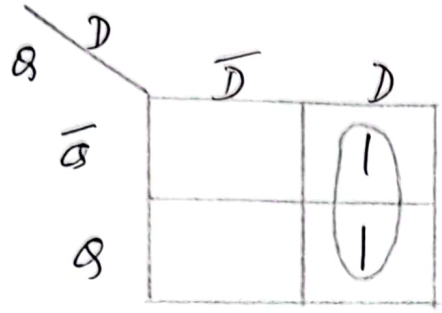


3. CHARACTERISTIC TABLE

Q	D	Q+1
0	0	0
0	1	1
1	0	0
1	1	1

inputs		outputs	
clk	D	Q	$\overline{Q}$
0	X	NC	NC
1	0	0	1
1	1	1	0

4. CHARACTERISTIC EQUATION



$Q(t+1) = D$

5) CONCLUSION:-

In this lab, we have realized the D-flip-flop circuit with logic diagram, characteristics table and characteristics equation.

iv) T-FLIP-FLOP

a) OBJECTIVE

→ To realize T flip-flop with logic diagram, characteristics table and equation

b) REQUIREMENT

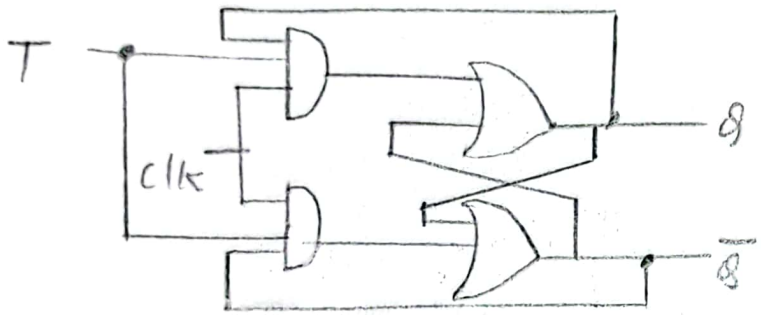
i) Digital logic kit or simulator
ii) 2 AND gates, 2 NOR gates
iii) Connecting wires
iv) Interactive / sequence generator as input
v) LED as output

c.) THEORY

1. INTRODUCTION

T means toggle flip-flop. It is a single input version of JK flip-flop. Regardless of present state, the flip-flop complements its state when clock pulse occurs while input T is 1.

2. LOGIC DIAGRAM

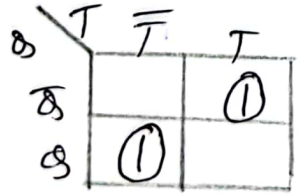


3. CHARACTERISTICS TABLE

Q	T	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

T	Q(t+1)	
0	Q_t	No change
1	$\overline{Q}_t$	complement

4. CHARACTERISTIC EQUATION



$$Q(t+1) = T.\overline{Q} + \overline{T}.Q$$

d.) CONCLUSION:

In this Lab, we have realized T-flip-flop with logic diagram, characteristic table and ~~Lag~~ characteristics equation.