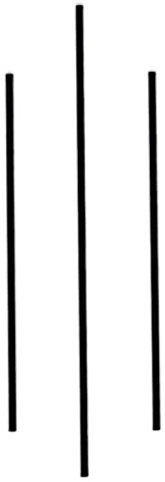
TRIBHUVAN UNIVERSITY

PATAN MULTIPLE CAMPUS

PATAN DHOKA, LALITPUR



DIGITAL LOGIC (BIT 103)

LAB .9...

SUBMITTED BY

NAME: Suresh Dahal

CLASS: BIT - II I

ROLL NO: 23

DATE: 20/01/2026

SUBMITTED TO

JYOTI PRAKASH CHAUDHARY

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CHECKED BY

TITLE:- REALIZE MASTER SLAVE FLIP-FLOP CIRCUIT WITH LOGIC DIAGRAM, TRUTH TABLE AND TIMING DIAGRAM

a) OBJECTIVE

→ To realize master-slave flip-flop circuit with logic diagram, truth table and timing diagram

b) REQUIREMENTS

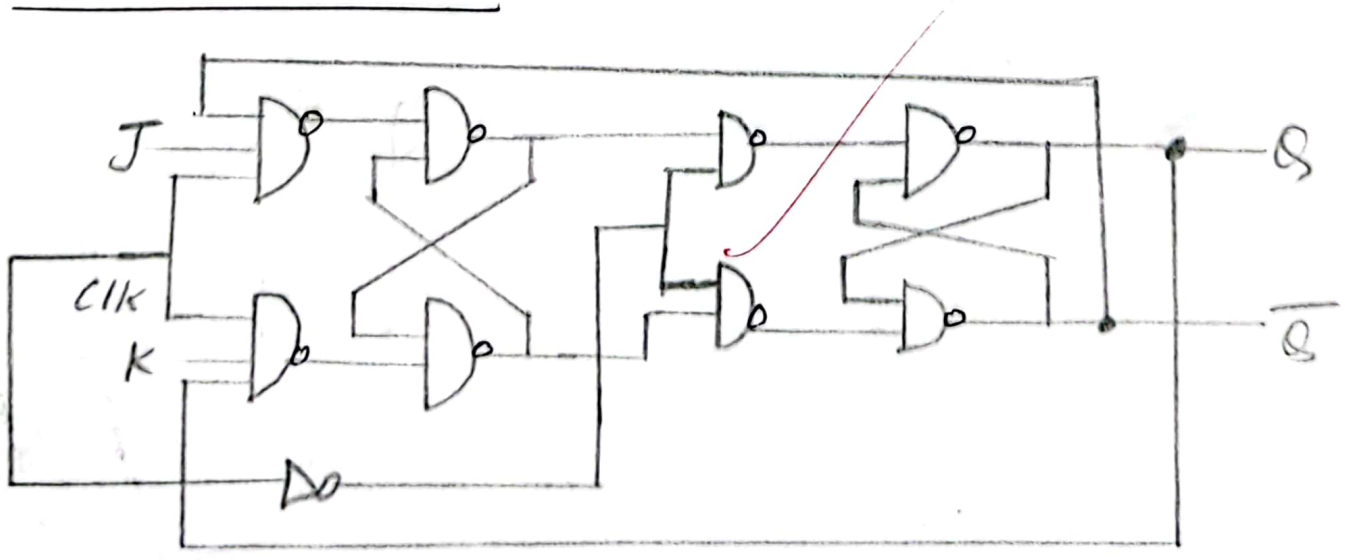
i) Digital logic kit and simulator
ii) 8 NAND gates, 1 NOT gate
iii) Connecting wires
iv) Interactive / sequence generator as input
v) LED as output

c) THEORY

1.) INTRODUCTION

It consists of two flip-flops. one is called master and another is called slave. Output from master is given input for slave and clock pulse provided to each flip-flop is complement of each other.

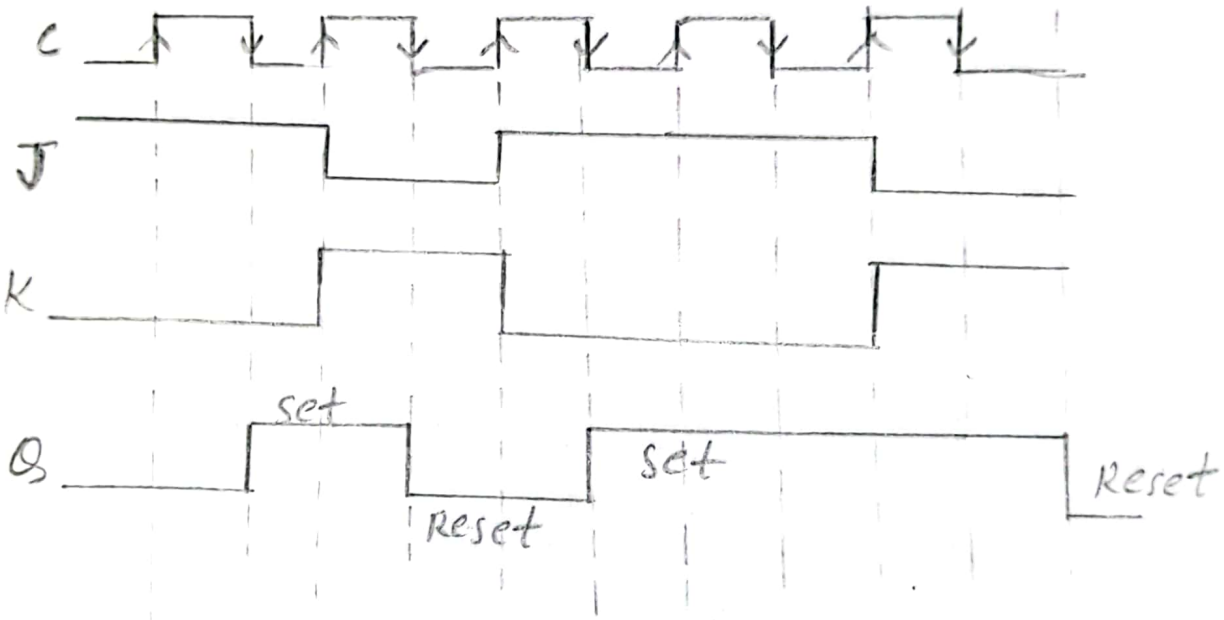
2.) LOGIC DIAGRAM



3. CHARACTERISTIC TABLE

inputs			outputs		Remark
Clk	J	K	Q_{n+1}	$\overline{Q_{n+1}}$	
X	0	0	Q_n	$\overline{Q_n}$	NO change
↑	0	0	Q_n	$\overline{Q_n}$	NO change
↑	0	1	0	1	Reset
↑	1	0	1	0	set
↑	1	1	$\overline{Q_n}$	Q_n	Toggle

4. TIMING DIAGRAM:-



5) CONCLUSION:-

In this lab, we have realized master slave flip flop with logic diagram, truth table and timing diagram.