

TRIBHUVAN UNIVERSITY

# PATAN MULTIPLE CAMPUS

PATAN DHOKA, LALITPUR



DIGITAL LOGIC (BIT 103)

LAB ...!

SUBMITTED BY

NAME: Suresh Dahal  
CLASS: BIT-I/I-A  
ROLL NO: 23  
DATE: 2080/12/22

SUBMITTED TO

JYOTI PRAKASH CHAUDHARY

.....  
CHECKED BY

TITLE:- DESIGN mod-11 SYNCHRONOUS UP COUNTER WITH STATE DIAGRAM, TRANSITION TABLE AND TIMING DIAGRAM.

a) OBJECTIVE

→ To design mod-11 synchronous up counter with state diagram, transition table and timing diagram

b) REQUIREMENTS

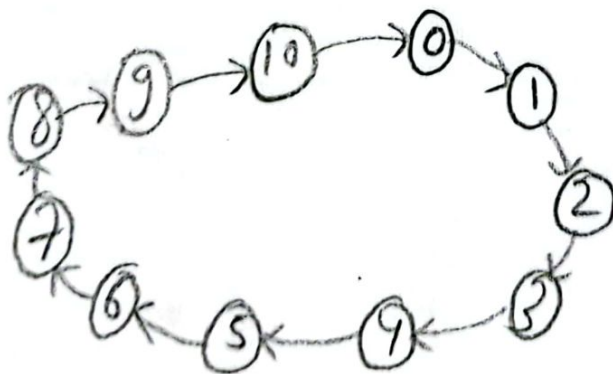
- i) Digital logic kit and simulator
- ii) 4 JK flip-flop
- iii) clock, interactive input
- iv) connecting wires
- v) LED as output

c) THEORY

1.) INTRODUCTION:-

mod (modules) - 11 synchronous up counter is a sequential logic circuit which contains 4 flip-flops as we need 4-bit to represent 10 in binary i.e. 1010. It counts from 0-10 and then cycles back to 0.

2.) STATE DIAGRAM



### 3. TRANSITION TABLE

prev. state				next state				Excitation			
$Q_4$	$Q_3$	$Q_2$	$Q_1$	$Q_4$	$Q_3$	$Q_2$	$Q_1$	$J_4 K_4$	$J_3 K_3$	$J_2 K_2$	$J_1 K_1$
0	0	0	0	0	0	0	1	0 X	0 X	0 X	1 X
0	0	0	1	0	0	1	0	0 X	0 X	1 X	X 1
0	0	1	0	0	0	1	1	0 X	0 X	X 0	1 X
0	0	1	1	0	1	0	0	0 X	1 X	X 1	X 1
0	1	0	0	0	1	0	1	0 X	X 0	0 X	1 X
0	1	0	1	0	1	1	0	0 X	X 0	X 1 X	X 1
0	1	1	0	0	1	1	1	0 X	X 0	X 0	1 X
0	1	1	1	0	0	0	0	1 X	X 1	X 1	X 1
1	0	0	0	1	0	0	1	X 0	0 X	0 X	1 X
1	0	0	1	1	0	1	0	X 0	0 X	1 X	X 1
1	0	1	0	0	0	0	0	X 1	0 X	X 1	0 X

### 4. EQUATIONS:- For $J_4$

$Q_4 Q_3$	$Q_2 Q_1$	$\overline{Q_2} \overline{Q_1}$	$\overline{Q_2} Q_1$	$Q_2 \overline{Q_1}$	$Q_2 Q_1$
$\overline{Q_4} \overline{Q_3}$	0	0	0	0	
$\overline{Q_4} Q_3$	0	0	1	0	
$Q_4 \overline{Q_3}$	X	X	X	X	
$Q_4 Q_3$	X	X	X	X	

$$J_4 = Q_3 Q_2 \overline{Q_1}$$

### For $K_4$

$Q_4 Q_3$	$Q_2 Q_1$	$\overline{Q_2} \overline{Q_1}$	$\overline{Q_2} Q_1$	$Q_2 \overline{Q_1}$	$Q_2 Q_1$
$\overline{Q_4} \overline{Q_3}$	X	X	X	X	
$\overline{Q_4} Q_3$	X	X	X	X	
$Q_4 \overline{Q_3}$	X	X	X	X	
$Q_4 Q_3$	0	0	X	1	

$$K_4 = Q_2$$

For  $J_3$

$\overline{Q_4}Q_3$ \ $Q_2Q_1$	$\overline{Q_2}\overline{Q_1}$	$\overline{Q_2}Q_1$	$Q_2\overline{Q_1}$	$Q_2Q_1$
$\overline{Q_4}\overline{Q_3}$	0	0	1	0
$\overline{Q_4}Q_3$	x	x	x	x
$Q_4\overline{Q_3}$	x	x	x	x
$Q_4Q_3$	0	0	x	0

$$J_3 = Q_2Q_1$$

For  $K_3$

$\overline{Q_4}Q_3$ \ $Q_2Q_1$	$\overline{Q_2}\overline{Q_1}$	$\overline{Q_2}Q_1$	$Q_2\overline{Q_1}$	$Q_2Q_1$
$\overline{Q_4}\overline{Q_3}$	x	x	x	x
$\overline{Q_4}Q_3$	0	0	1	0
$Q_4\overline{Q_3}$	x	x	x	x
$Q_4Q_3$	x	x	x	x

$$K_3 = Q_2Q_1$$

For  $J_2$

$\overline{Q_4}Q_3$ \ $Q_2Q_1$	$\overline{Q_2}\overline{Q_1}$	$\overline{Q_2}Q_1$	$Q_2\overline{Q_1}$	$Q_2Q_1$
$\overline{Q_4}\overline{Q_3}$	0	1	x	x
$\overline{Q_4}Q_3$	0	1	x	x
$Q_4\overline{Q_3}$	x	x	x	x
$Q_4Q_3$	0	1	x	x

$$J_2 = Q_1$$



For  $K_2$

$\overline{Q_4}Q_3$ \ $Q_2Q_1$	$\overline{Q_2}\overline{Q_1}$	$\overline{Q_2}Q_1$	$Q_2\overline{Q_1}$	$Q_2Q_1$
$\overline{Q_4}\overline{Q_3}$	X	X	1	0
$\overline{Q_4}Q_3$	X	X	1	0
$Q_4\overline{Q_3}$	X	X	X	X
$Q_4Q_3$	X	X	X	1

$$K_2 = Q_1 + Q_4$$

For  $J_1$

$\overline{Q_4}Q_3$ \ $Q_2Q_1$	$\overline{Q_2}\overline{Q_1}$	$\overline{Q_2}Q_1$	$Q_2\overline{Q_1}$	$Q_2Q_1$
$\overline{Q_4}\overline{Q_3}$	1	X	X	1
$\overline{Q_4}Q_3$	1	X	X	1
$Q_4\overline{Q_3}$	X	X	X	X
$Q_4Q_3$	1	X	X	0

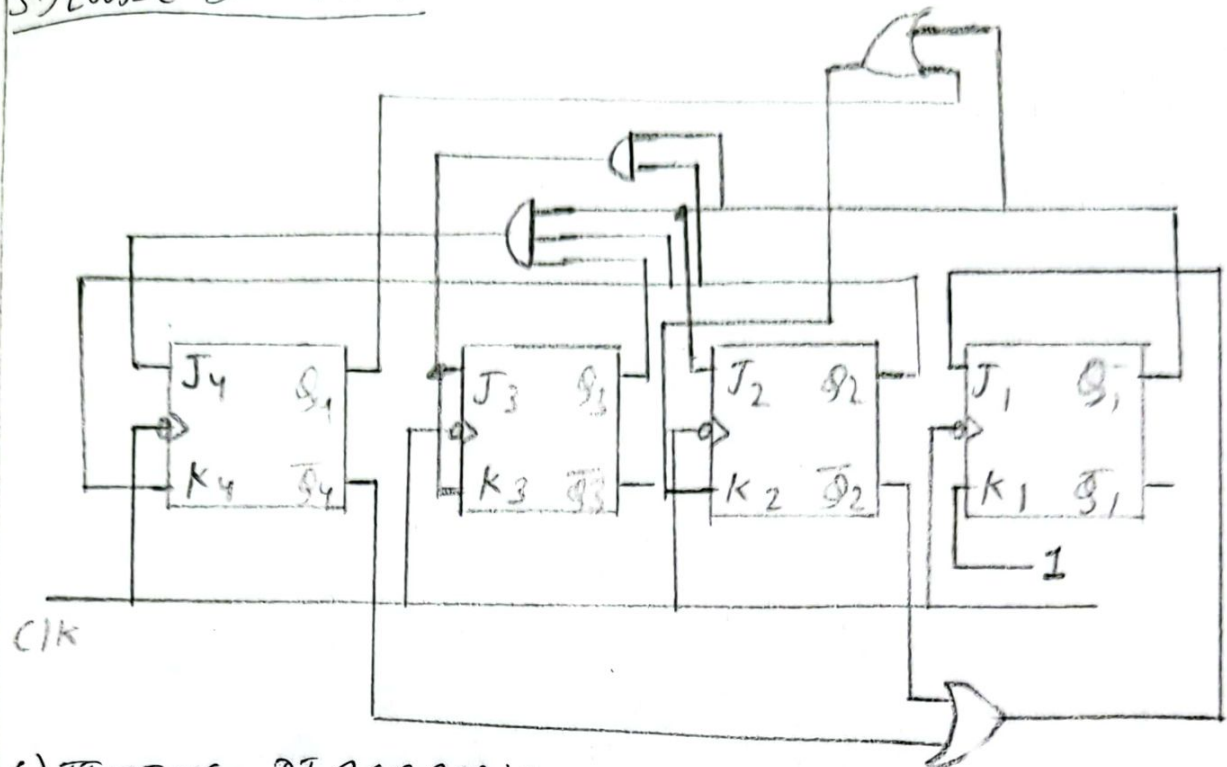
$$J_1 = \overline{Q_4} + \overline{Q_2}$$

For  $K_1$

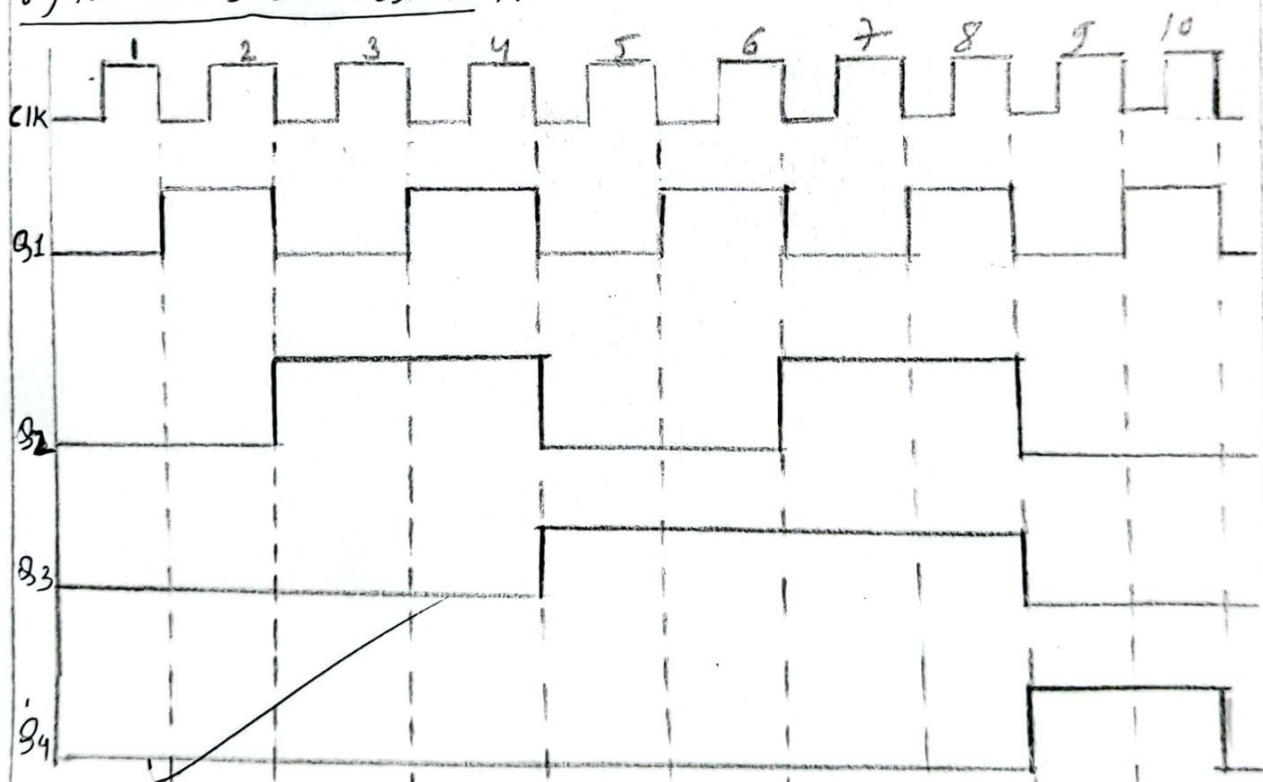
$\overline{Q_4}Q_3$ \ $Q_2Q_1$	$\overline{Q_2}\overline{Q_1}$	$\overline{Q_2}Q_1$	$Q_2\overline{Q_1}$	$Q_2Q_1$
$\overline{Q_4}\overline{Q_3}$	X	1	1	X
$\overline{Q_4}Q_3$	X	1	1	X
$Q_4\overline{Q_3}$	X	X	X	X
$Q_4Q_3$	X	1	X	X

$$K_1 = 1$$

### 5.) LOGIC DIAGRAM



### 6.) TIMING DIAGRAM:-



### 7.) CONCLUSION:-

In this lab, we have designed a mod-11 synchronous up counter with transition table, logic diagram and timing diagram and state diagram.

*[Signature]*  
02/01/22