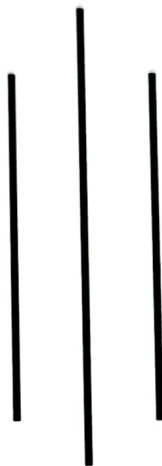TRIBHUVAN UNIVERSITY

PATAN MULTIPLE CAMPUS

PATAN DHOKA, LALITPUR

DIGITAL LOGIC (BIT 103)
LAB ..6..

SUBMITTED BY

NAME: Suresh Dahal
CLASS: BIT - I II
ROLL NO: 23
DATE: 2080 / 12 / 16

SUBMITTED TO

JYOTI PRAKASH CHAUDHARY

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CHECKED BY

TITLE:- IMPLEMENT THE FULL ADDER LOGIC CIRCUIT IN BOTH SOP AND POS WITH LOGIC DIAGRAM AND TRUTH TABLE.

a) OBJECTIVE

⇒ To implement the full adder Logic circuit in both SOP and POS

b) REQUIREMENTS

i) Digital logic kit and simulator
ii) 6 OR gate, 3 NOT gates, 8 AND gates
iii) Connecting wires
iv) Interactive /sequence generator as input
v) LED as output

C) THEORY

1. INTRODUCTION :-

Full adder is a combinational logic circuit that forms the arithmatic sum of three inputs. It has three inputs and 2 outputs i.e. Sum and carry.

2. FOR SOP

2.1. TRUTH TABLE :-

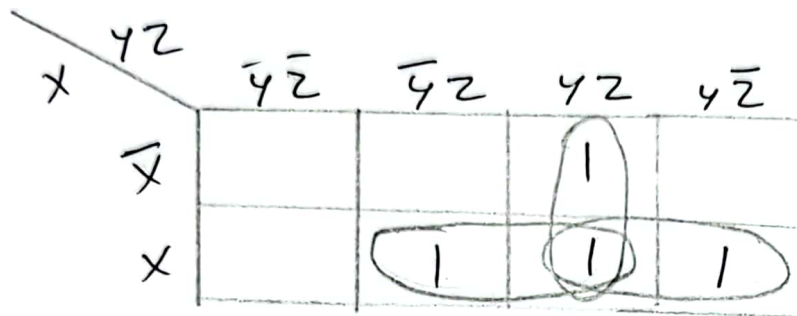| X	Y	Z	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$Sum = X'y'z + X'yz' + Xy'z' + Xyz$

$Carry = X'yz + Xy'z + Xyz$

2.2 K-MAP :-

Since sum can't be further simplified even after using k-map as there exists no loop between two or more adjacent elements, we use k-map to simplify equation of carry.
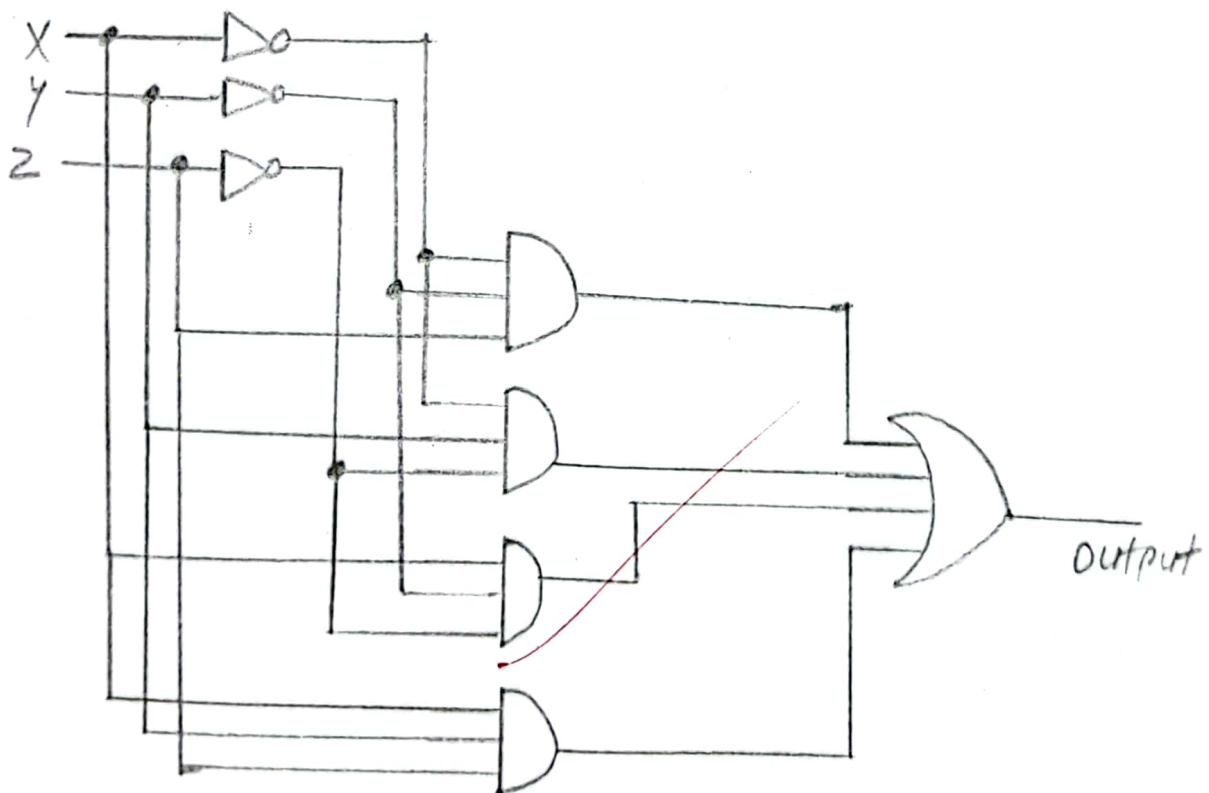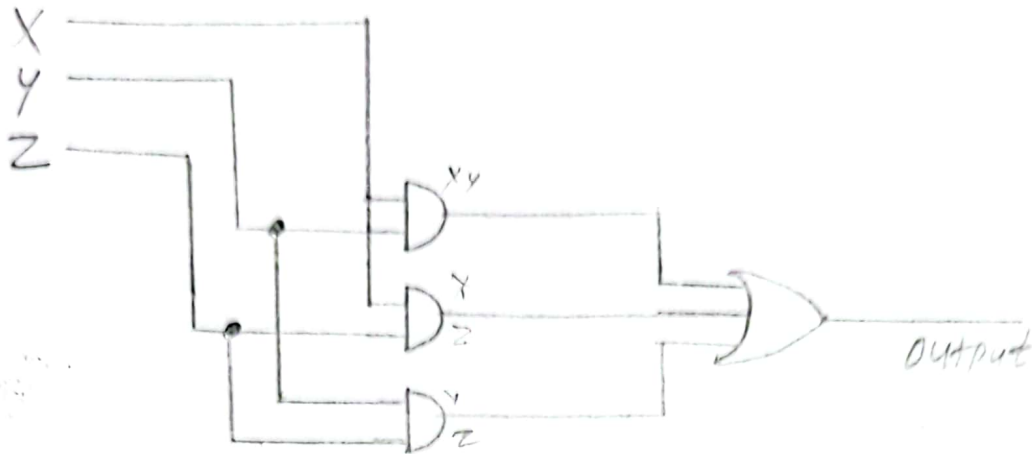
⇒ FOR CARRY :-

Now, carry $= xz + yz + xy$

2.3. CIRCUIT DIAGRAM

FOR SUM

output

FOR CARRY

3. FOR POS

$$S = (x+y+z)(x'+y'+z')(x'+y+z')(x'+y'+z)$$
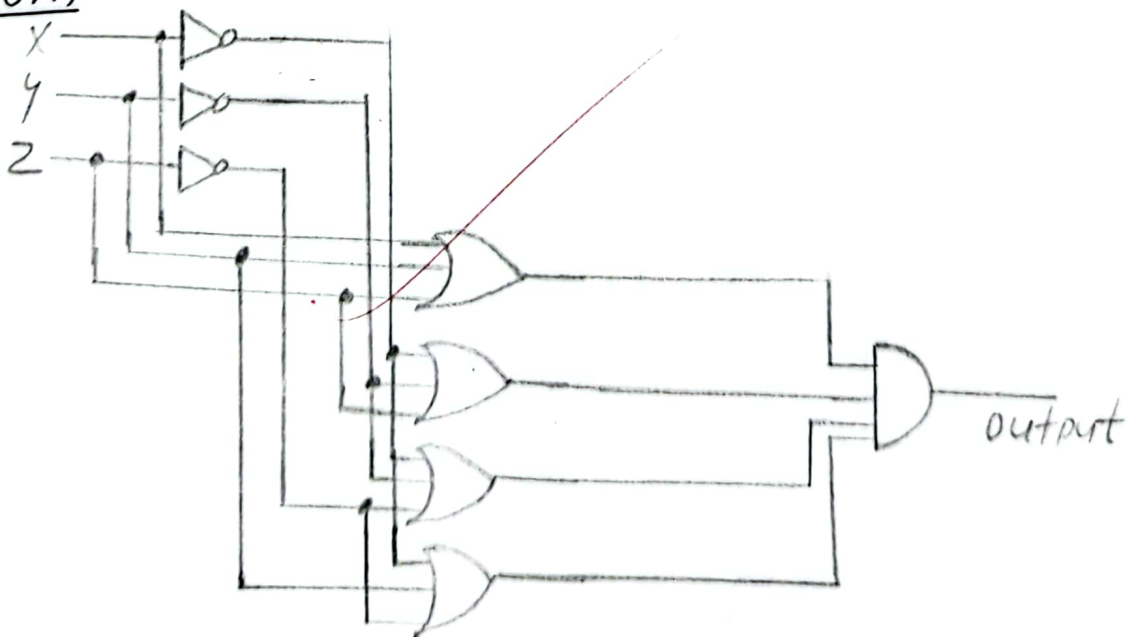$$C = (x+y+z)(x+y+z')(x+y'+z)(x'+y+z)$$
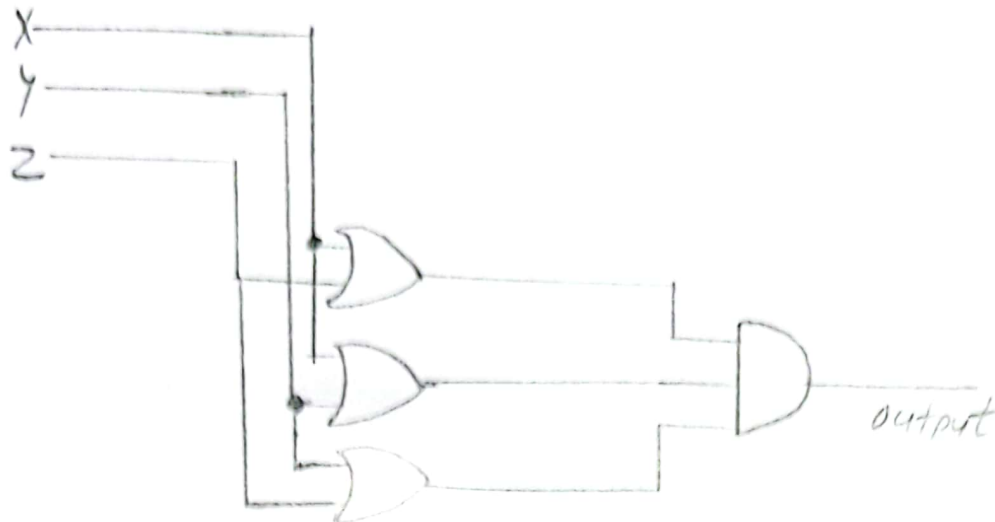
3.1 K-MAP FOR CARRY

NOW,
$$C = (x+z)(x+y)(y+z)$$

3.2 CIRCUIT DIAGRAM :-

For Sum

FOR CARRY:-

output

d.) CONCLUSION:-

In this lab, we have learned to implement full adder logic circuit in both sop and pos with the help of digital logic simulator software and verified the output with the truth table.