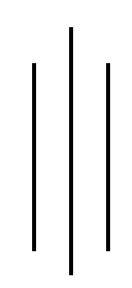
#### TRIBHUVAN UNIVERSITY

# PATAN MULTIPLE CAMPUS

PATAN DHOKA, LALITPUR



# DIGITAL LOGIC (BIT 103) LAB 6

SUBMITTED BY	SUBMITTED TO
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DATE: 2080/12/13

# TITLE: IMPLEMENT THE FULL ADDER LOGIC CIRCUIT IN BOTH SOP AND POS WITH LOGIC DIAGRAM AND TRUTH TABLE.

#### a) OBJECTIVE

• To implement full adder logic circuit in both SOP and POS with truth table and logic diagram.

#### b) REQUIREMENTS

- i. Digital Learning Kit and Simulator
- ii. 6 OR gate, 3 NOT gates, 8 AND gates
- iii. Connecting wires
- iv. Interactive / Sequence generator as input
- v. LED as output

#### c) THEORY

#### 1. INTRODUCTION

Full adder is a combinational logic circuit that forms the arithmetic sum of three input bits. It consists of three inputs and two outputs i.e. sum and carry. In this lab we are going to implement the full adder circuit in both SOP and POS to see working of full adder circuit with the help of a digital logic simulator.

#### 2. FOR SOP

#### 2.1. TRUTH TABLE

X	Y	Z	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$S = X'Y'Z + X'YZ' + XY'Z' + XYZ$$

$$C = X'YZ + XY'Z + XYZ$$

#### 2.2. K-MAP

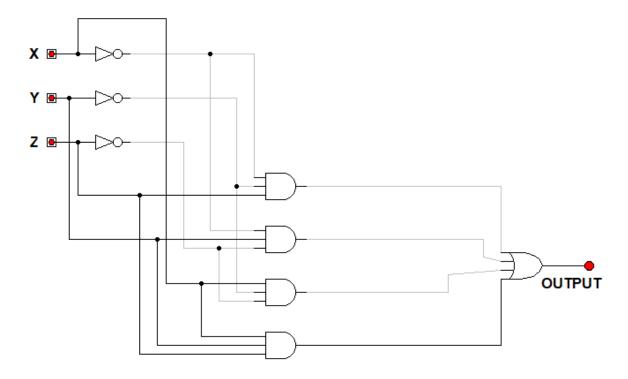
## **2.2.1 FOR SUM**

	Y'Z'	Y'Z	YZ	YZ'
X'		1		1
X	1		1	

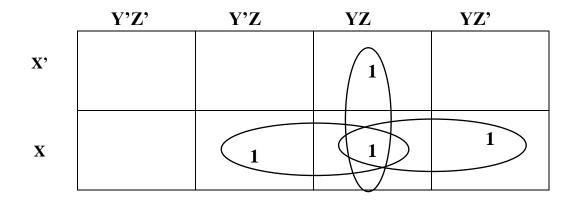
# SIMPLIFIED LOGIC EXPRESSION

S = X'Y'Z + X'YZ' + XY'Z' + XYZ

#### **CIRCUIT DIAGRAM**



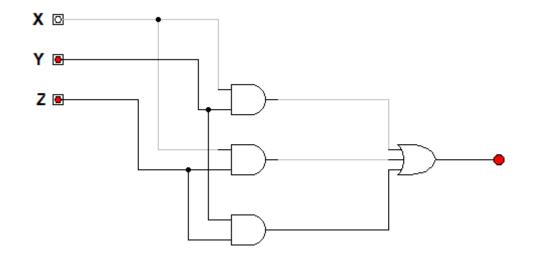
## **2.2.2 FOR CARRY**



## SIMPLIFIED LOGIC EXPRESSION

$$C = XZ + YZ + XY$$

# **CIRCUIT DIAGRAM**



#### 3. FOR POS

$$S = (X+Y+Z)(X'+Y'+Z')(X'+Y+Z')(X'+Y'+Z)$$

$$C = (X+Y+Z)(X+Y+Z')(X+Y'+Z)(X'+Y+Z)$$

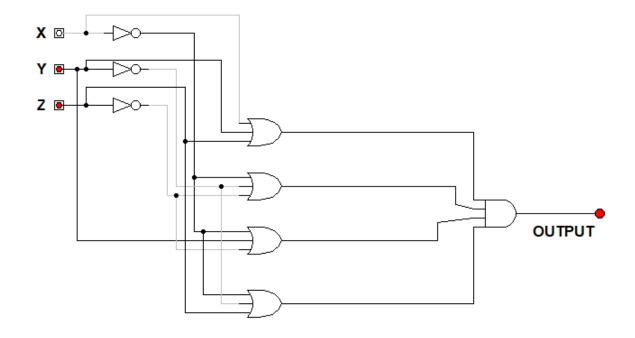
#### 3.1. K-MAP FOR SUM

	Y'Z'	Y'Z	YZ	YZ'
х'	0		0	
X		0		0

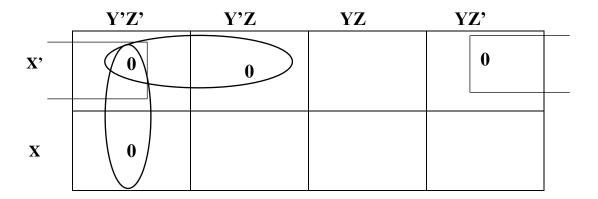
#### **SIMPLIFIED EXPRESSION**

$$S = (X+Y+Z)(X'+Y'+Z')(X'+Y+Z')(X'+Y'+Z)$$

#### **CIRCUIT DIAGRAM**



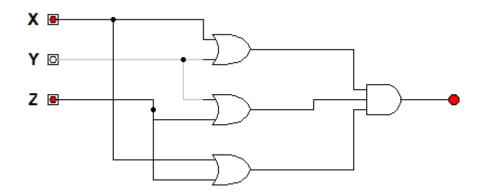
#### 3.2. K-MAP FOR CARRY



#### SIMPLIFIED EXPRESSION

$$C = (X+Z) (Y+Z) (X+Y)$$

#### **CIRCUIT DIAGRAM**



#### d. CONCLUSION

In this lab, we learned to implement full adder logic circuit in both SOP and POS with the help of the digital logic simulator software and verified its output with the truth table.