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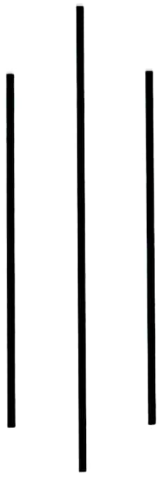

DIGITAL LOGIC (BIT 103)

LAB ...

SUBMITTED BY

NAME: Suresh Dahal
CLASS: BIT - I/I
ROLL NO: 23
DATE: 2080/12/18

SUBMITTED TO

JYOTI PRAKASH CHAUDHARY

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CHECKED BY

TITLE:- REALIZE THE GIVEN BOOLEAN FUNCTION $F = W'X'YZ + W'XY'Z + WXZ + WX'YZ$ WITH LOGIC DIAGRAM. SIMPLIFY USING K-MAP AND IMPLEMENT SIMPLIFIED FUNCTION WITH BASIC LOGIC GATES.

a) OBJECTIVE

→ To use k-map to simplify the given Boolean expression.

b) REQUIREMENTS

i) Digital logic kit and simulator
ii) 1 OR gate, 3 NOT gates, 4 NAND gates
iii) Connecting wires
iv) Interactive / sequence generator as input
v) LED as output

c.) THEORY

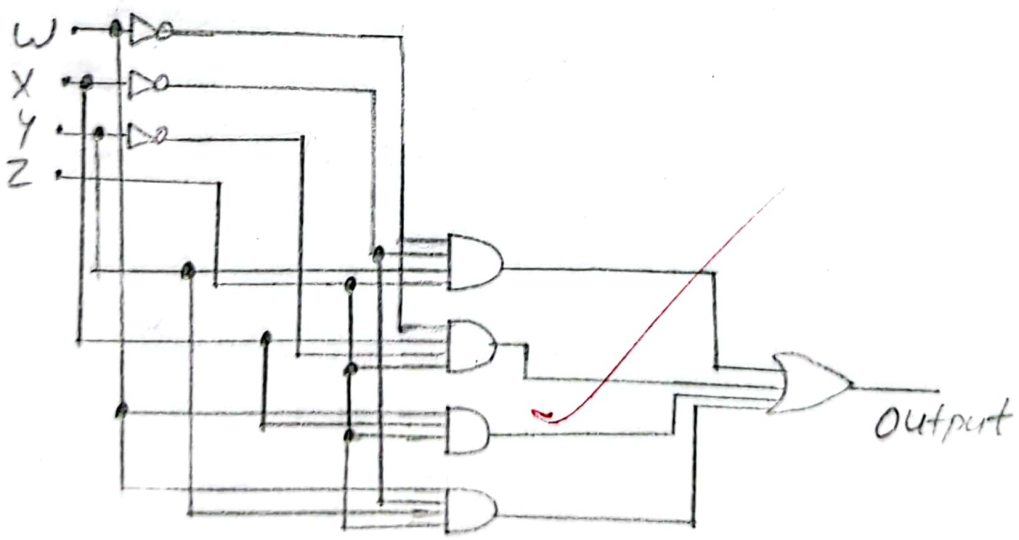
1. INTRODUCTION :-

k-map is a graphical method used to simplify boolean algebra expression by grouping adjacent cells representing similar input combinations. It offers a visual representation of truth tables, aiding in the minimization of logic functions and optimizations of digital circuits.

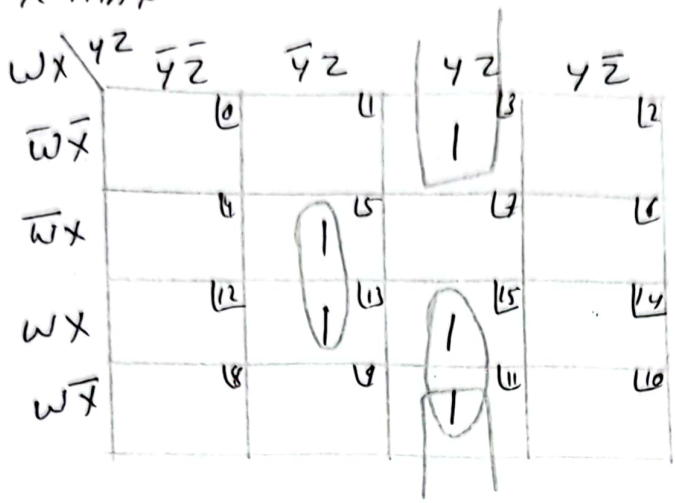
2. LOGIC EXPRESSION :-

$$F = W'X'YZ + W'XY'Z + WXZ + WX'YZ$$

3. CIRCUIT DIAGRAM :-



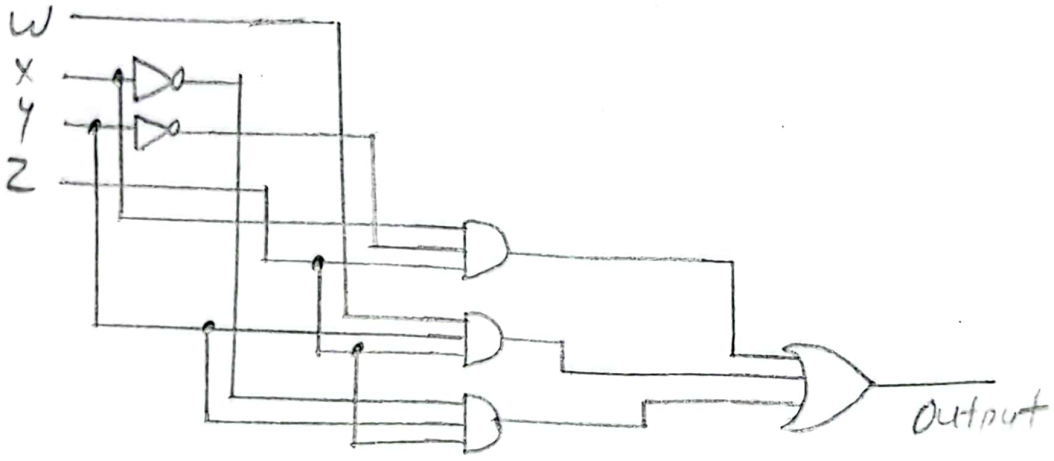
4. K-MAP



SIMPLIFIED EXPRESSION

$$F = xy'z + wyz + x'yz$$

CIRCUIT DIAGRAM FOR SIMPLIFIED EXPRESSION



d) CONCLUSION:-

Hence, by doing this practical experiment, we have seen a real world benefit of using k-map to optimize a boolean expression. It helped us get same result with simpler circuit and less electronic components.