TRIBHUVAN UNIVERSITY

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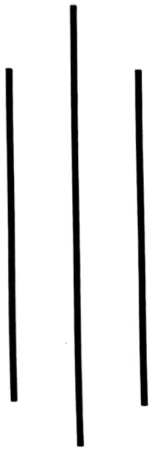
PATAN DHOKA, LALITPUR



DIGITAL LOGIC (BIT 103)

LAB .10.

SUBMITTED BY

NAME: Suresh Dahal
CLASS: BIT - II/I - A
ROLL NO: 23
DATE: 2080/12/22

SUBMITTED TO

JYOTI PRAKASH CHAUDHARY

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CHECKED BY

TITLE:-DESIGN 4-BIT BINARY RIPPLE COUNTER WITH STATE DIAGRAM ,TRUTH TABLE AND TIMING DIAGRAM

a.) OBJECTIVE

→ To design 4-bit binary ripple up counter with state diagram, truth table and timing diagram

b.) REQUIREMENTS

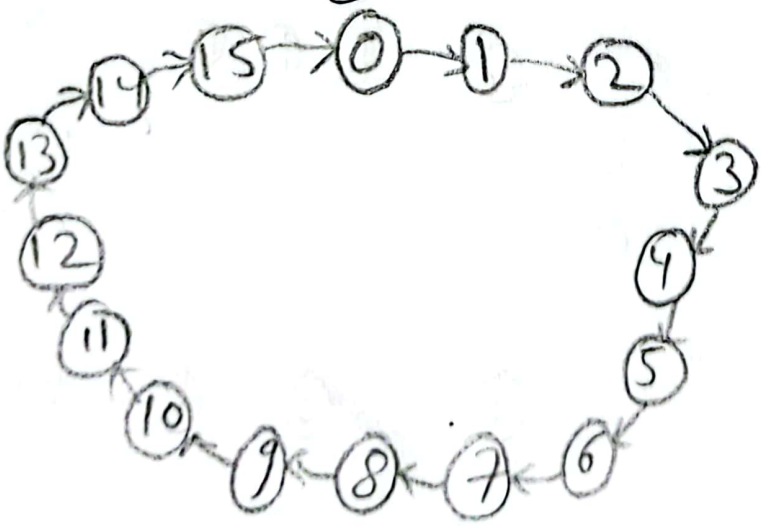
i) Digital logic kit and simulator
ii) 4 JK flip-flop, 1 NOT gate
iii) Vcc and clock input
iv) Connecting wires
v) LED as output

c.) THEORY

1. INTRODUCTION :-

Ripple Counter is a sequential logic circuit. It cycles through a specified number of state, in this case of 4-bit ripple counter, it counts from 0-15 and then recycles to 0 because it is 4-bit up counter. Ripple counter is asynchronous in nature in which first flip flop is given a negative clock pulse whose output becomes input of second flip-flop and so on.

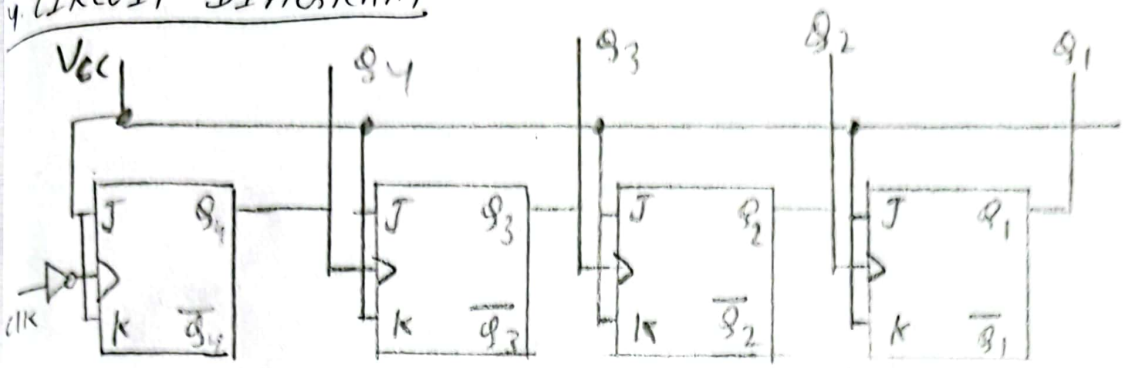
2. State Diagram :-



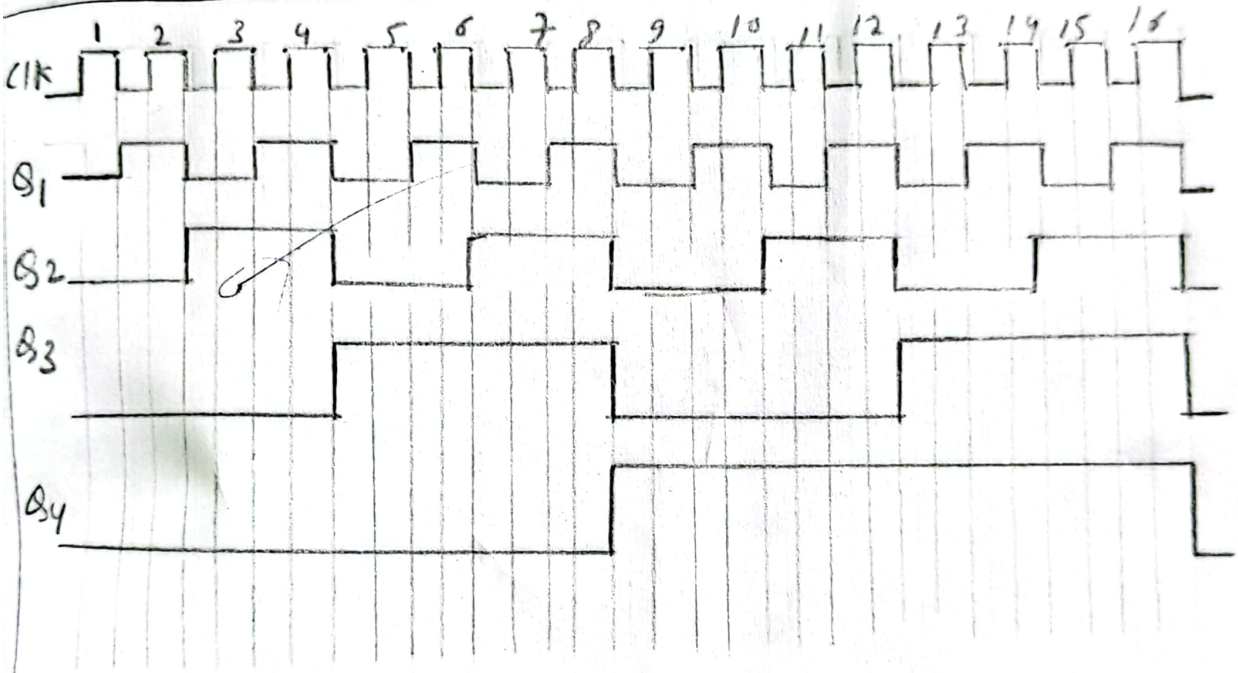
3. TRUTH TABLE

CLK	Q_4	Q_3	Q_2	Q_1
↓	0	0	0	0
↓	0	0	0	1
↓	0	0	1	0
↓	0	0	1	1
↓	0	1	0	0
↓	0	1	0	1
↓	0	1	1	0
↓	0	1	1	1
↓	1	0	0	0
↓	1	0	0	1
↓	1	0	1	0
↓	1	0	1	1
↓	1	1	0	0
↓	1	1	0	1
↓	1	1	1	0
↓	1	1	1	1

4. CIRCUIT DIAGRAM



5. TIMING DIAGRAM:-



6) CONCLUSION :-

In this lab, we have implemented 4-bit binary ripple up counter with state diagram, truth table and timing diagram.

08/01/2023